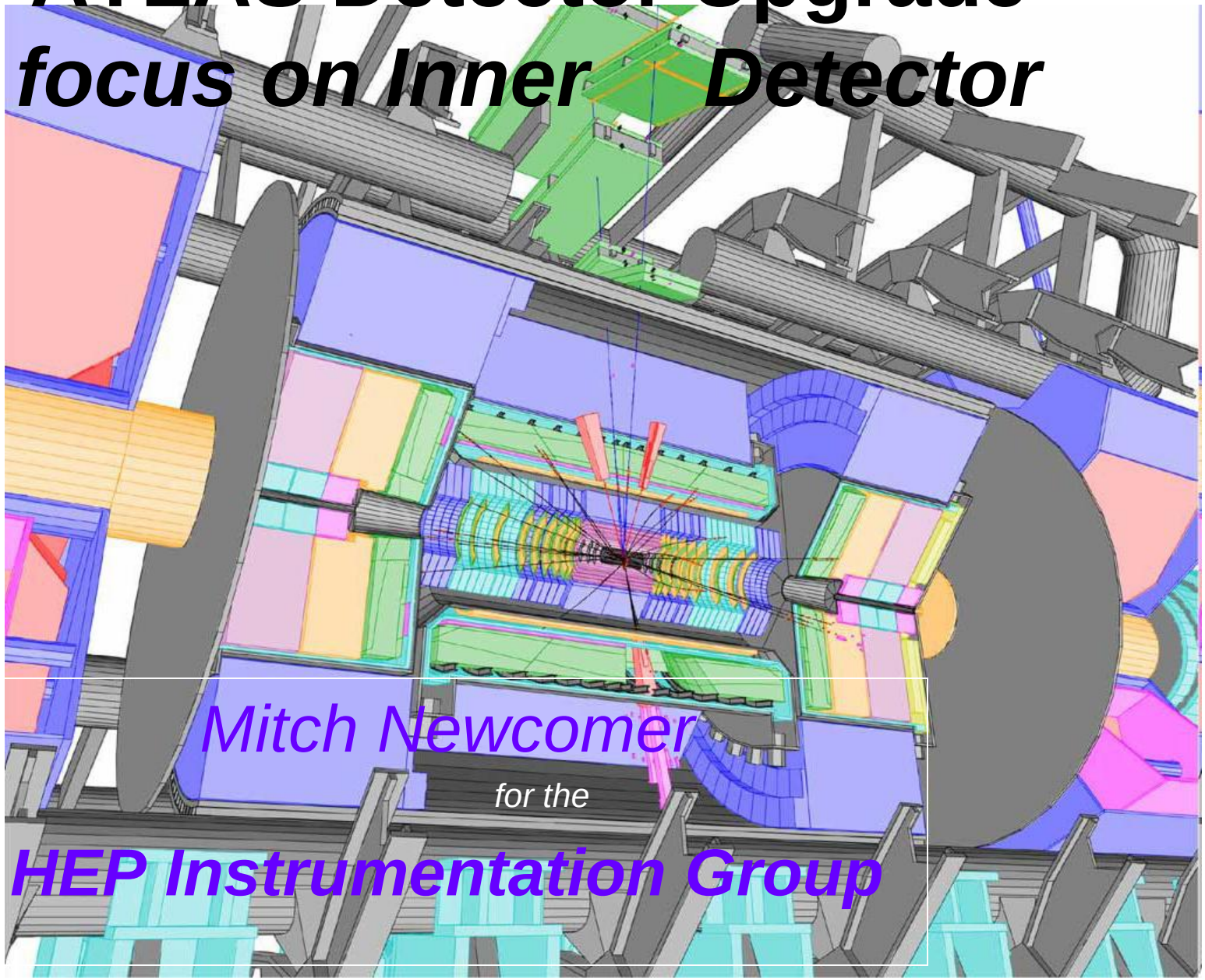
ATLAS Detector Upgrade

focus on Inner Detector



Mitch Newcomer

for the

HEP Instrumentation Group

HEP Instrumentation Group

Rick Van Berg (lead)

Nandor Dressnandt, Paul Keener, Walt Kononenko, Godwin Mayers, Mitch Newcomer, Mike Reilly and Invaluable student help

With this group we have the good fortune to be able to play a meaningful lead role in several parts of the

ATLAS UpGrade

This Talk

- Will be somewhat reductionist in starting with Silicon and emerging with an ATLAS Upgrade.
- Will not defend the upgrade based on expected Physics.
- Will assume some Unfamiliarity with the baseline ATLAS detector and will review the Inner tracker systems.
- Will describe the Novel Next Gen tracking sensors at the end..

- One hope is to encourage additional interest from within the department in Upgrade Activities especially Novel sensors that may play an important role in future detector systems either at ATLAS or some future detector.

ATLAS Detector at LHC

- Designed for Luminosity of 10^{34} p /cm^2 /s
- In the first 5 years 700 fb^{-1} * Integrated Luminosity
  - Most sensors in the inner tracker have occupancies of up to several percent @ design luminosity. TRT occupancies are highest.
- First Colliding Beams Spring/Summer 2009

* SLHC Upgrade Plans envision 3000 fb^{-1}

? Atlas Upgrade ?

With first LHC collisions set to occur in 2009 why consider a super LHC ATLAS detector now?

Designing and building the ATLAS detector was a daunting task. It is one of the most complex instruments built by people.

Concept to Reality has taken ~ 15years

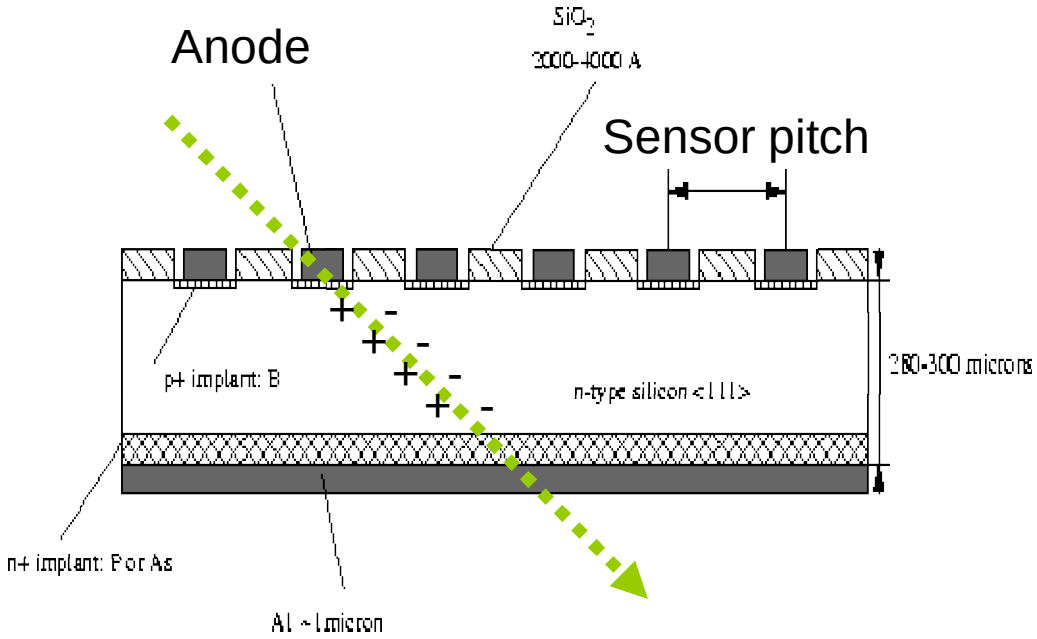
- By starting now we can take advantage of experienced designers battle hardened by the realities of producing a working detector system.
- Higher luminosity will occur in stages at LHC. A new Linac will increase the Available beam current, possibly by 2014. A better focusing scheme will intensify the concentration of protons in the interaction point and a tightning of the length of proton bunches is expected to increase the luminosity to 10^{35} by 2017.
- Even at the proposed Luminosity of 10^{34} p/cm^2/s sub-systems within the detector will need replacement in the first few years of LHC operation.
- An obvious strategy is to focus contributions on systems with the highest priority for replacement as beam luminosity evolves upwards.

Silicon Tracking Detectors

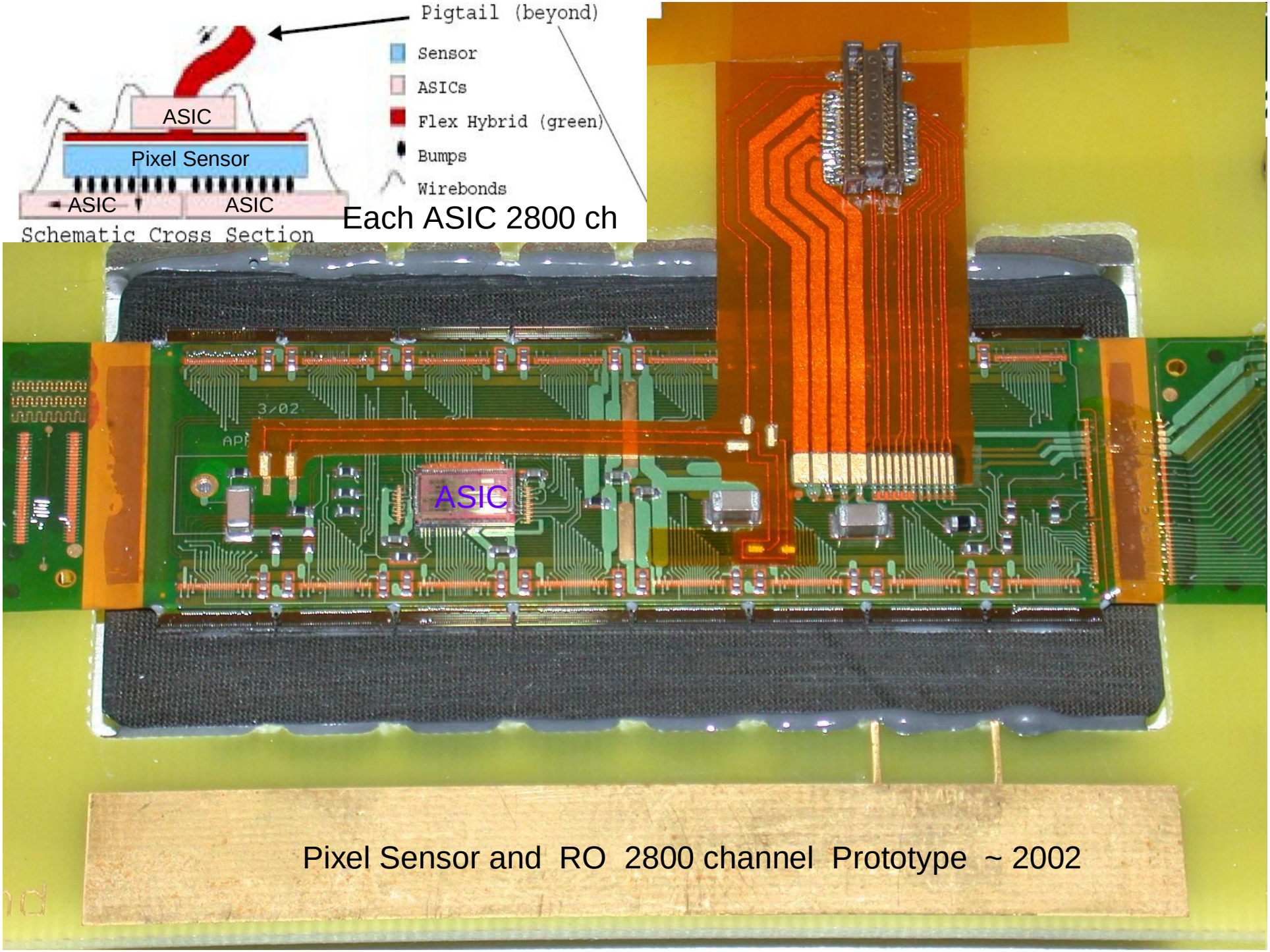
- Ionization Energy 3.6eV
- 390 eV/um
- Gain ~1
- Typical Signal 30,000e
- Charge Collection time~30ns
- Charge Collection node shape determines tracking coordinate precision.

  Pixels ~ 50um X 400um

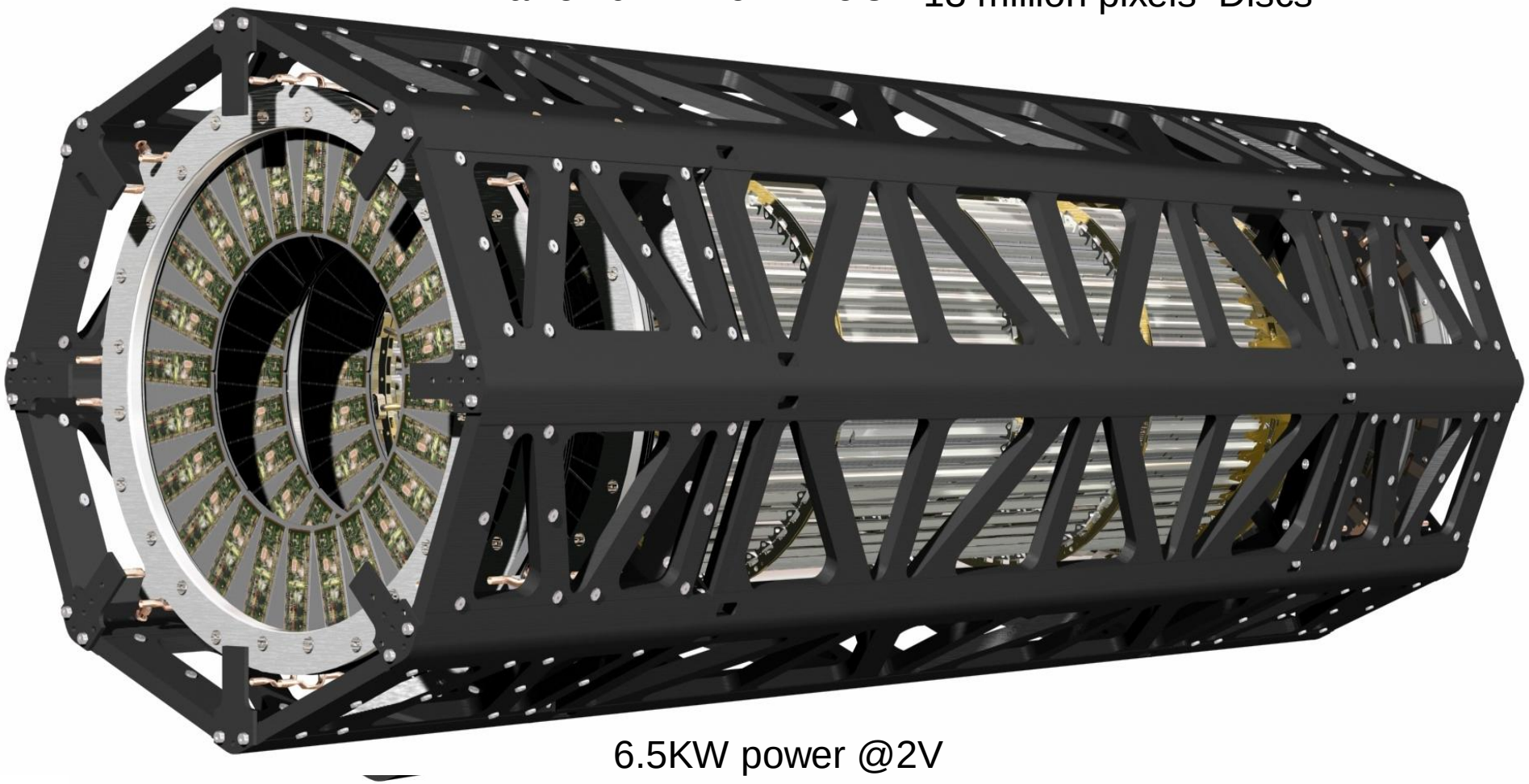
  Strips ~ 50um X 10cm



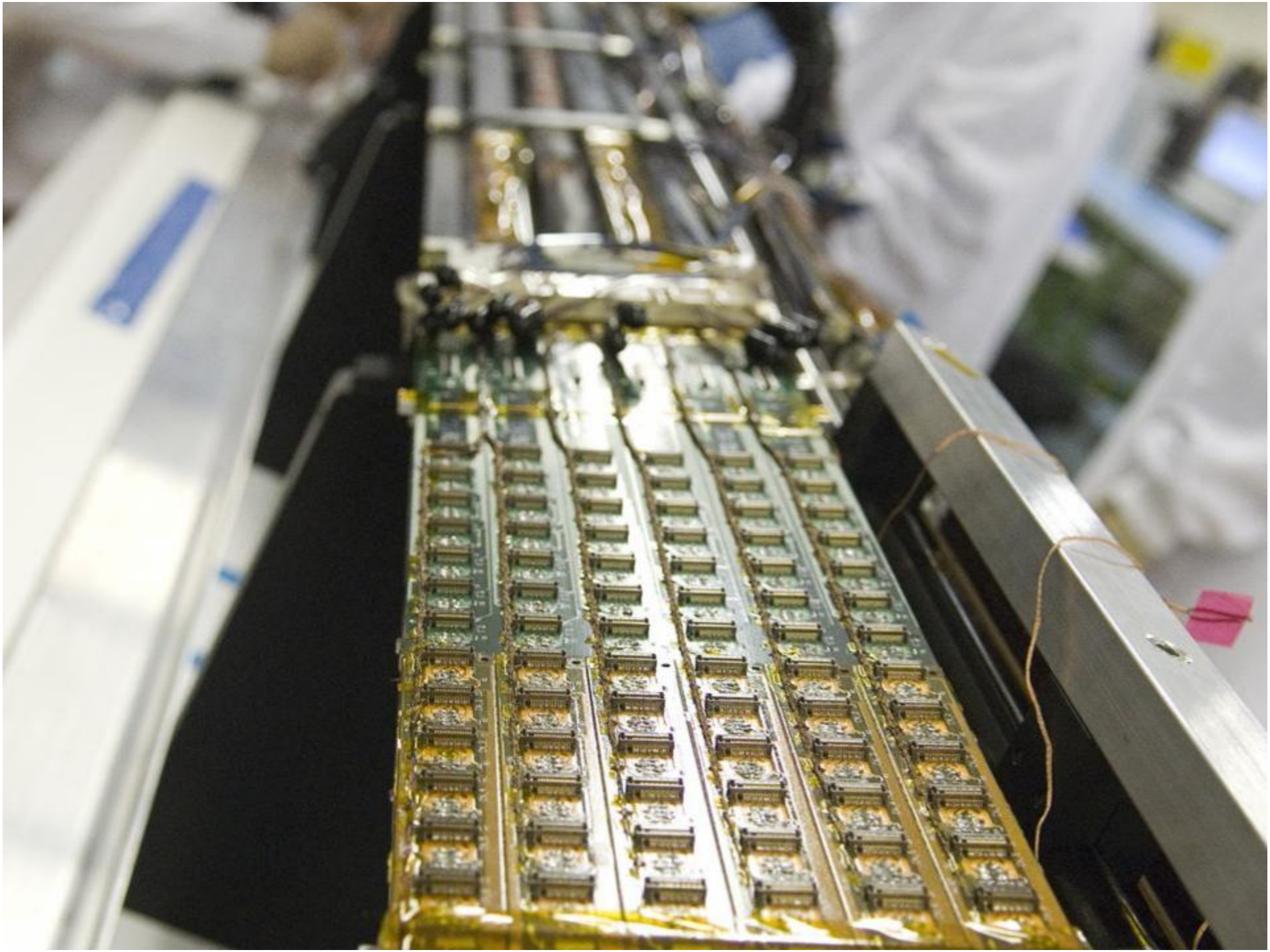
The ATLAS Pixel Detector

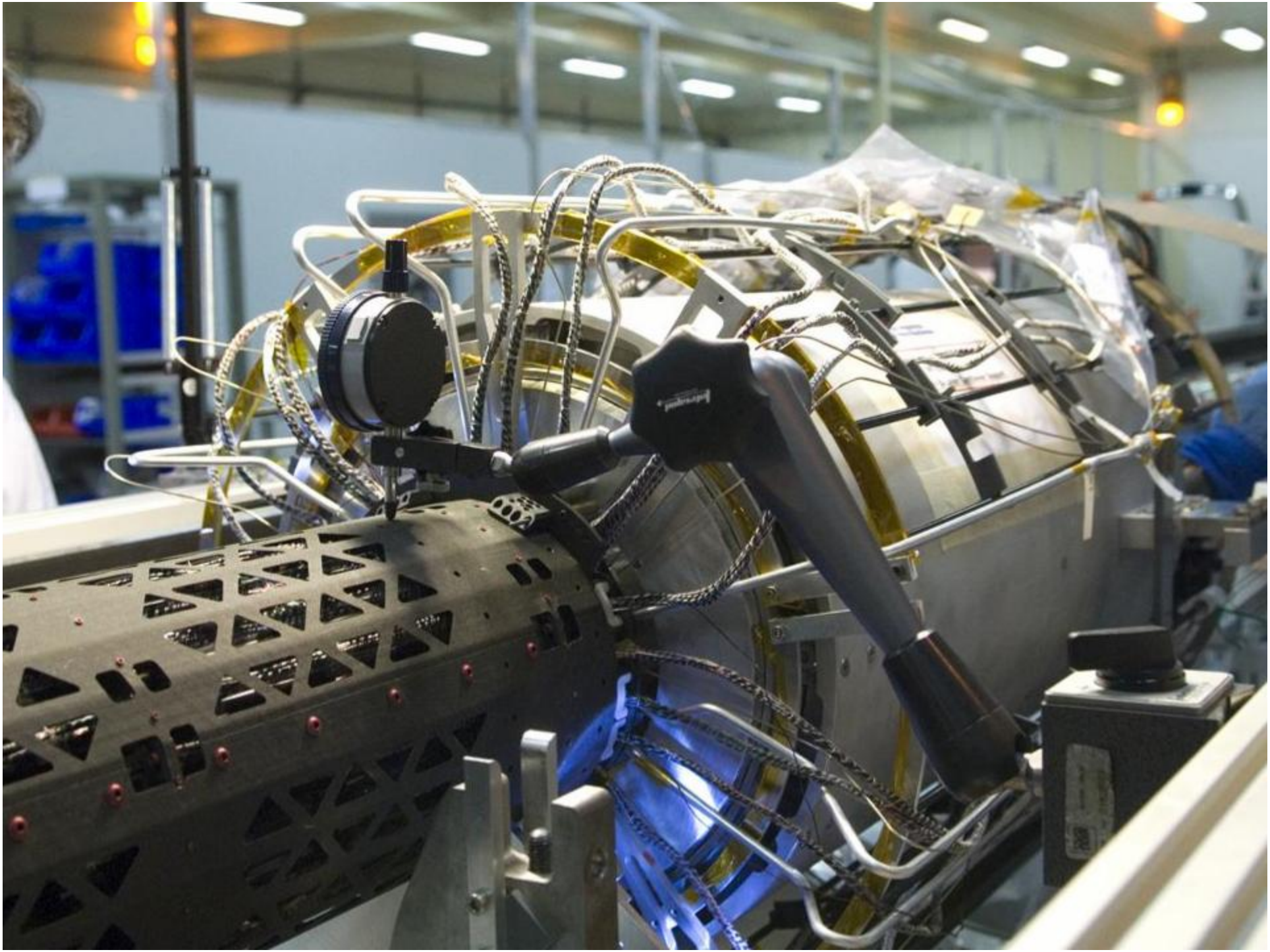

Pigtail (beyond)
Sensor
ASICs
Flex Hybrid (green)
Bumps
Wirebonds
ASIC
Pixel Sensor
ASIC
ASIC
Schematic Cross Section
Each ASIC 2800 ch
ASIC
Pixel Sensor and RO 2800 channel Prototype ~ 2002

Barrel 67 million Pixels 13 million pixels Discs



6.5KW power @2V
10% Radiation Length Material
Useful to an Exposure of 50MRad



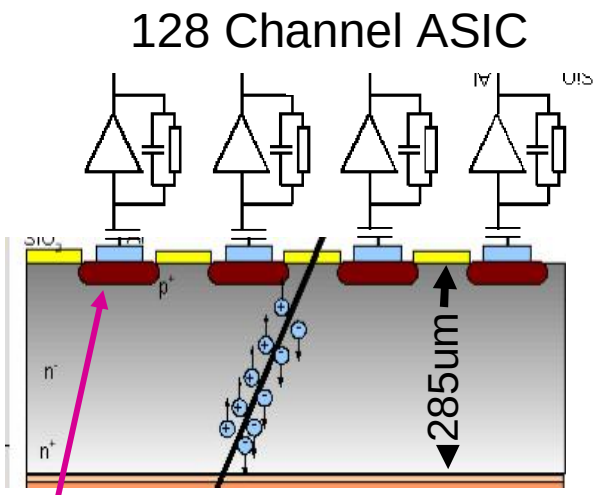



A-Side

The Silicon Strip Tracker (SCT)

SCT detectors are AC-coupled, single-sided strip detectors based on p+ strip implants in an n-type silicon bulk. The strips are biased through polysilicon or implant resistors from a common bias line which surrounds all strips on a wafer. The detector edge and guard ring design varies depending on the manufacturer. Due to radiation induced changes of the bulk effective doping concentration, we require the detectors (and all related components on hybrid and supply system) to operate reliably up to 500 V. After irradiation we expect an operation voltage of approximately 350 V with the measured pre-irradiation values for the full depletion voltage typically in the range of 60–80 V.

ATLAS irradiation studies of n-in-n and p-in-n silicon microstrip detectors, P. Allport et.al. NIM A435 (1999)

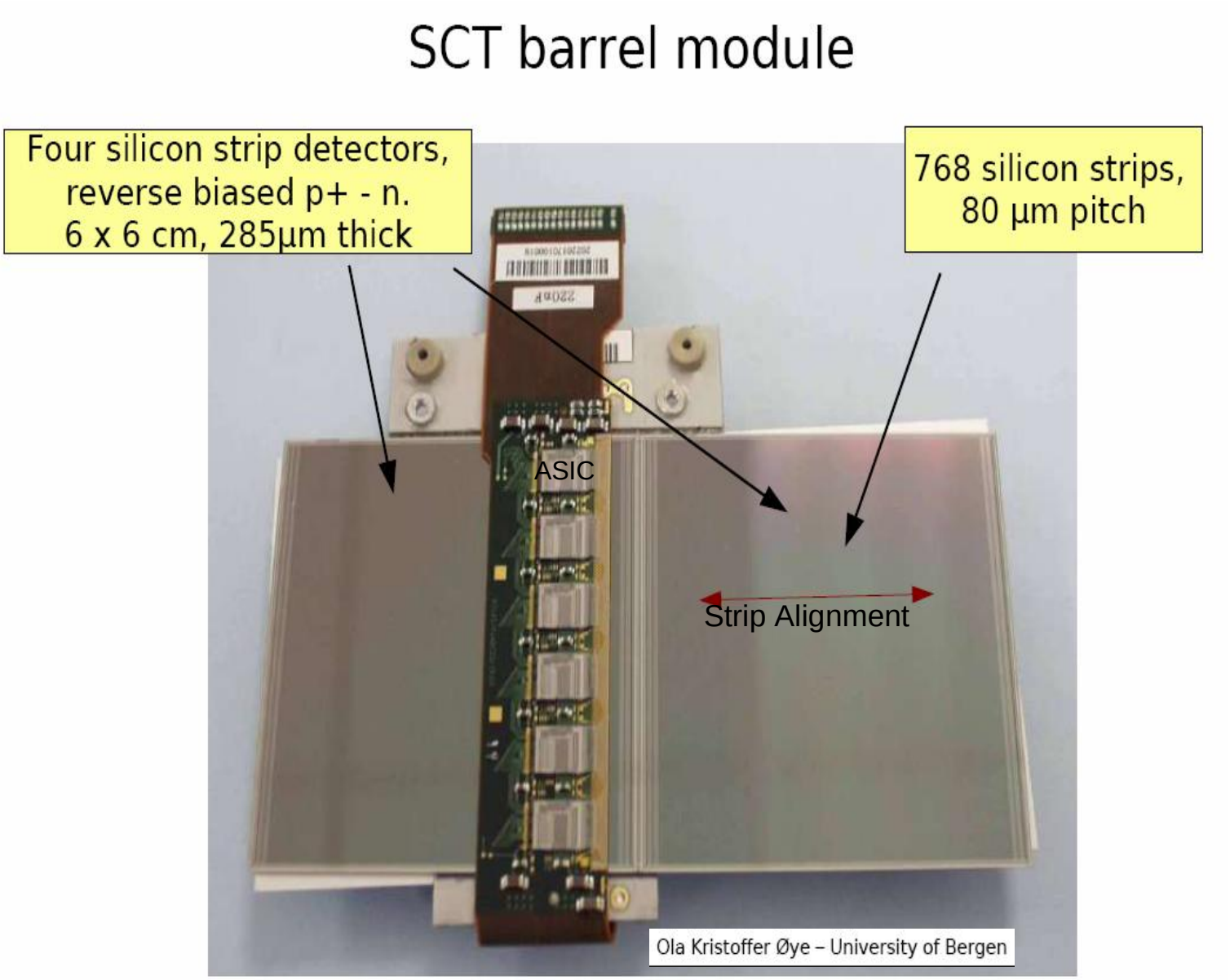


Strips:

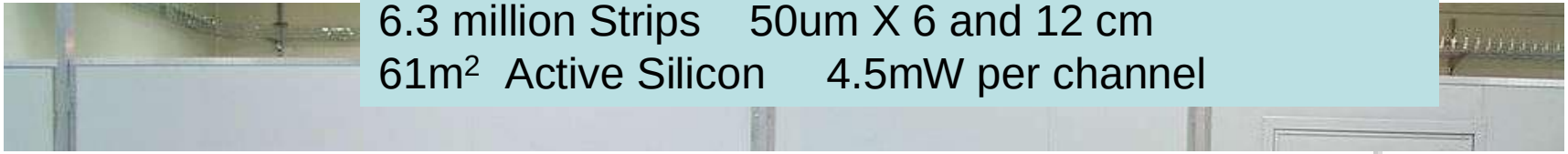
Pitch 80um

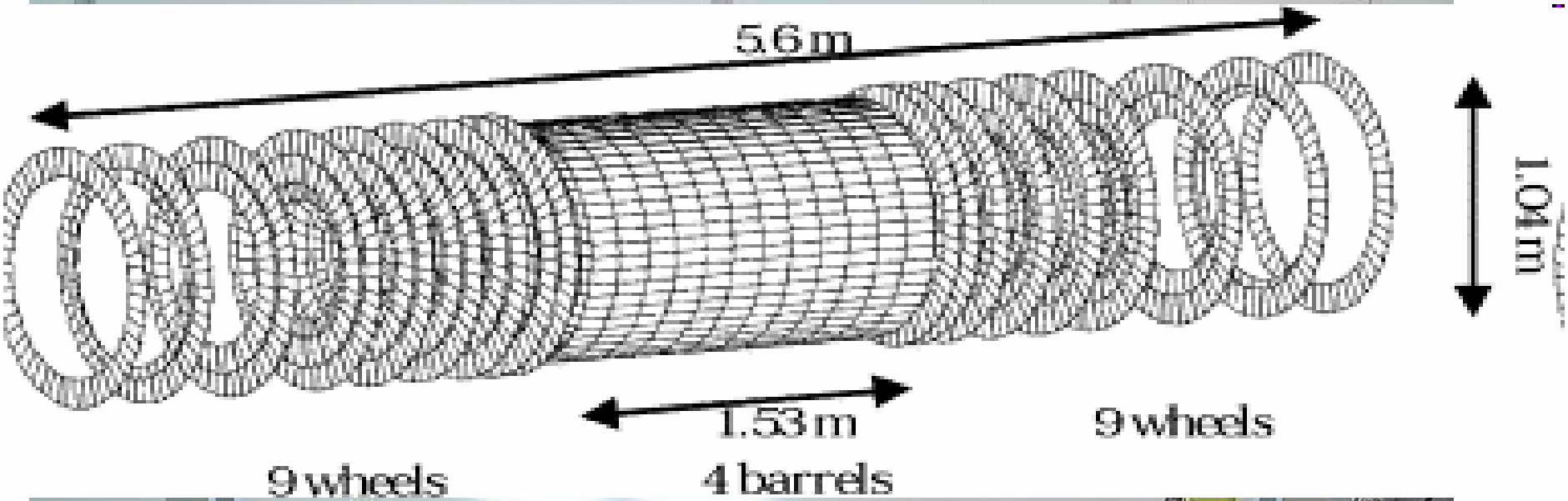
Length 6 and 12 cm

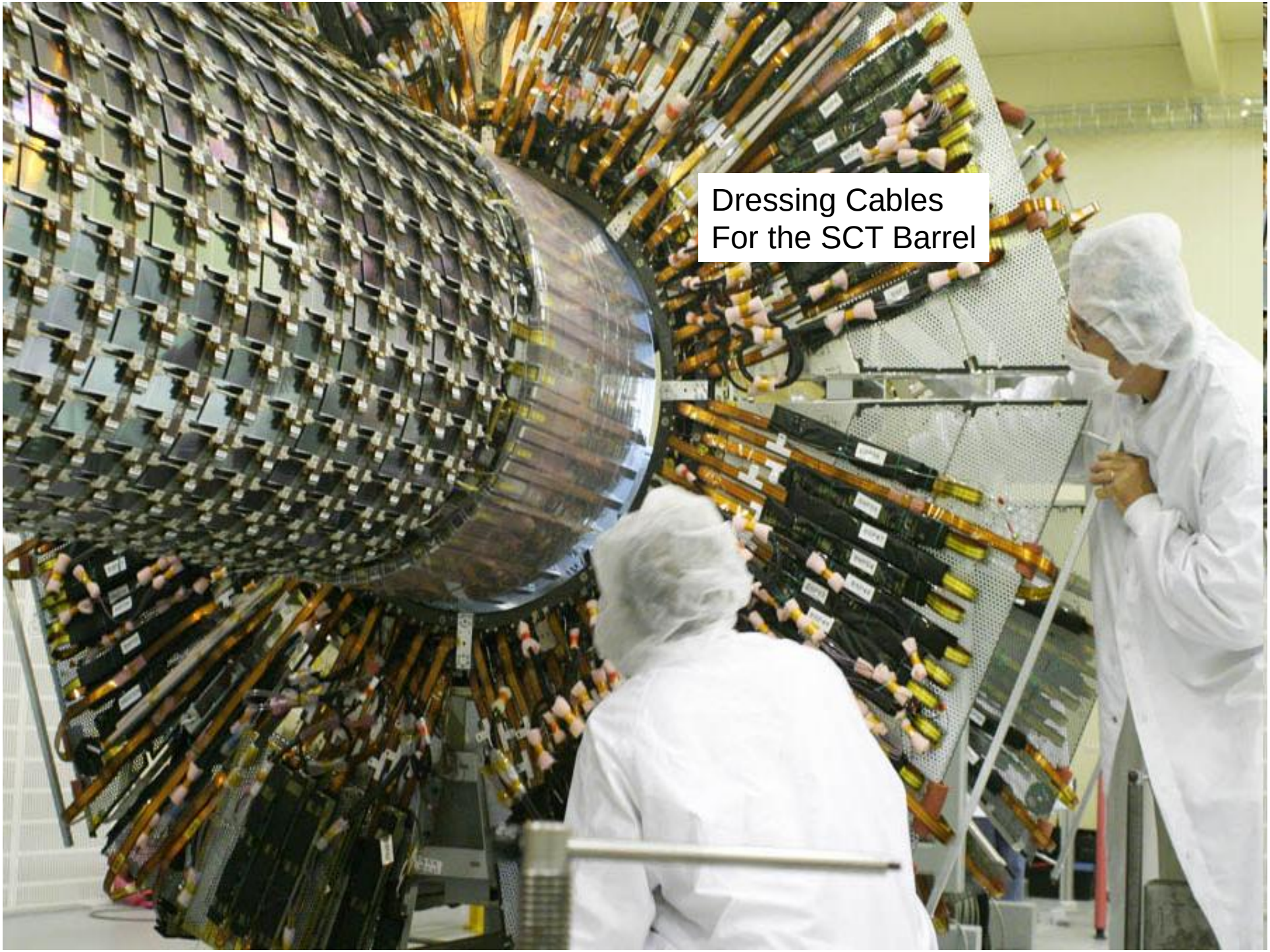
SCT barrel module

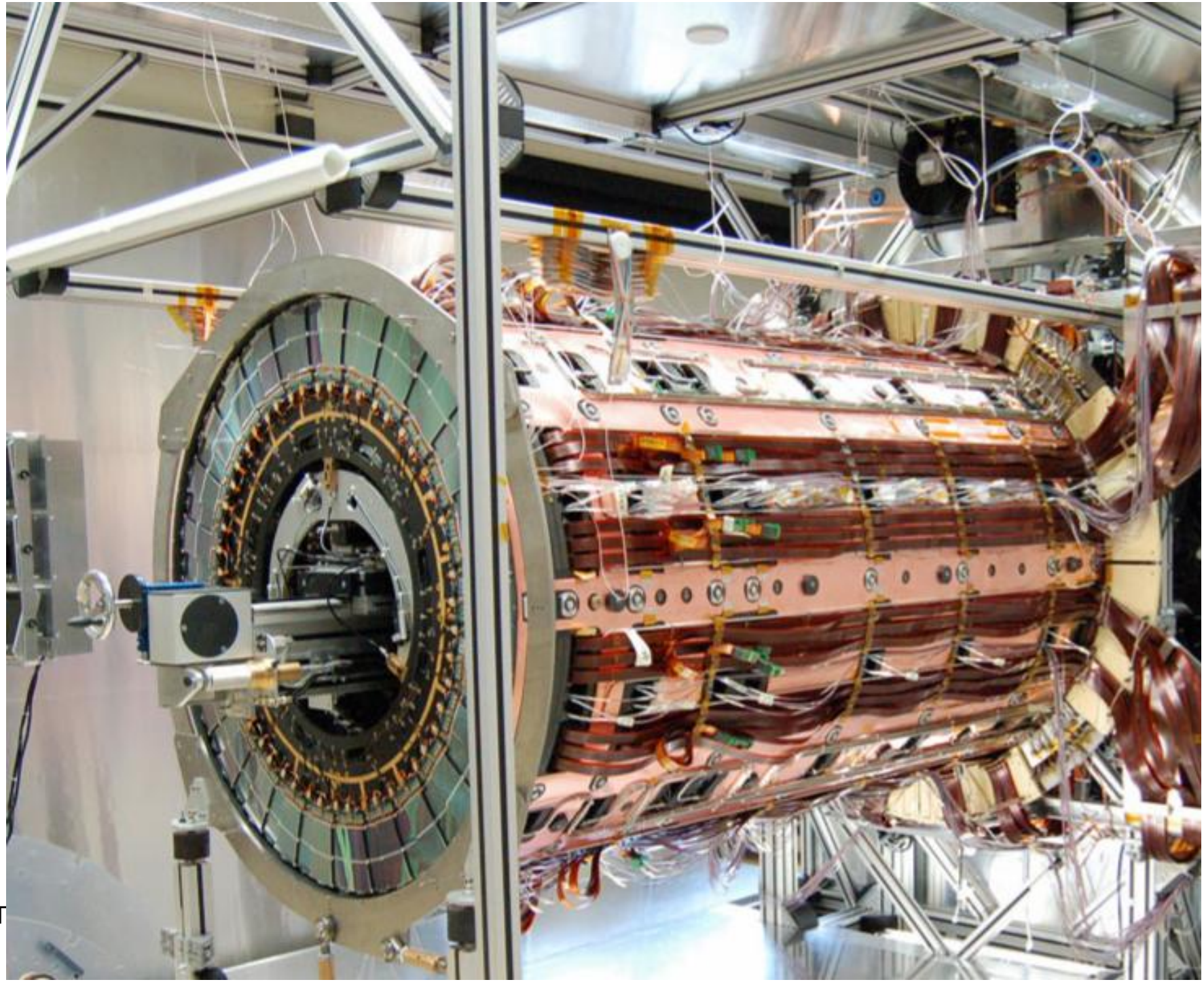


Silicon Strip Detector Barrel and (Partial) End Caps
6.3 million Strips 50um X 6 and 12 cm
61m^2 Active Silicon 4.5mW per channel



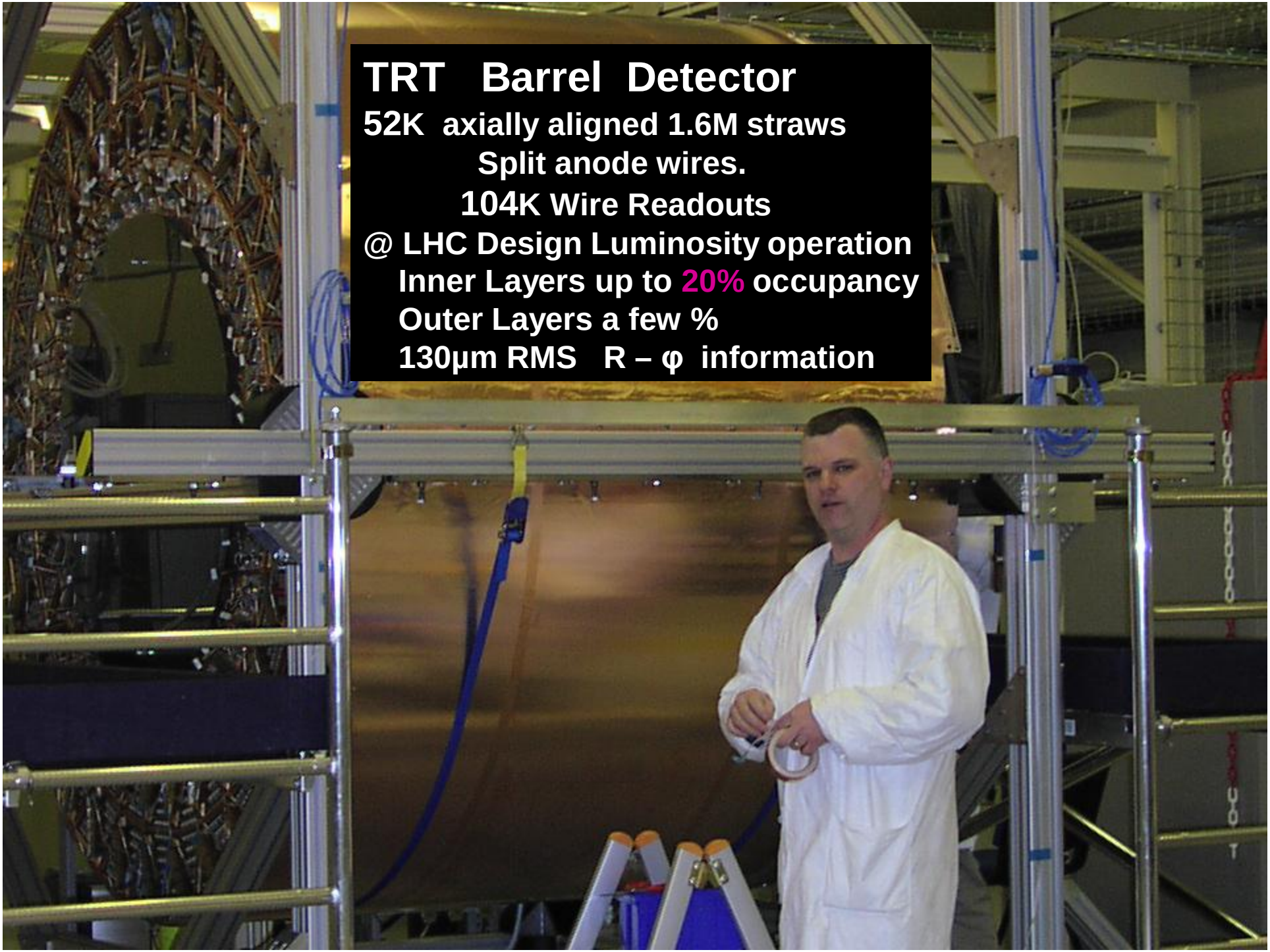


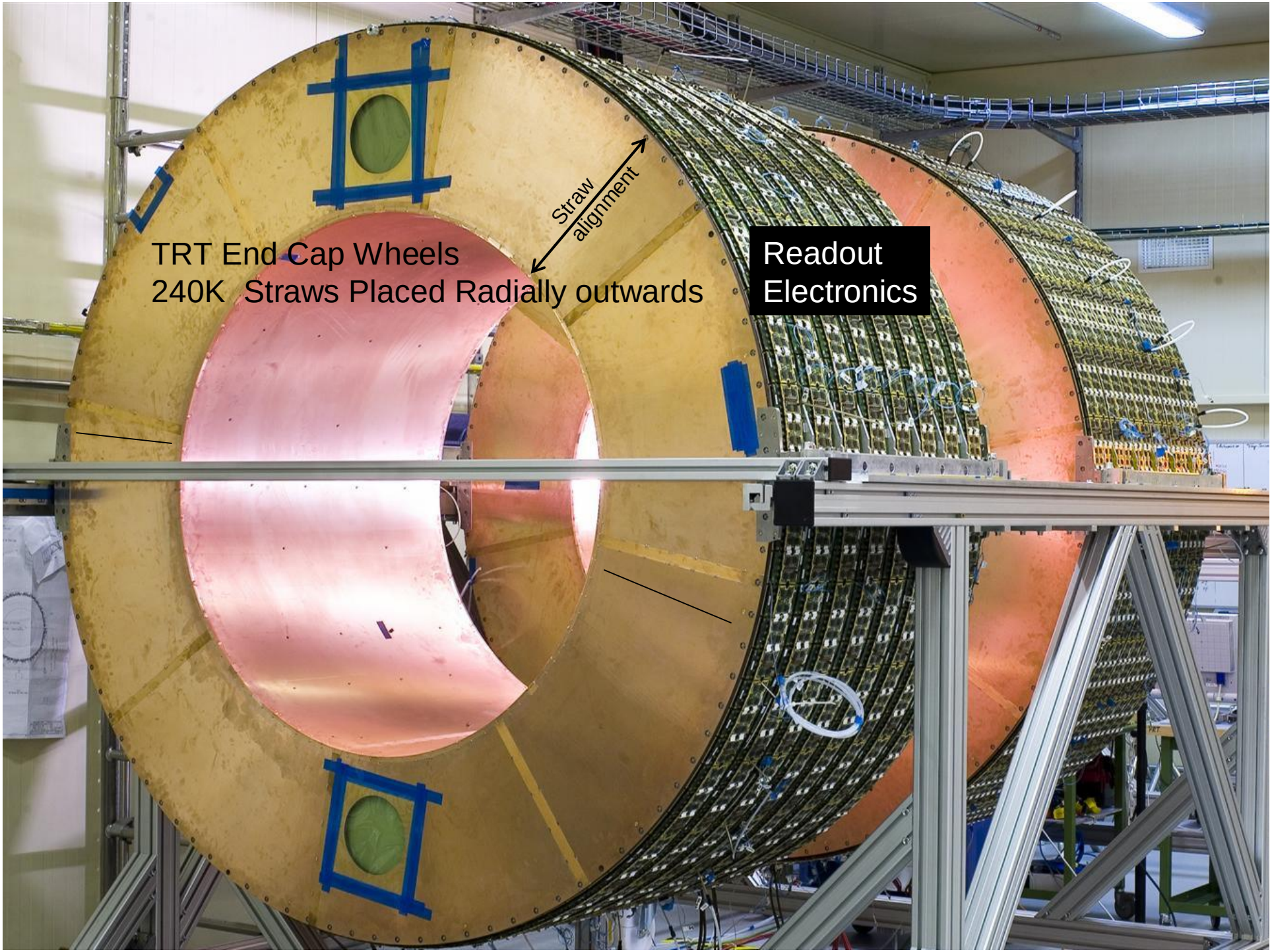

Dressing Cables
For the SCT Barrel

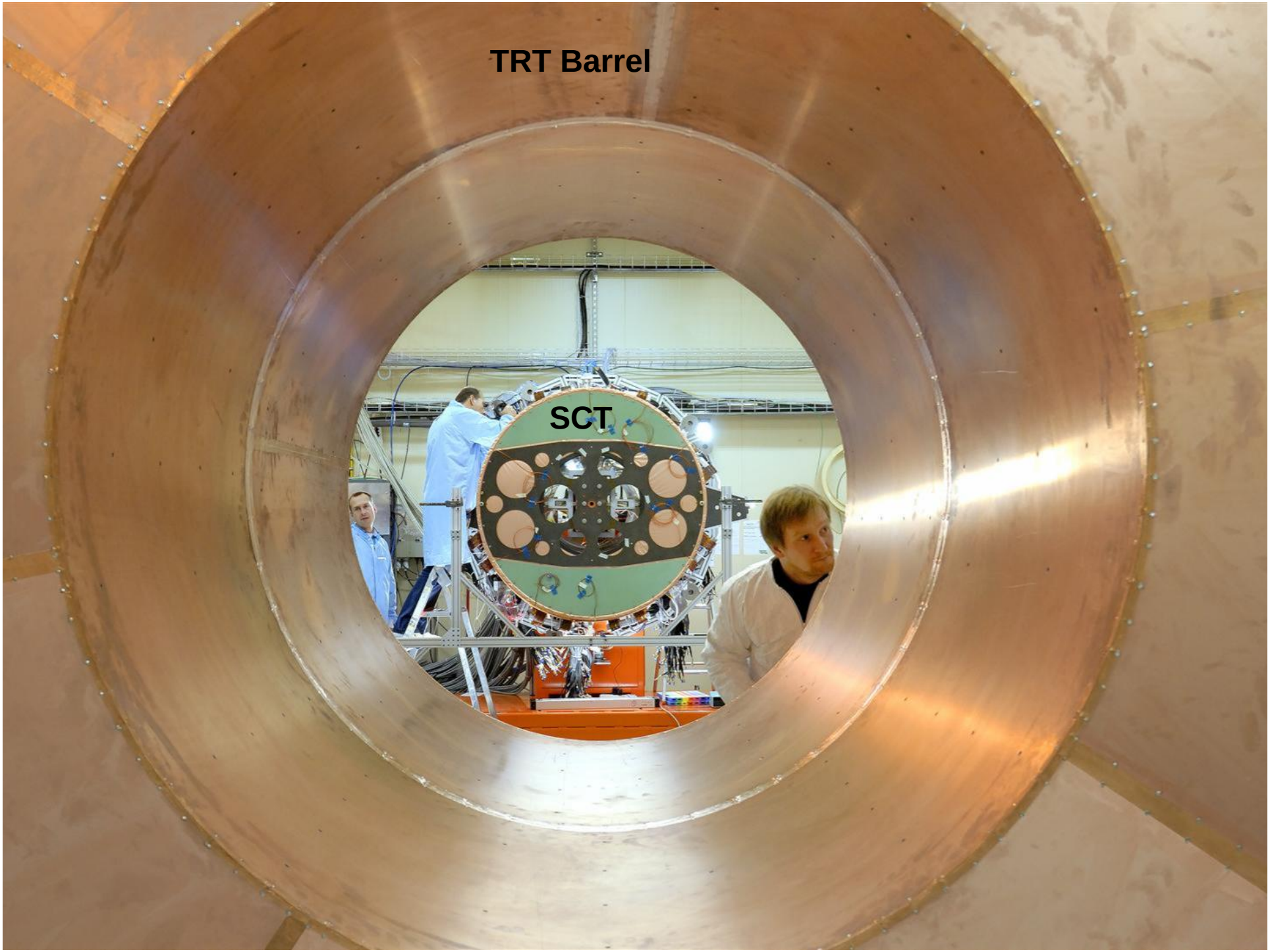


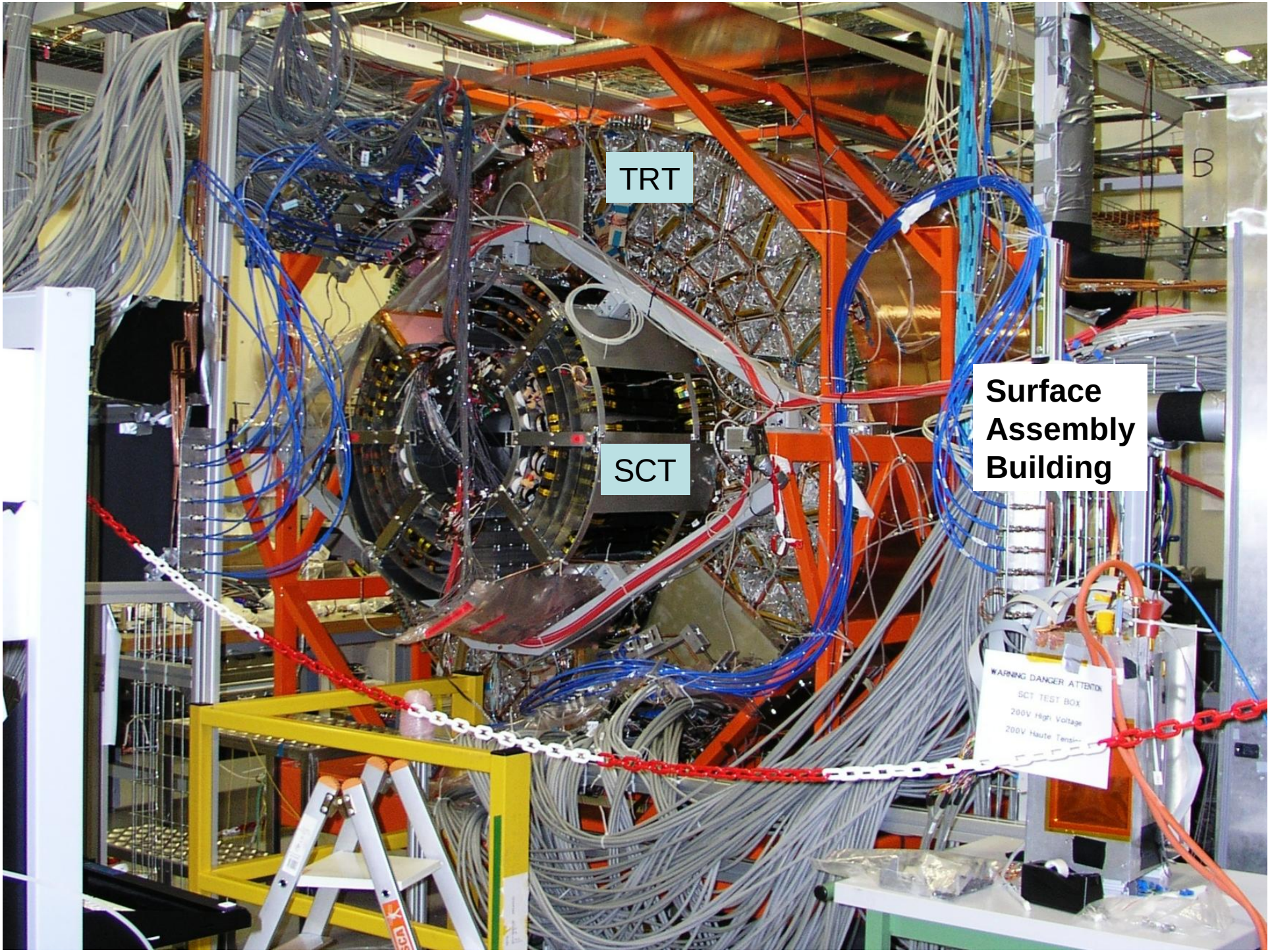
AT

The
Transition Radiation Detector

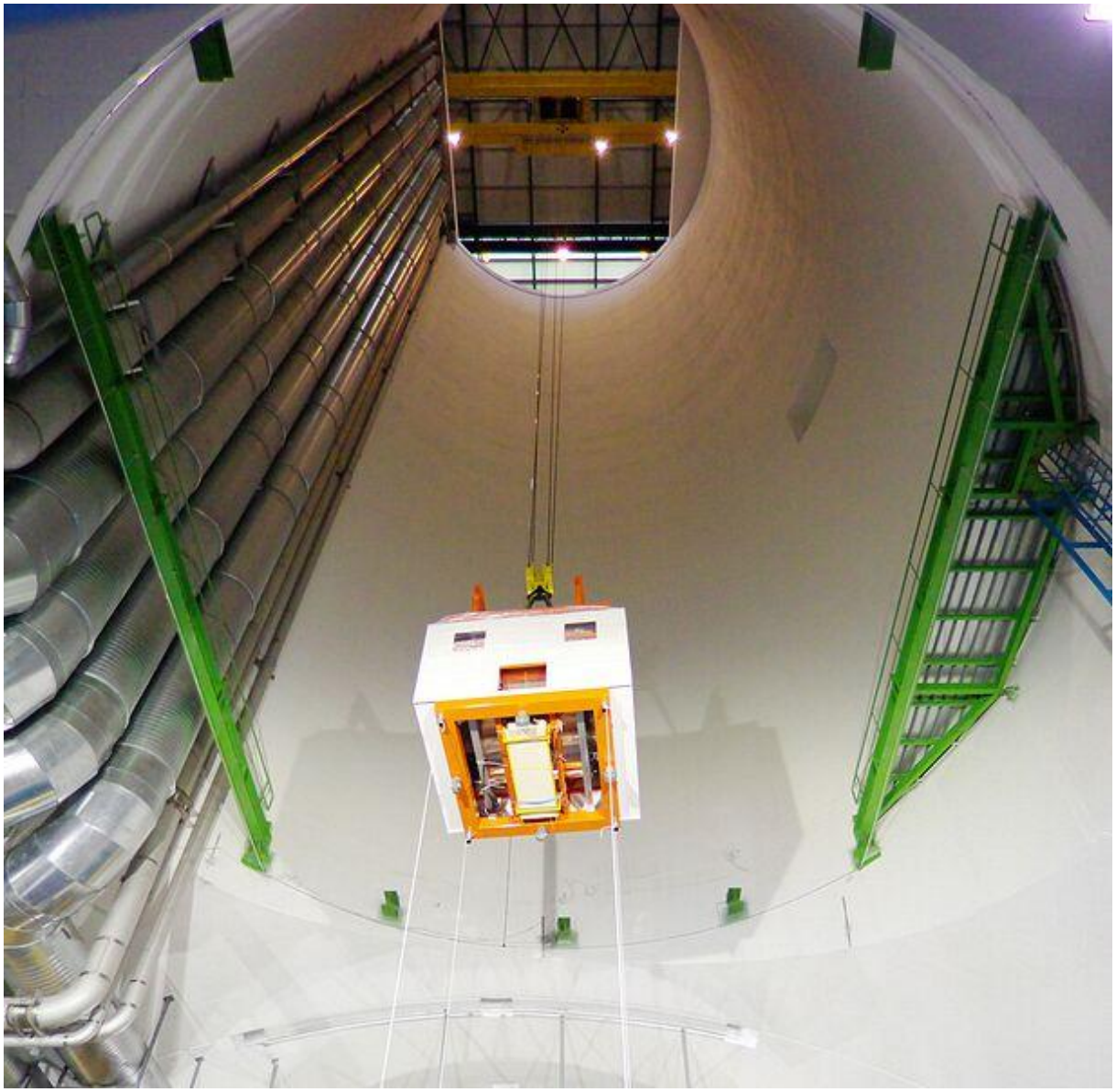

TRT Barrel Detector
52K axially aligned 1.6M straws
Split anode wires.
104K Wire Readouts
@ LHC Design Luminosity operation
Inner Layers up to 20% occupancy
Outer Layers a few %
130μm RMS R – φ information

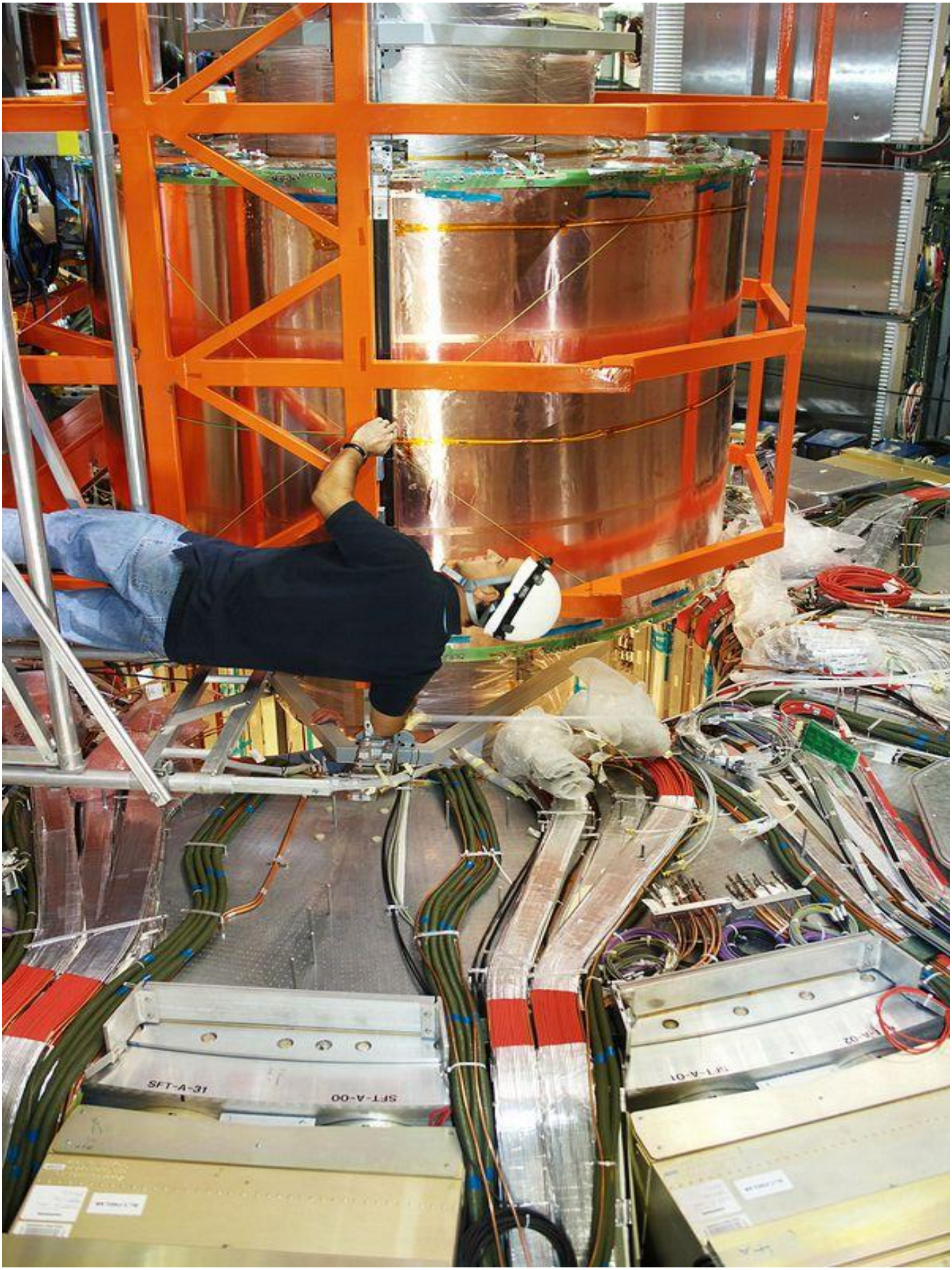

TRT End Cap Wheels
240K Straws Placed Radially outwards
Straw alignment
Readout Electronics

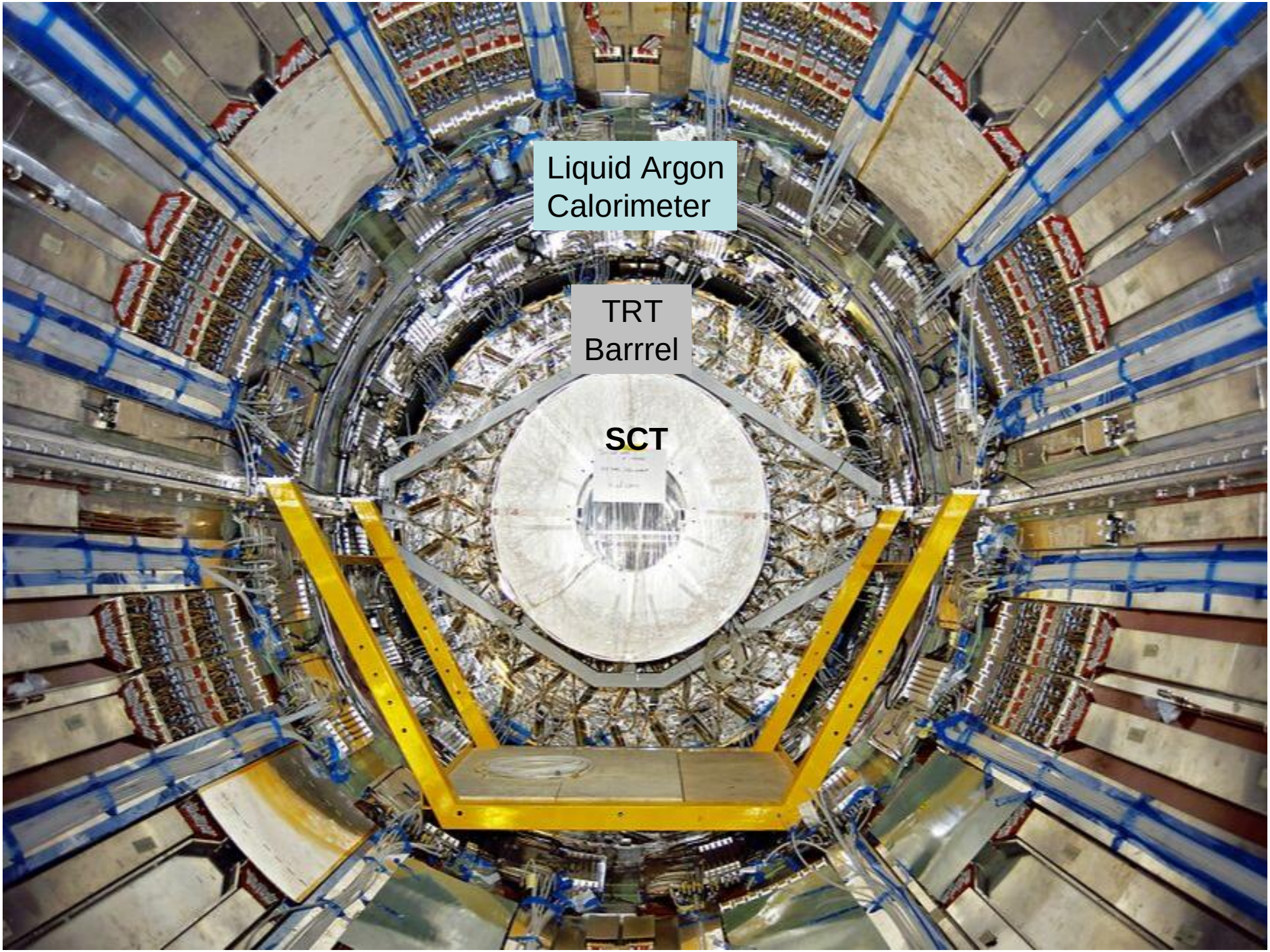

TRT Barrel
SCT

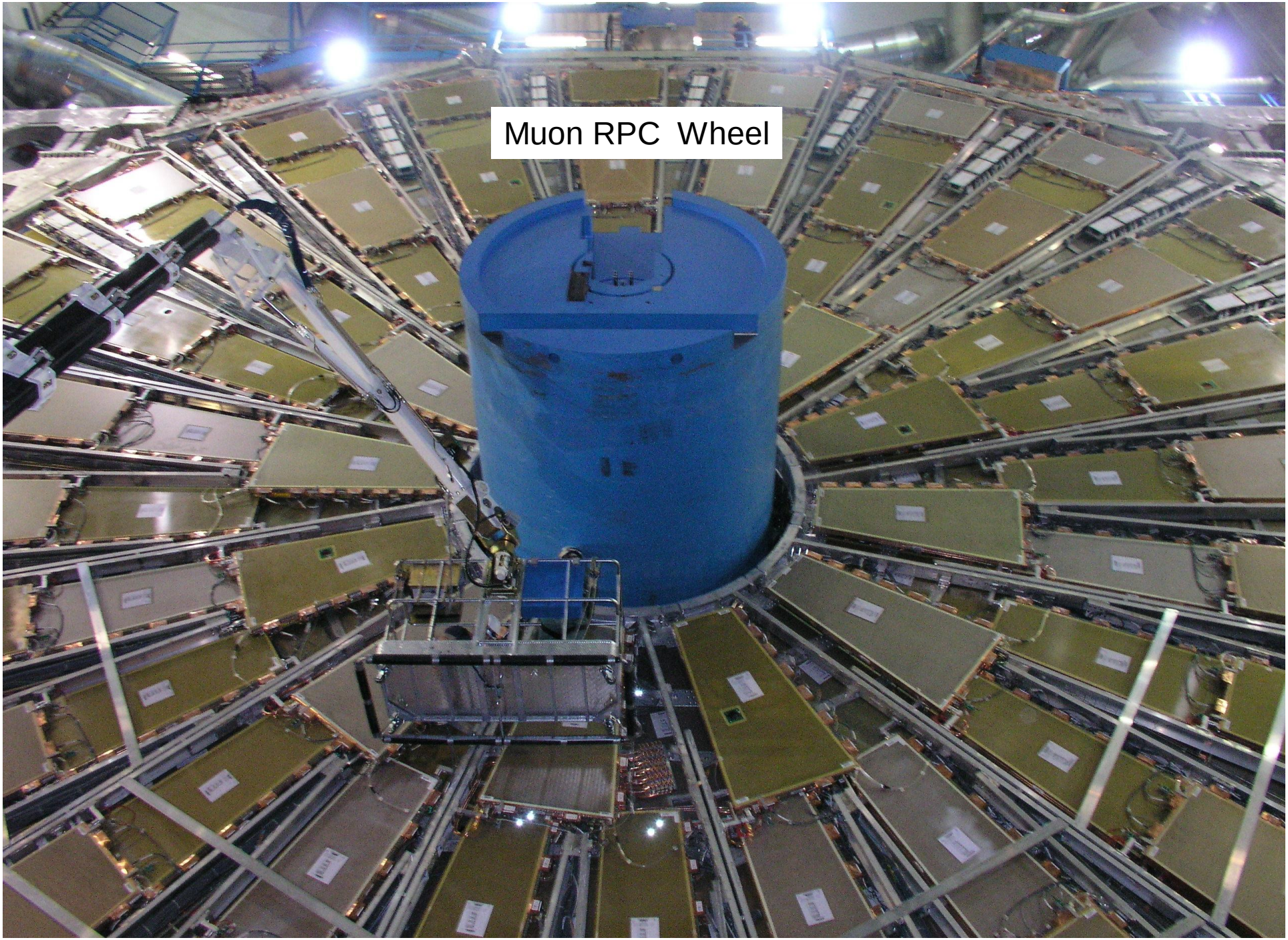

TRT
SCT
Surface Assembly Building
B
WARNING DANGER ATTENTION
SCT TEST BOX
200V High Voltage
200V Haute Tensi

ATLAS



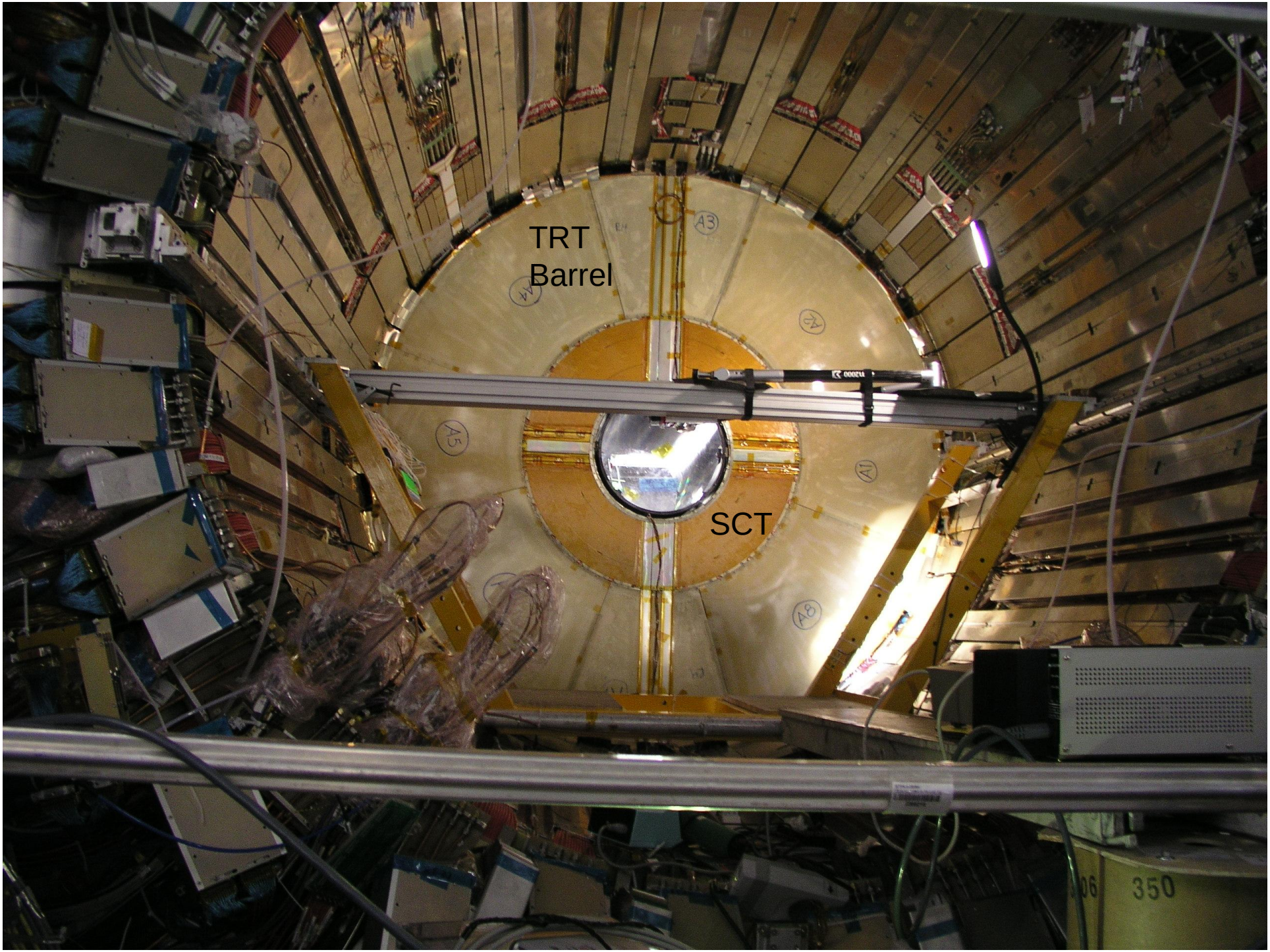

SFT-A-31
SFT-A-00

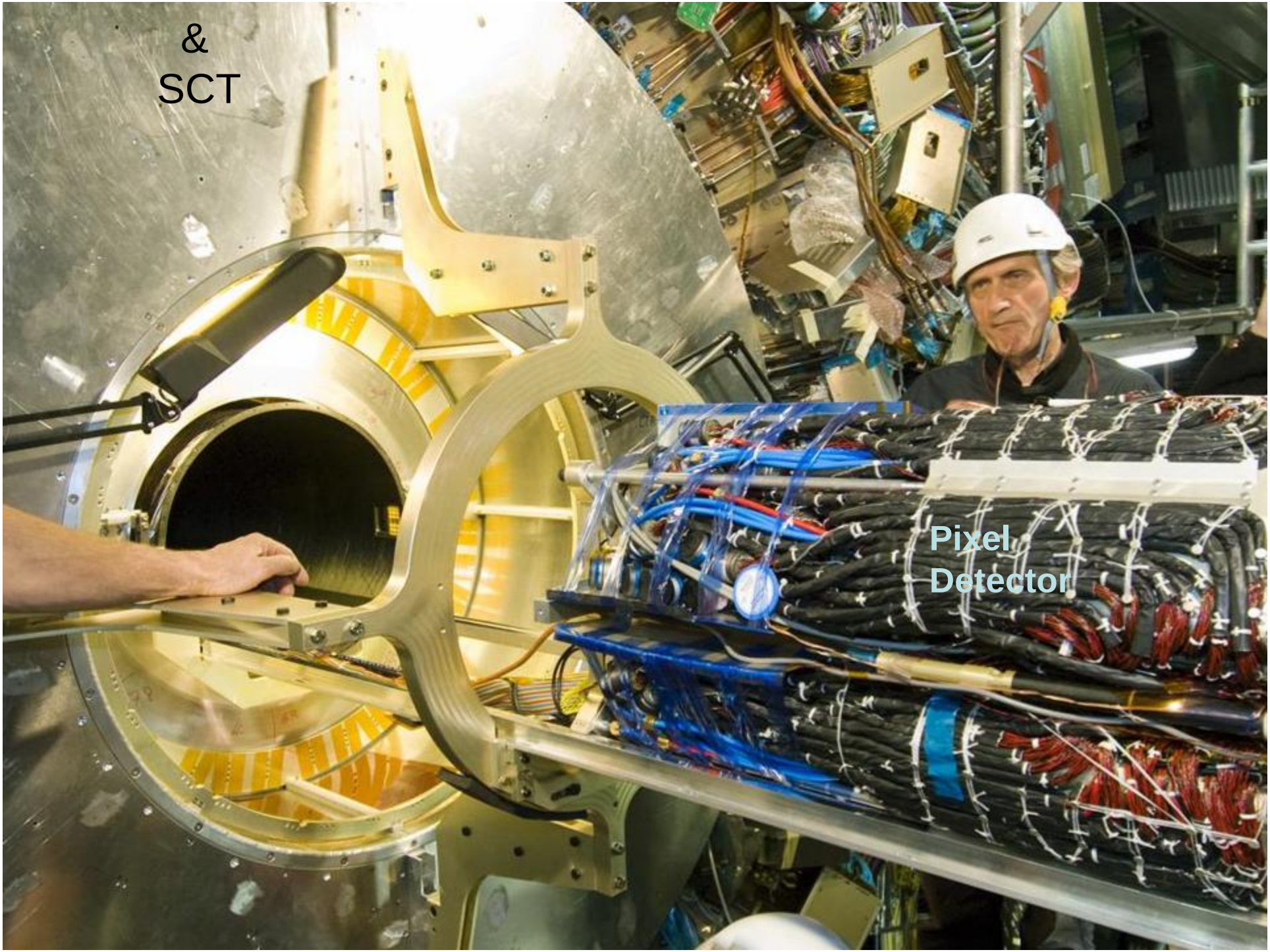

Liquid Argon
Calorimeter
TRT
Barrrel
SCT

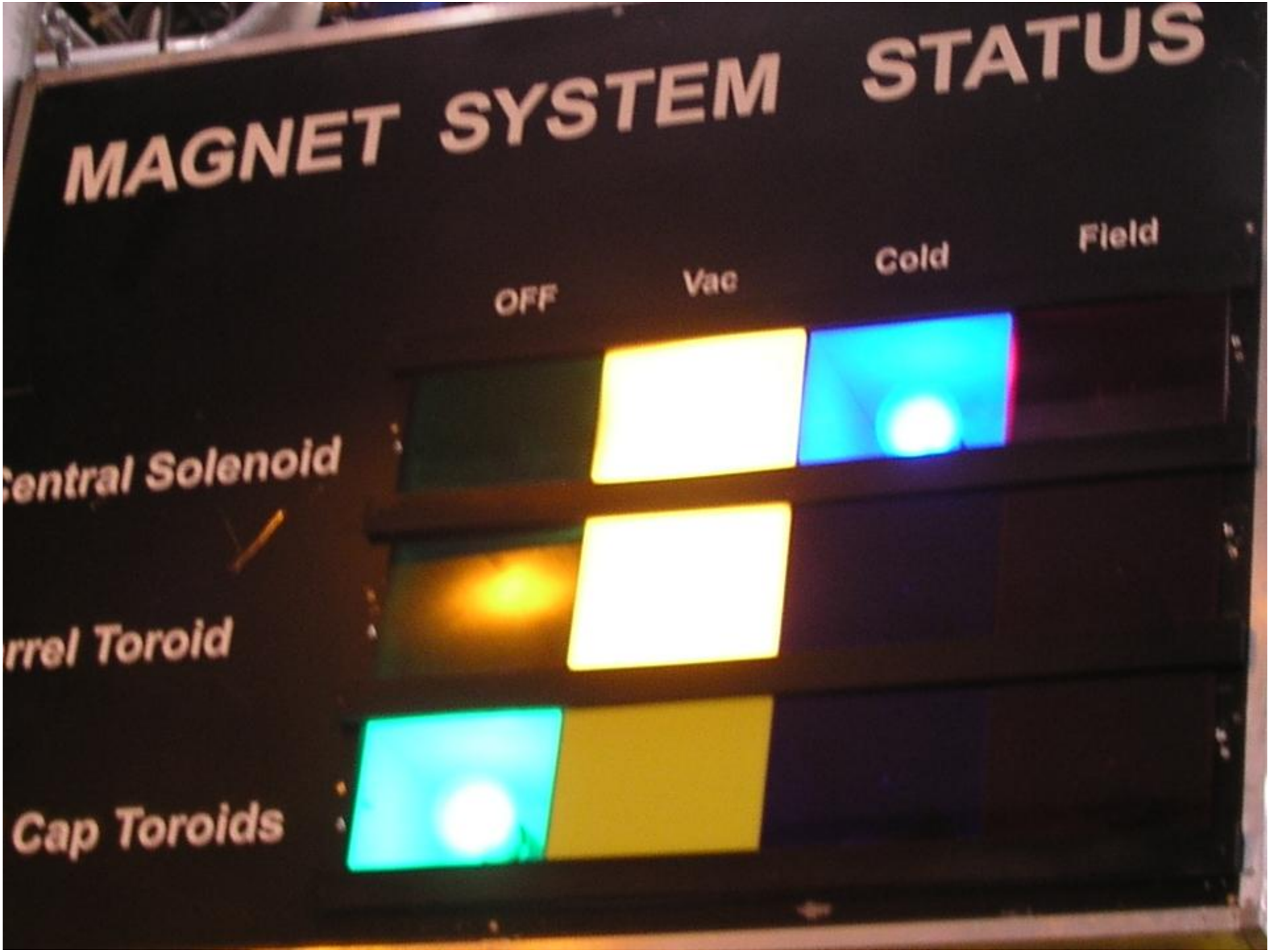

Muon RPC Wheel


Jack Fowler, Duke
Wiring the TRT


Ben Legit
Mike
Hance

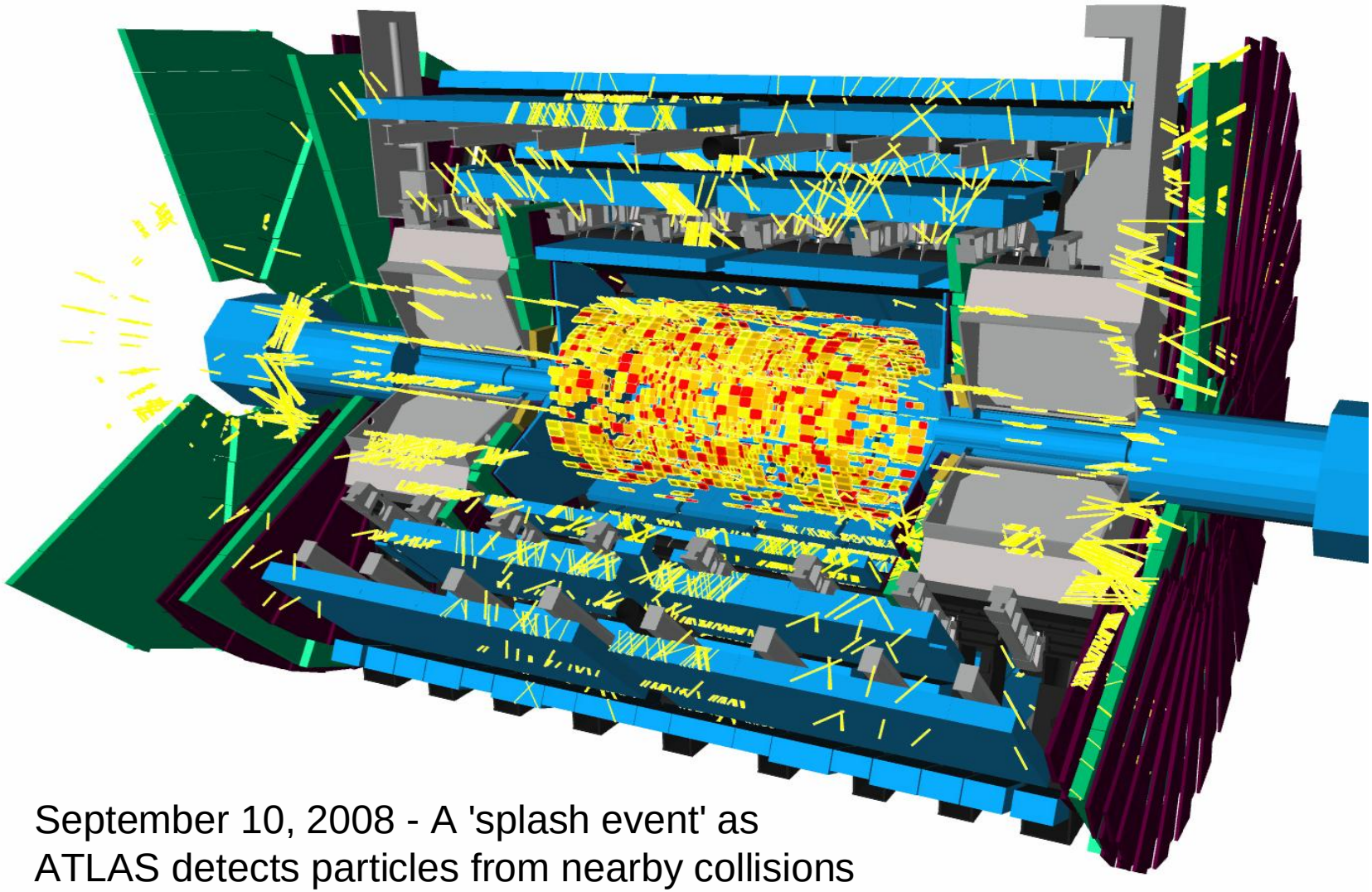

TRT
Barrel
SCT


&
SCT
Pixel
Detector

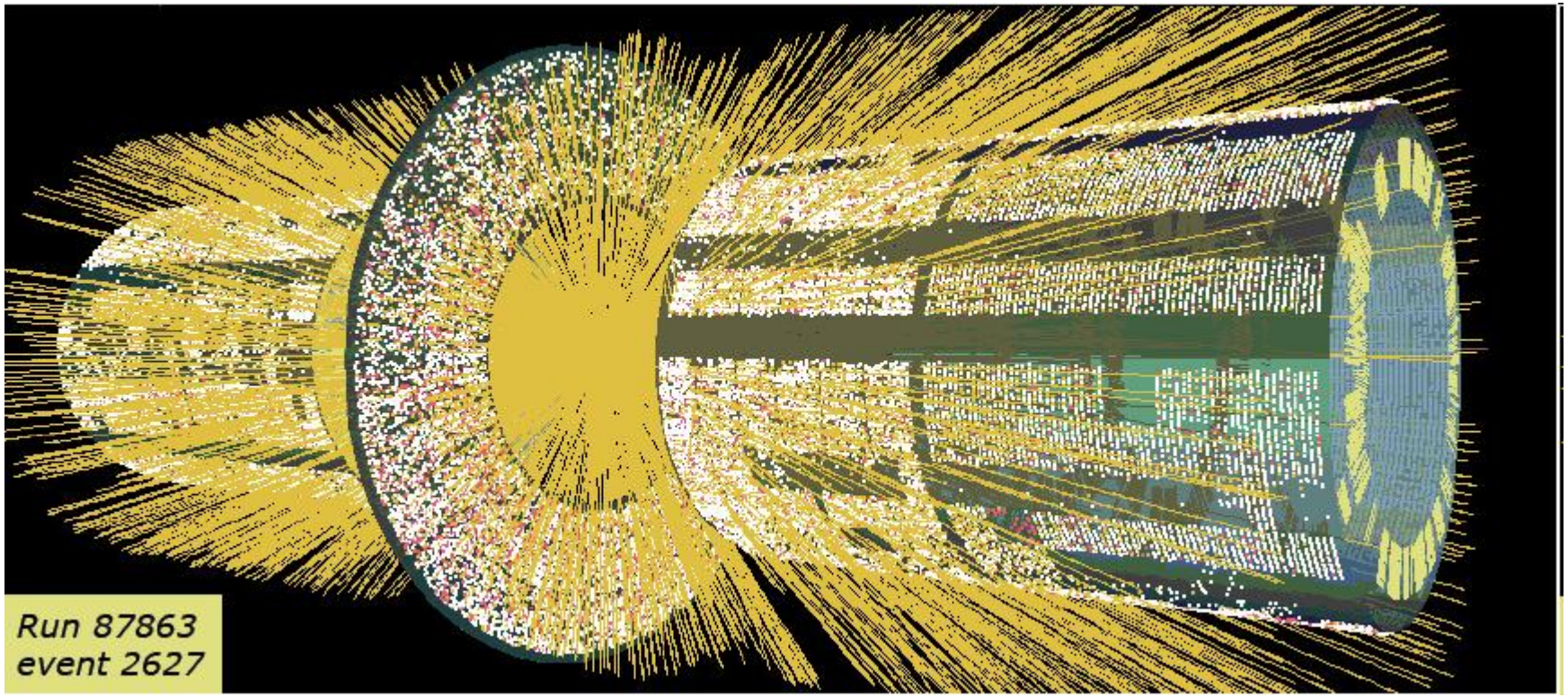

MAGNET SYSTEM STATUS
OFF
Vac
Cold
Field
entral Solenoid
rrel Toroid
Cap Toroids

First Events

September 10, 2008



September 10, 2008 - A 'splash event' as ATLAS detects particles from nearby collisions from the first beams through the LHC



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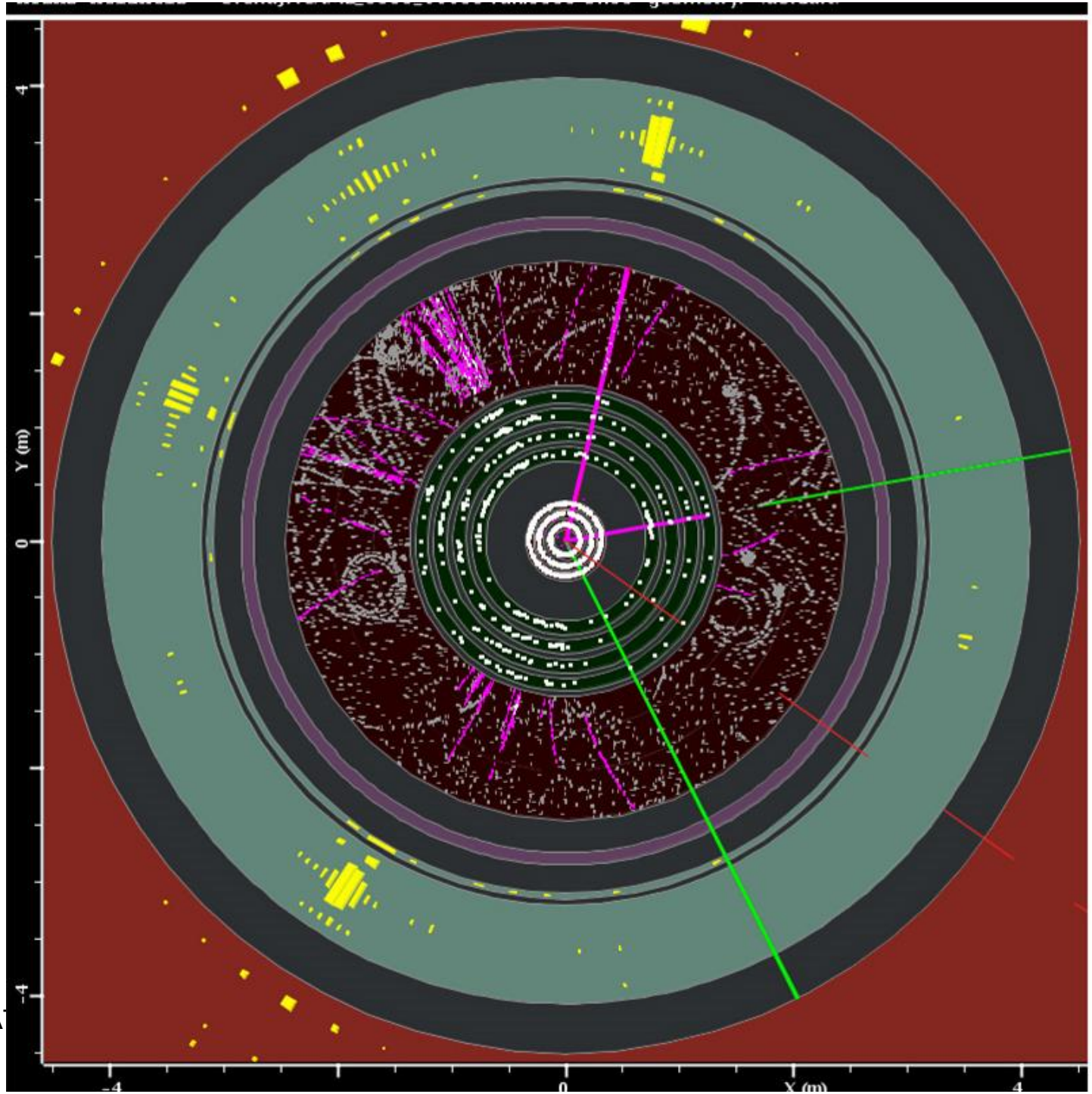


September 10, 2008 - A 'splash event' as ATLAS detects particles from nearby collisions from the first beams through the LHC.

Upgrades to The ATLAS Inner Detector

Goals for Upgrade

The goals for the Upgrade are:

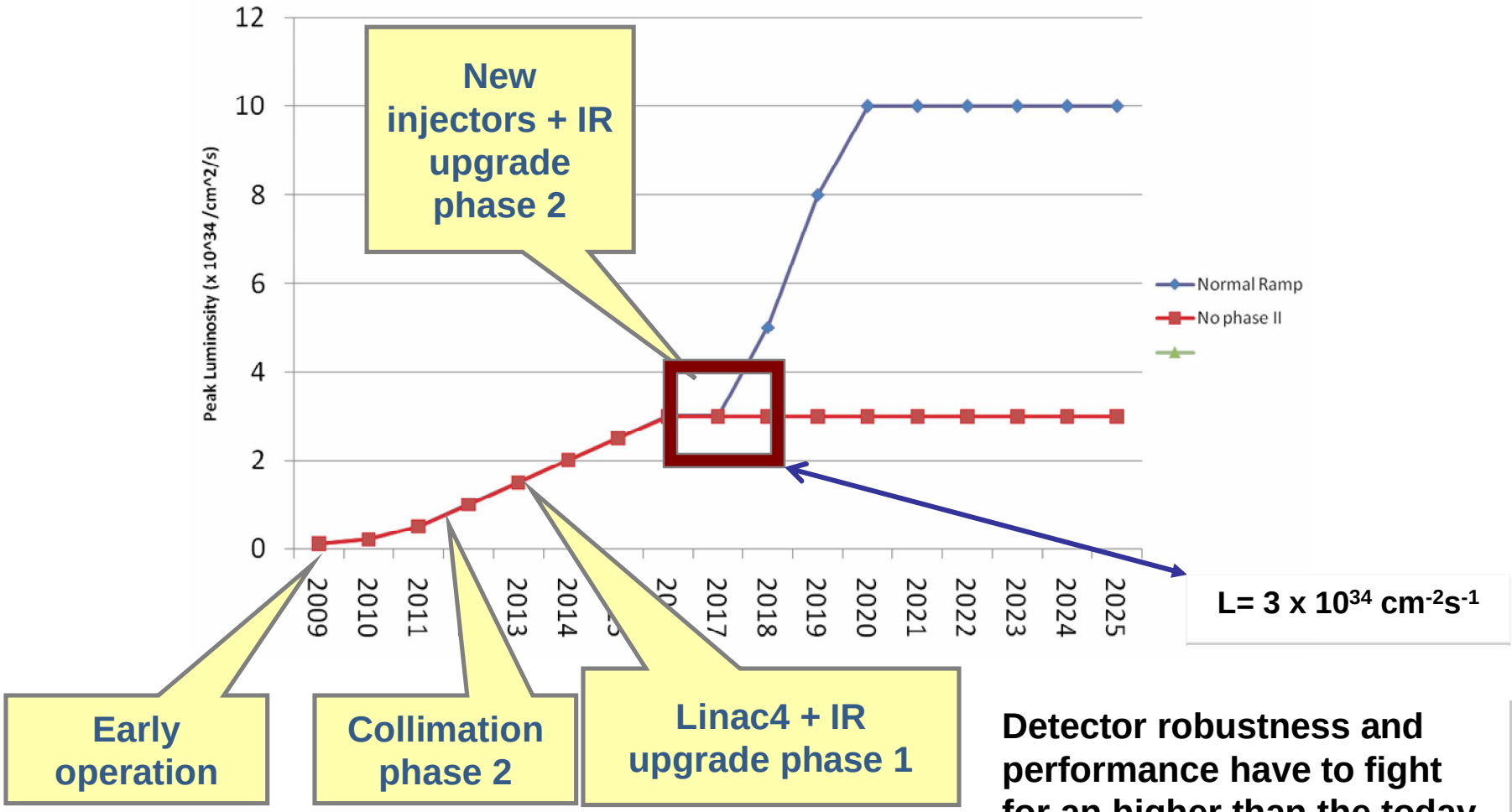
1) **Maintain at higher luminosity the same performance as the present ATLAS has at 10^{34} luminosity.**

2) **Allow collection of up to 6000 fb^{-1} of data with good performance. This is nearly 10 times the data expected between 2009 and 2016, allowing a large increase in physics reach.**

3) **The resulting design, to be presented, works well in the range of 10^{34} to 10^{35} luminosity. Design is based on all silicon sensors.**

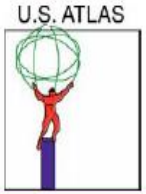
Abe Seiden UCSC Report to Joint Oversight Group (JOG) 11/08

LHCC: Peak Luminosity



Detector robustness and performance have to fight for an higher than the today BL design luminosity ($2x10^{34}$) at a smaller radius (3.7 cm instead 5.0 cm)

- Ref: LHCC 1/4/2008 – Roland Garoby
  - http://indico.cern.ch/conferenceDisplay.py?confId=36149



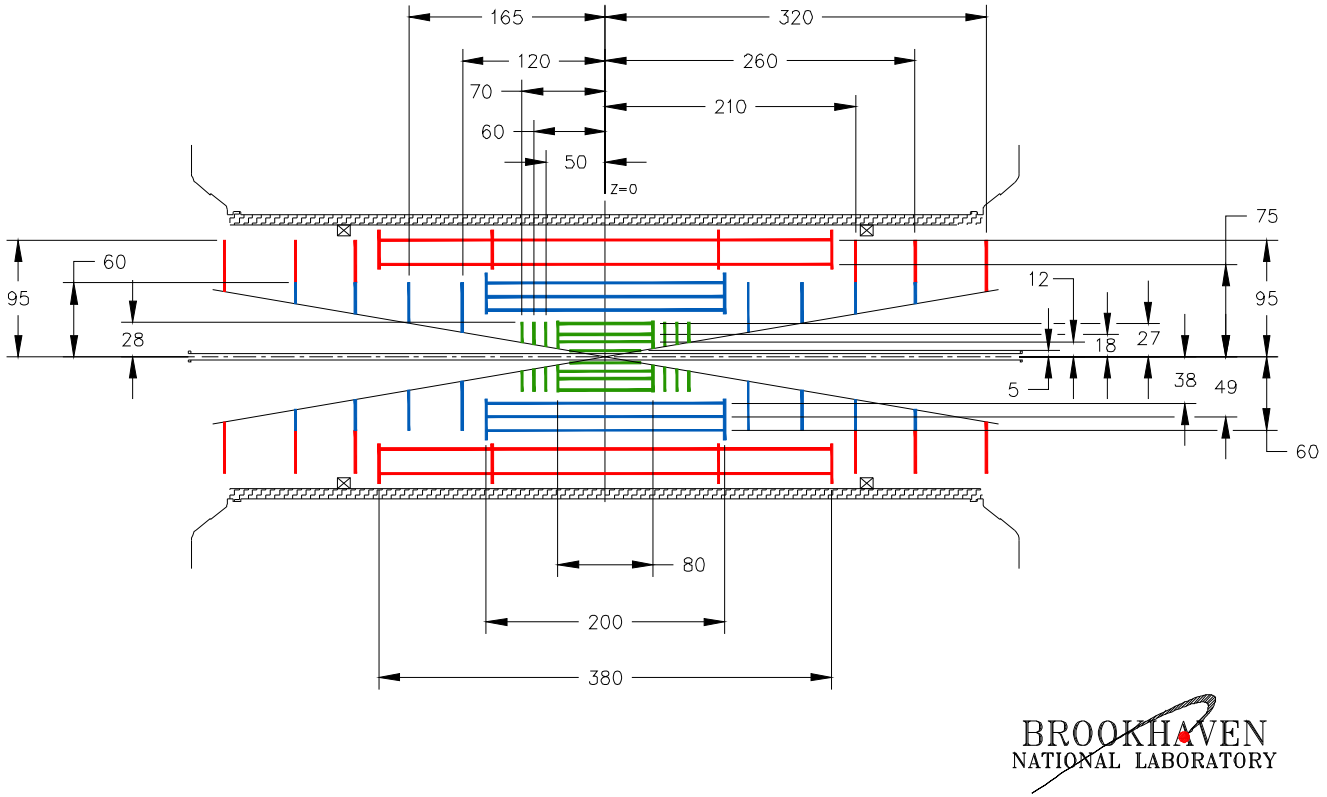
Items to Develop (R&D Program)

- Two types of pixel detectors:
  3-D detector for innermost layer (alternative diamond detector).
  n-on-p detector for 3 other layers (alternative is n-on-n detector).
- n-on-p short and long-strip detectors for the 5 strip layers.
- New front-end chips for these as well as associated controller and data collection chips. A major goal is to reduce power in the front-ends.
- New optical readout components (exploring several options for VCSELs and PIN diodes).
- New powering schemes (to power many modules per input power cable) to minimize mass in the detector and maintain safety for the chips.
- New mechanical scheme for holding individual sensors to reduce mass and complexity.
- New cooling system to improve on present detector (a possible choice is CO_2).

All items have been under development for the past few years and we plan to be ready for pre-production by June 2011.

Abe Seiden, UCSC JOG workshop 11/08

SLHC Draft Inner Detector Tracker Layout for Planning Purposes



New All Silicon Tracker replaces current pixel, SCT and TRT:

- pixels,
- short strips (2.5cm)
- long strips (10cm)

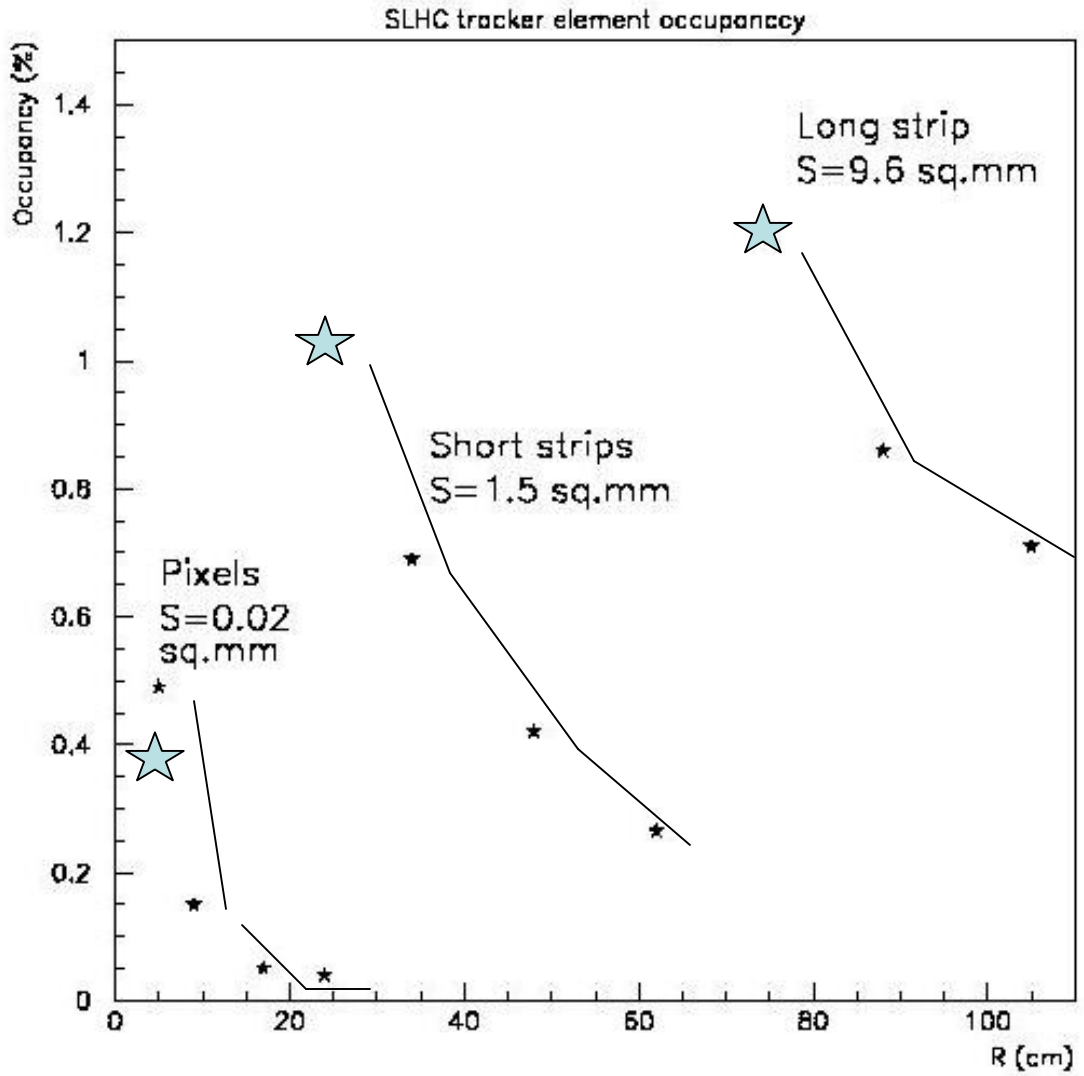
SLHC predicted occupancy

Old assumptions - 230 events/BX…

(New estimates~400)

Few comments:

- At 4-6 cm pixels layer should be <300μ
- At 24 cm even short strips are have > 1% occupancy
- At 71 cm long strips have occupancy > 1%



Pavel Nevski ***BNL***

SLHC Radiation Environment

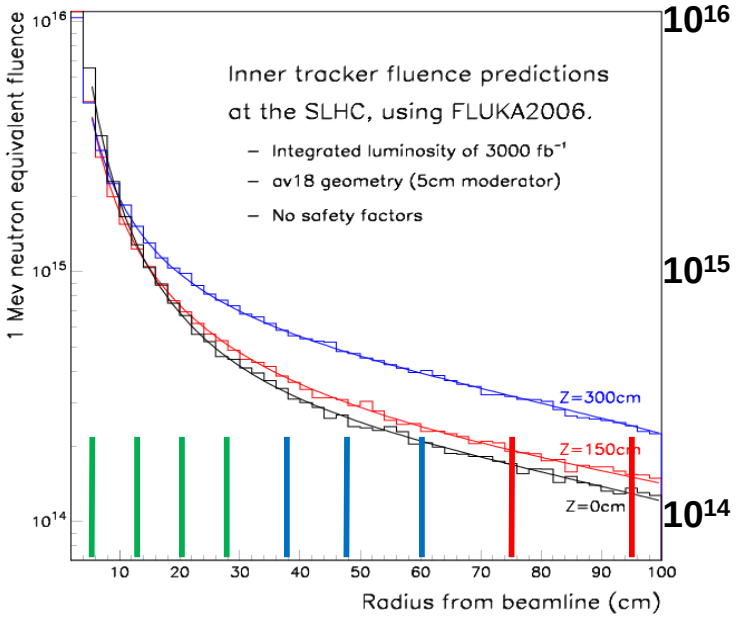
Radiation for 3000 fb^{-1}

Total Dose from Ionizing Particles

Radius in cm	Det.	Dose in kGy	
5.05	Pixel - 3d	15800	(158MRad)
12.25	Pixel	2540	
29.9	SCT SS	760	
51.4	SCT SS	450	
43.9	SCT SS	300	
108	SCT LS	70	(700KRad)

Neutron 1MeV Equivalent Dose

NIEL



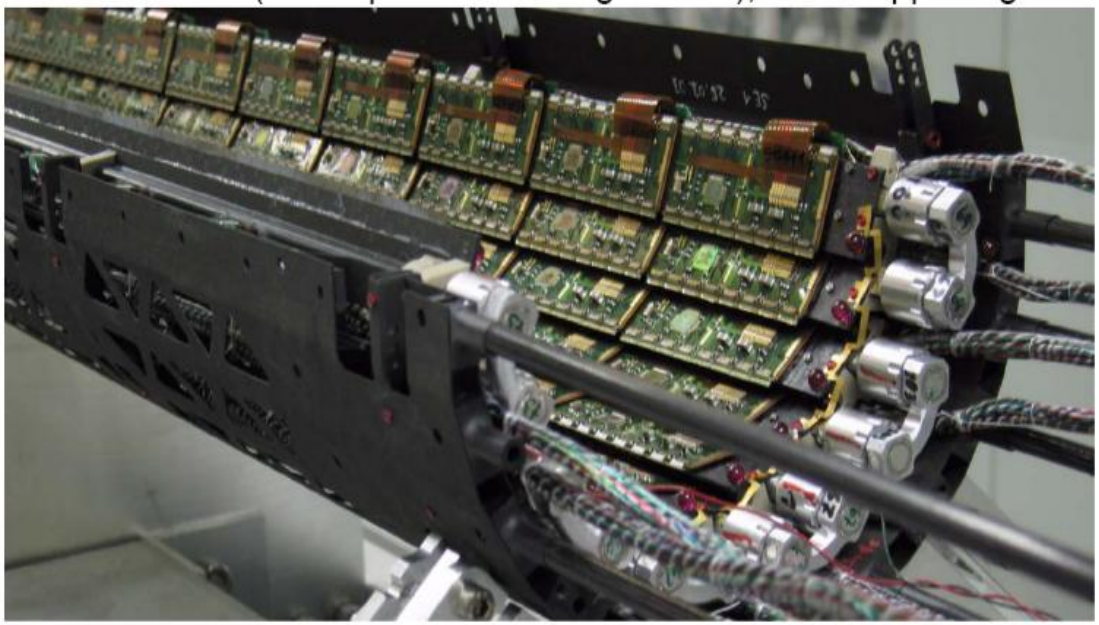
- Running up to 3000 fb^{-1}
  - Design for 6000 fb^{-1}
  - Should take about 6 years (?) à hadron rate for SEE
- Detector temperature ~-30^{o}C (minimize damage to Silicon)
- Magnetic Field ~2T

Philippe Farthaout TWEPP 2008

Present ATLAS Pixel B-Layer

Innermost layer of the ATLAS Pixel Detector:

- Historically called B-layer. Sensor radius is 50mm, and layer consists of 22 carbon-carbon staves (11 evaporative cooling circuits), each supporting 13 modules:



- Total of 286 modules (16%) with 20 degree tilt angle, 13.2M channels, active area roughly 0.29 m^2, worst-case end-of-lifetime power load as high as 2.4kW.
- Features: two data fibers/module at 80Mbit/s each, all cooling connections on C-side (historical), operation to 10^{34} luminosity with 99% single hit efficiency.
- Staves are mounted inside carbon-fiber half-shells, which clamp to form the layer.

■

Pixel B-Layer Replacement, May 3, 2007

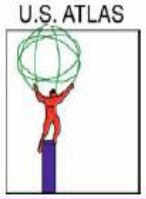
B-Layer Replacement Concept:

Justification: 300 fb^{-1} expected Life time

- With nominal luminosity profile, expect B-layer performance to start degrading after 2-3 years at LHC design luminosity or about 300 fb^{-1} (10^{15} NIEL dose, 50MRad ionizing dose). Expect reduced efficiency and modest reduction in point resolution.
- The performance of the B-Layer has a large impact on ATLAS physics performance, particularly for B-tagging. On the timescale of next several years, expect that improvements in technology should allow construction of a B-Layer with improved segmentation, greater radiation hardness, and reduced material.
- Propose to prepare an upgraded B-Layer for installation during the Winter 2012/ 2013 shutdown, after roughly 4 full years of ATLAS operation.

Principal goals are:

- **Reduction of material**, required to take full advantage of point resolution. This could use a combination of improved power distribution (reduced electrical services) and improved active fraction for the basic modules (closer to 90% rather than the present 71%). Present best estimate for pixel layer now is 2.5% X_0 per layer. Would like to target between 1.5% X_0 and 2.0% X_0 per layer.
- **Improvement of segmentation**, useful to cope with higher occupancy and provide improved point resolution in one or both measurement coordinates. Ideally, would like to reduce pixel area by a factor 2-3. What is the optimal aspect ratio ?
- **Increased radiation tolerance**, both for higher instantaneous luminosity and for higher total dose tolerance. Set nominal goal of a factor 3 increase, leading to instantaneous rate of $1x10^8$ $cm^{-2}s^{-1}$, and a total dose of $3x10^{15}$ neutron equivalent. This is an intermediate step to SLHC, and would be consistent with operation at 30mm radius and the present LHC design luminosity up to SLHC (2016) period.



Projected U.S. Activities and Deliverables

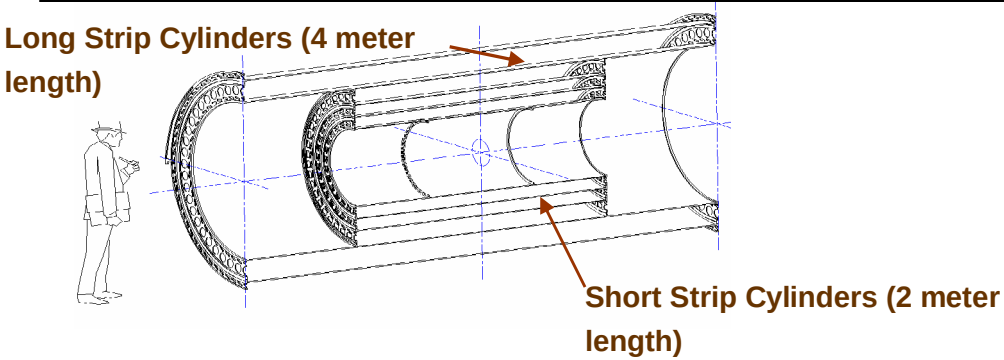
Silicon Strips

- Leading role in the definition and implementation of the overall electronics architecture, including design contributions to specific elements. The definition of the overall electronics architecture (for strips and pixels) is currently being co-led by the U.S. (UCSC, Penn)
- Contribution to the procurement of front-end integrated circuits and local control integrated circuits. Testing of integrated circuits. This follows naturally from the role in defining the overall electronics architecture. (UCSC, Penn)
- Common design of powering and data transmission with the pixel detector, fabrication and test of unique elements of these systems. (UCSC, Ohio State, Oklahoma, Oklahoma State, SMU, SLAC)
- Development of planar sensors (in common in part with pixels), contribution to procurement costs and testing as part of a module assembly program in the U.S. (UCSC, BNL, Stony Brook, NYU, LBNL)
- Fabrication of a fraction of the local supports for silicon strip modules. The U.S. is currently leading the conceptual design of the preferred technique for holding, locating and cooling strip modules. Design and contribution to the global support structures. (Yale, BNL, LBNL)
- Mounting and testing of modules on local supports. It is essential that integrated structures be assembled world-wide and shipped to a central point (likely CERN) for final rapid integration into support structures to meet schedule constraints. (Yale, BNL, Stony Brook, NYU)
- Contributions to integration and installation at CERN. (BNL)

Abe Seiden, UCSC JOG 11/08

Strips Detector in numbers

	Layer	Type	Radius [cm]	Phi segmentation	Number of modules per half single sided stave	Number of 128-ch FEIC per half single sided stave
Barrel	0	Short Strips	38	28	10	400
	1	Short Strips	49	36	10	400
	2	Short Strips	60	44	10	400
	3	Long Strips	75	56	19	190
	4	Long Strips	95	72	19	190
	Total number of staves for the Barrel					*236*
	Total number of modules for the Barrel					*14,336*
	Total number of FEIC for the Barrel					*270,080*
Endcap	*Total number of staves for one End-cap*					*1,152*
	Total number of 128-ch FEIC for the two End-cap					*57,088*
Total number of 128-channel FEICs						**327,168**
Total amount of channels						**41,877,504**



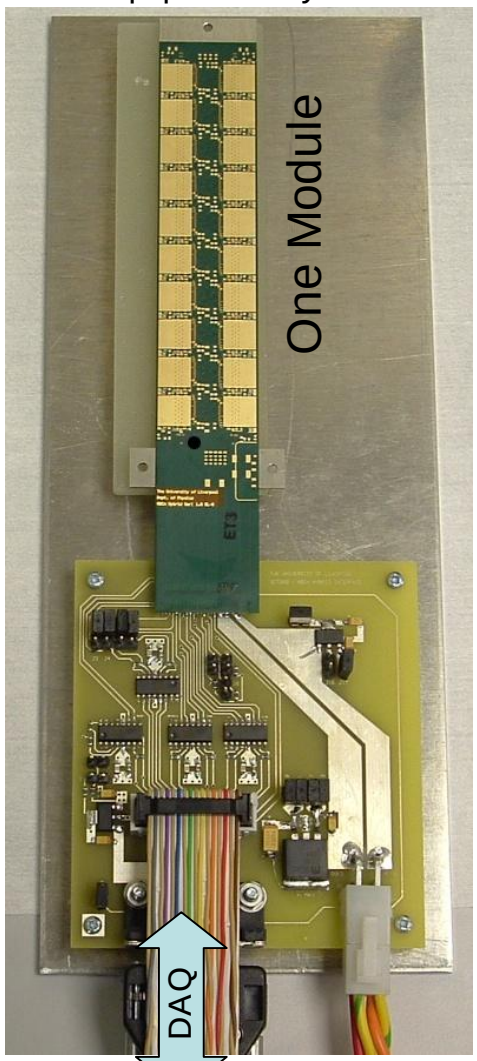
- *Current SCT detector*
  - *4088 modules*
  - *49k 128-channel FEIC*
  - *6.3M channels*

Philippe Farthouat (CERN)

Prototype Hybrid Realisation

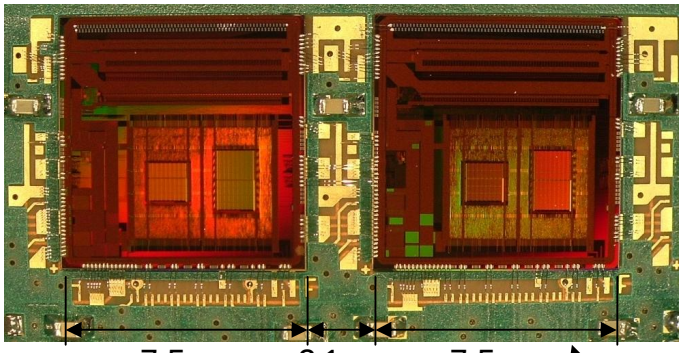
November 2008

Unpopulated hybrid

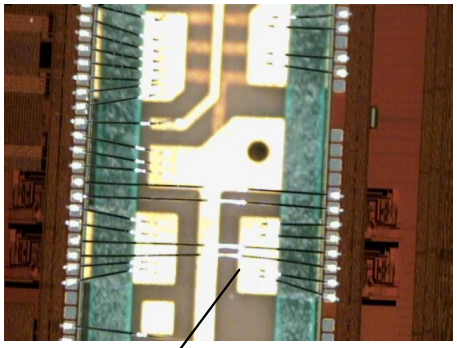


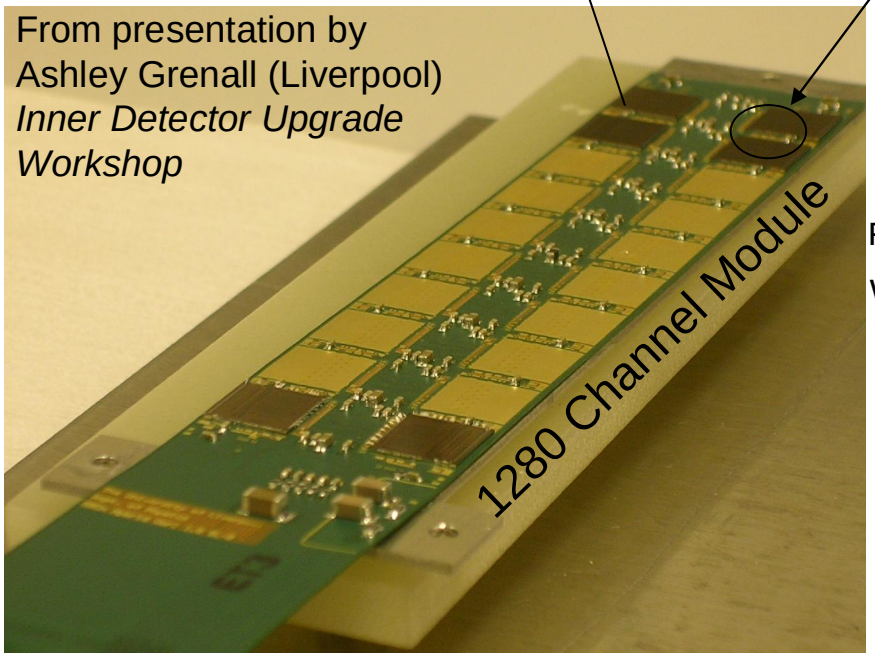
LVDS Repeater & Hybrid Power Card

Neighbouring ABCns wire bonded



Inter-chip bonding





Flex thickness ~270µm

Weight ≤2g (unpopulated)

Hybrid Stuffed with Passives and 6 x ABCns

First Generation Hybrid & ABCn first tests

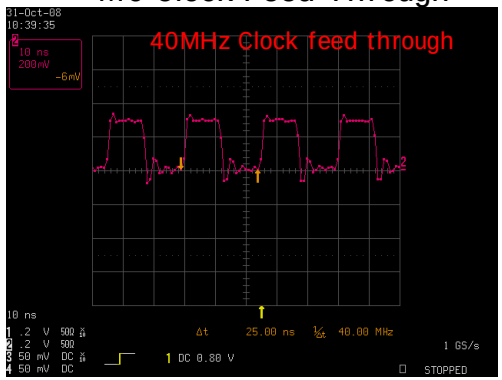
What we presently know

- Hybrid connectivity confirmed to be ok
- Able to read back correctly thermistor temperature

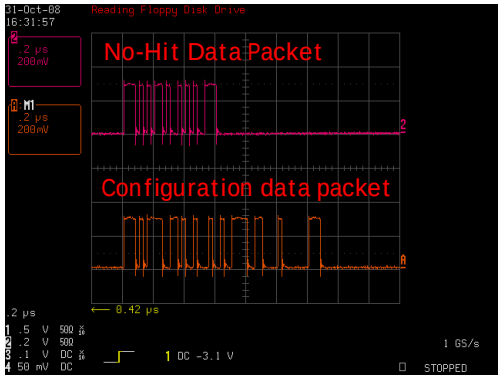
- Wire bonded up single ABCn as a Master (M0), operating in Legacy mode
- Disabled on-board Regulator + Shunt circuits (use external powering/regulation)
  - VDDD = 2.5 I = 110mA, VDDA = 2.2V I = 30mA (with clock supplied)
  - Specification is for a nominal of 96mA and 27mA!

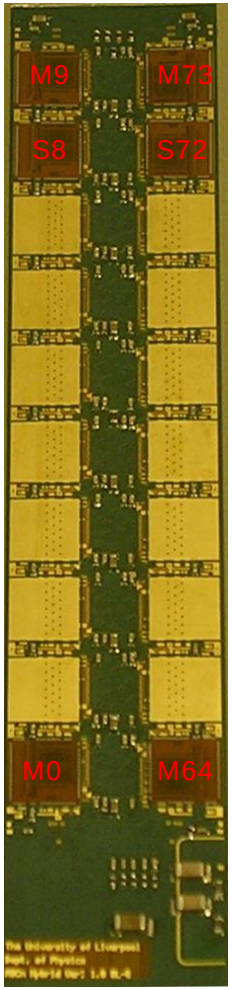
- Clock feed through is enabled, default state for Masters on power-up
  - 40MHz clock is observed on Ldo outputs
- Send command to disable Clock feed through – 40MHz clock goes away
  - Chip is responding to commands!
- Send L1 trigger (toggle ABCn between data taking mode and Send_ID mode)
  - Observe No_Hit data packet and ABCn configuration data packet
  - ABCn responds to L1 triggers!

M0 Clock Feed Through

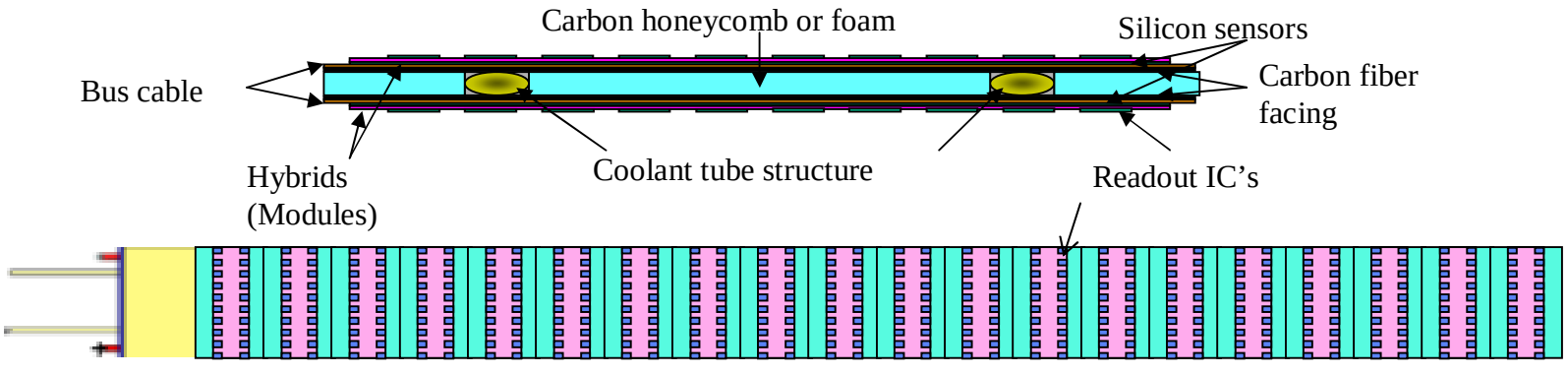


M73 response to L1 trigger





SCT Barrel Stave



24X128X12 per side

A conceptual drawing of an SCT barrel stave. Details of powering, cabling control, monitoring and data collection are in early conceptual stages.

Prototypes and Designs

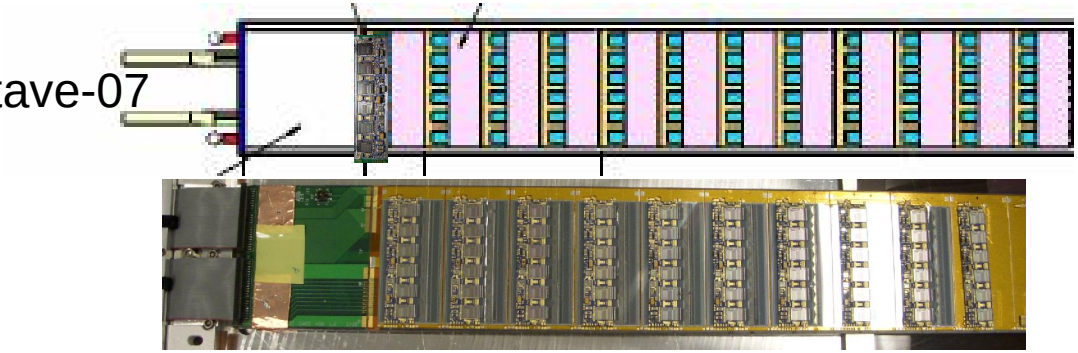
LBL

60 cm, 9 cm strip, 6 segments/side

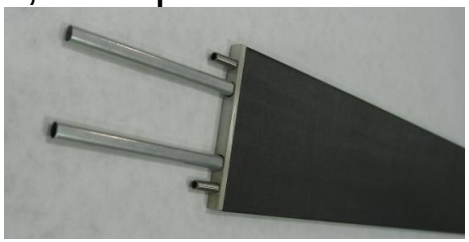
Stave-06

1 meter, 3 cm strip, 30 segments/side
192 Watts (ABCD chip), ~2.4 % Xo + support structure

Stave-07

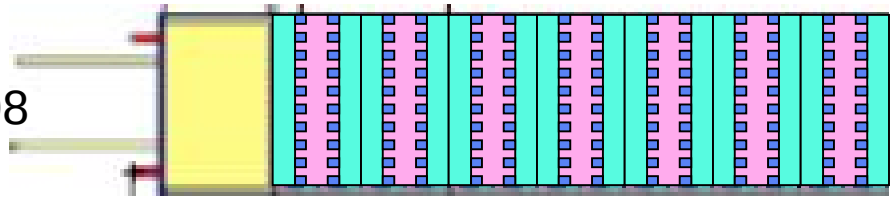


6 x 3 cm, 6 chips wide



1.2 meter, 2.5 cm strip, 48 segments/side ~250-300 Watts (@0.25 W/chip)
1.7 – 2.4 % Xo + support structure, depends upon coolant and hybrid design

Stave-08

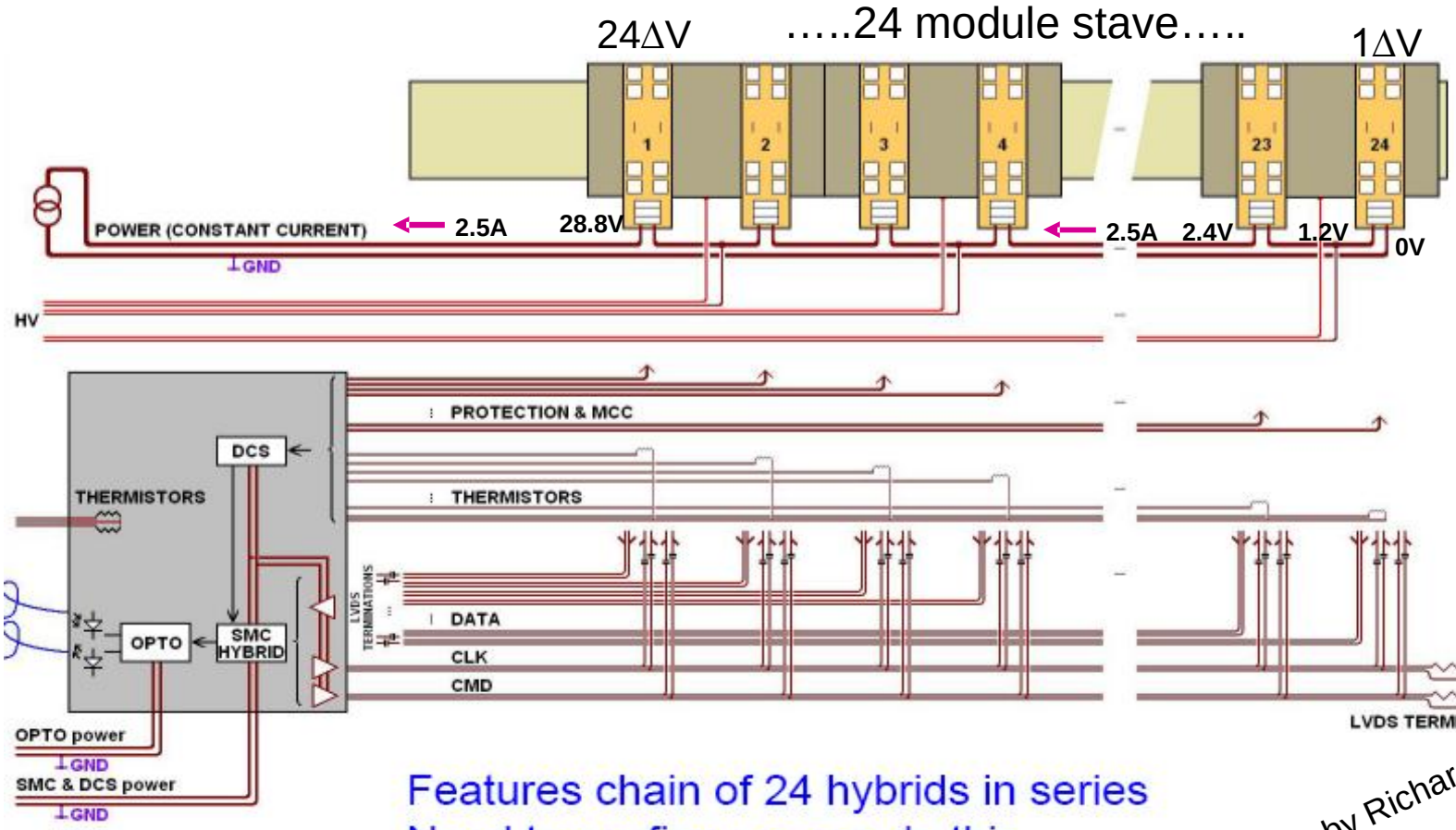


10 x 10 cm, 10 chips wide

Carl Haber LBL

Serial powering of Staves

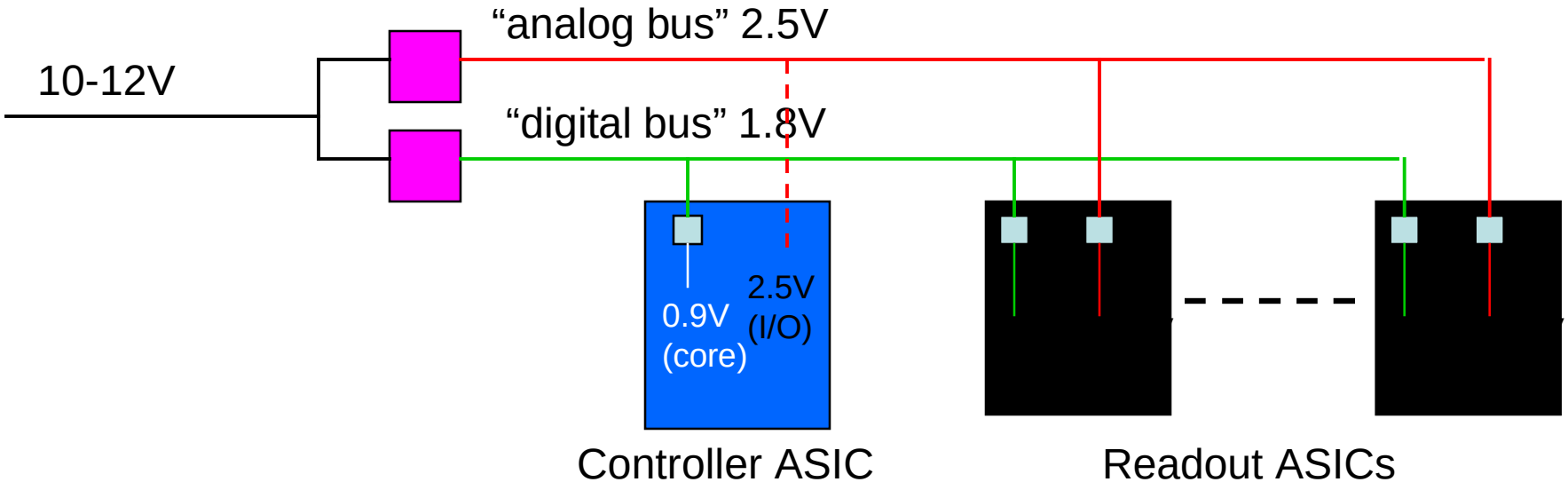
By powering each module in series a cable sized for a single module (2.5A). Can be used to minimize the material in the interaction area.



Drawing by Richard Holt (RAL)

DC to DC power distribution scheme

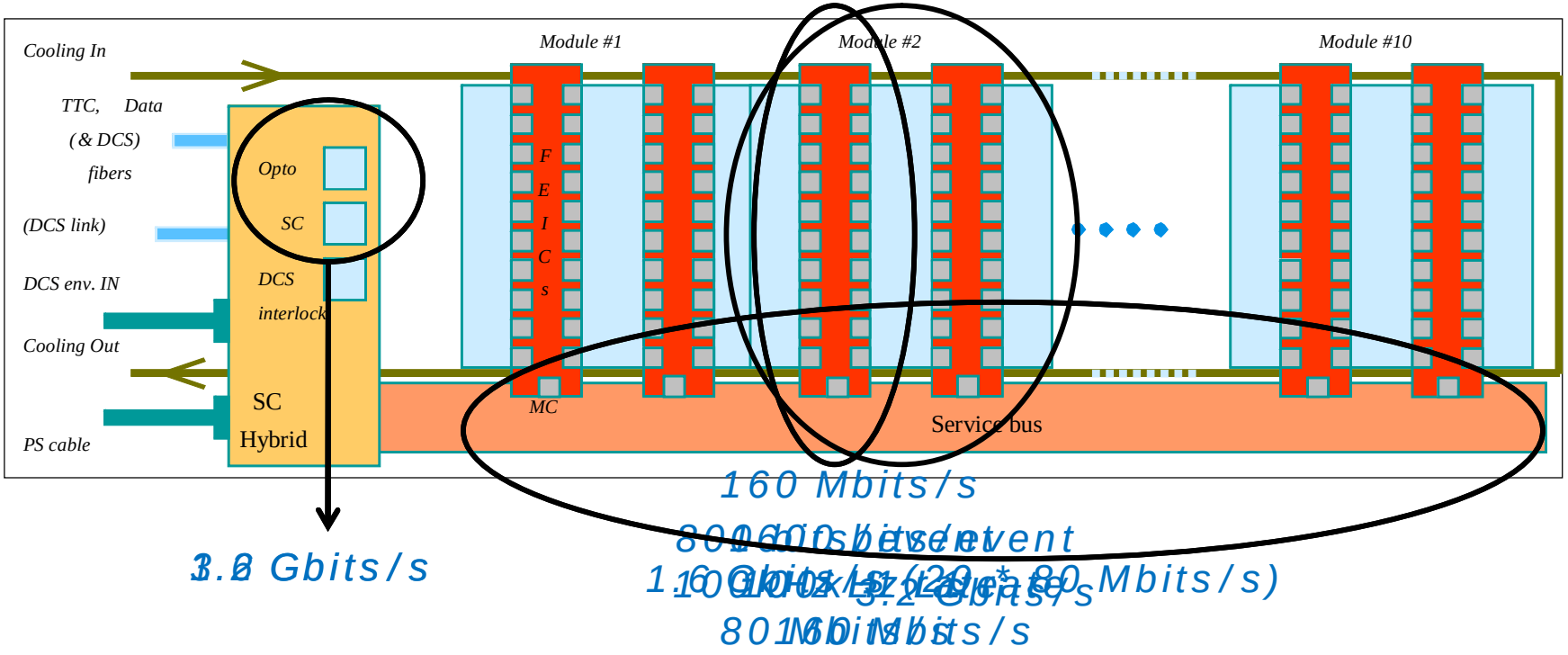
With Efficient DC-DC conversion schemes, voltage and current can be traded off
To lower power cable material required to supply detector mounted ASIC voltages.



Conversion stage 1 (ratio 4-5.5)
-Vin=10V => high-V technology
-Same ASIC development for analog and digital, only feedback resistive bridge is different

Conversion stage 2 (ratio 2)
- Embedded in controller or readout ASIC
- Closely same converter for analog and digital (different current, hence different size of switching transistors): macros (IP blocks) in same technology

Module Data Rates



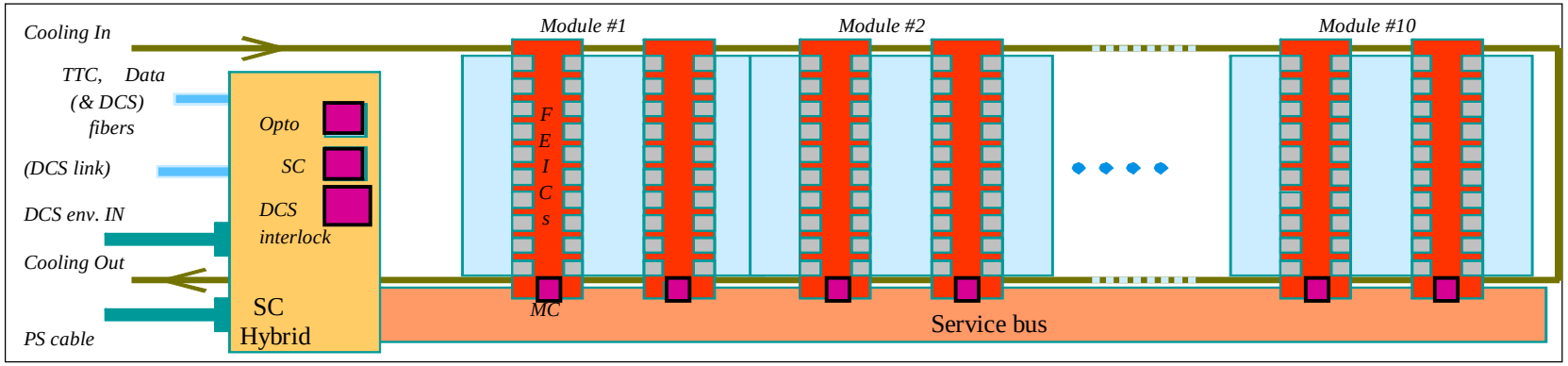
- Long strips and short strips are well balanced
  - 400 versus 380 FEIC
- Numbers without so much safety margin
  - Detector layout very likely to change
  - L1A rate could increase
  - Luminosity could increase
  - Data format might change
- Pixel will require more bandwidth
- Better design for more → x2

Philippe Farthouat (CERN)

Architecture

Although the data rates, radiation levels and first front end readouts have been identified, the overall architecture is not defined.

A ***strip readOut working group*** has been formed and meets regularly to define an architecture that will enable designs to proceed.



Yet to be designed

Module Control ASIC
Optical Link
Stave Control ASIC
Optical DATA Link

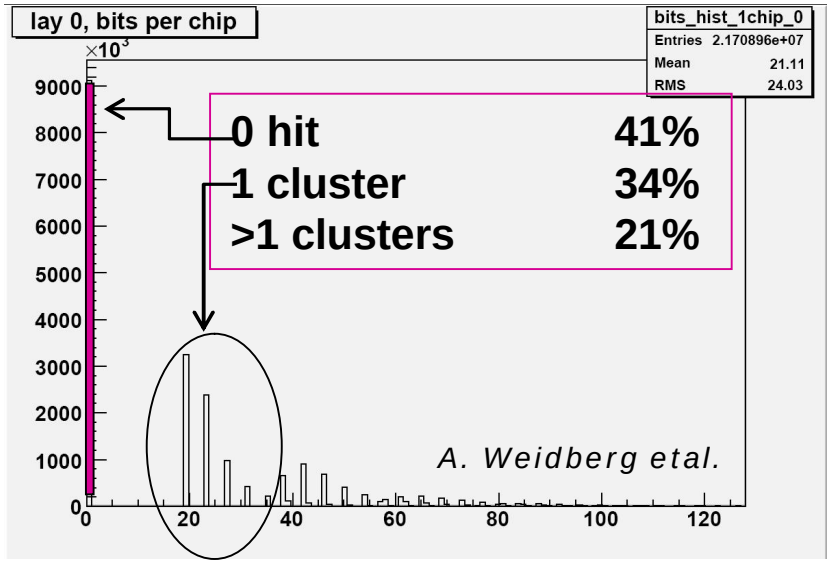
Tradeoffs / Resources:

- Number and type of ASICs
- Command complexity vs hybrid real estate
- Redundancy vs hybrid real estate
- Data transfer protocol
- Data recovery techniques

Short Strip DATA Rate at SLHC

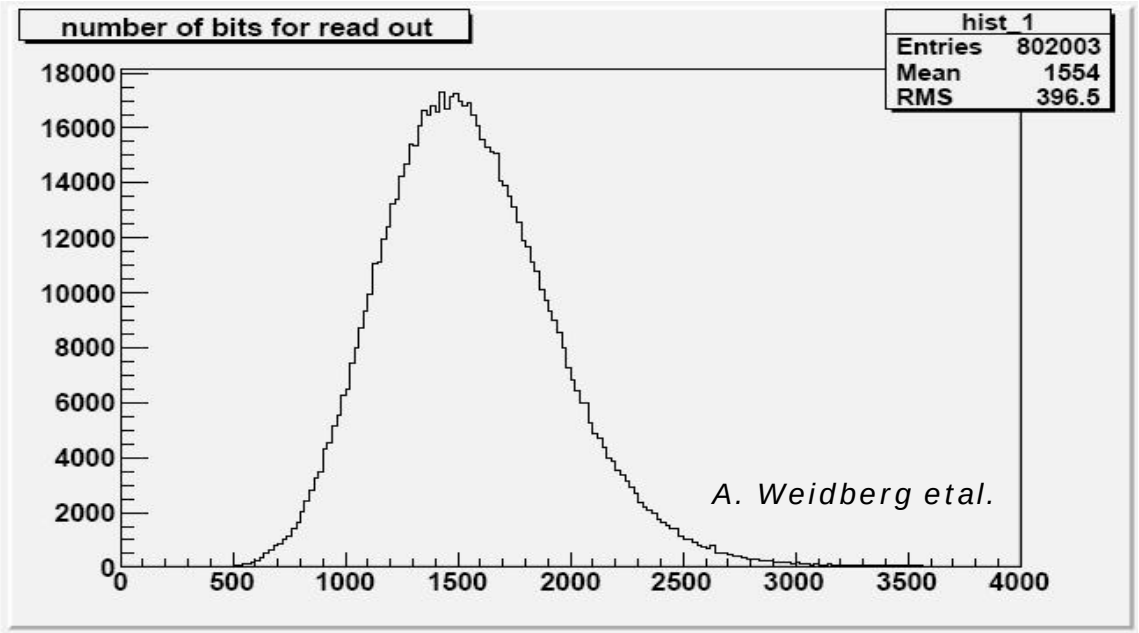
Simulation for worst case scenario:
10^{35} cm^{-2} luminosity
50 ns BC period (400 overlapping events per BC)
Short Strips

Number of hits per FEIC



Event size for a short strips module (40 128-channel FEICs). Current ATLAS SCT detector coding scheme

Mean size ~1600 bits



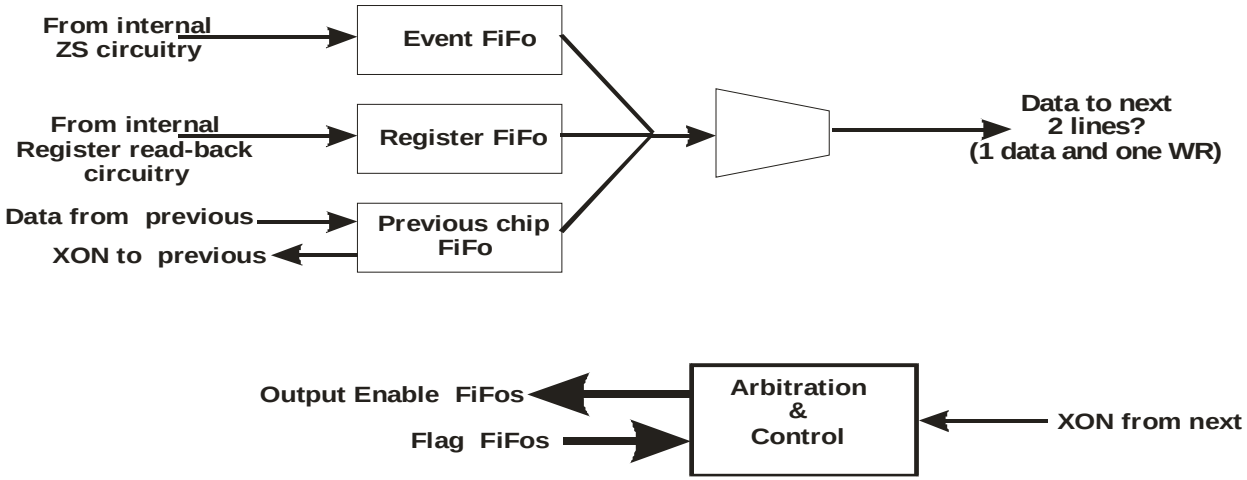
Fixed Length Data Transmission

Fixed size packet for one non-empty ABCn	#bits	
Start	0	No need
Chip ID	5	Readout hybrid contains at most 20 chips
Data type	3	Data, register readback, DCS, Test mode, …Not more than 8 types
Sub-header	12	Register address, DCS sub-type, etc and header for data. In the later, must contain BCID (8 to 12 bits) and L1ID (4 to 8 bits). Max length 12 - 20 bits
CRC	7	7 bits for protecting ChipID, Data type and sub-header (1 error recovery, 2 errors detection)
Pay load	28	Must be large enough so that most of events can totally fit in that space. If not, a second packet must be sent which has a large overhead. Simulations show a 21-hit average for 10 ABCn. Size of two isolated hits is 28 bits. Size for three is 42 bits
Stop	0	No need
Total	55	

Many events with ‘0’ occupancy / ASIC see previous slide

à Only ASICS with data transmit.

One possible scheme

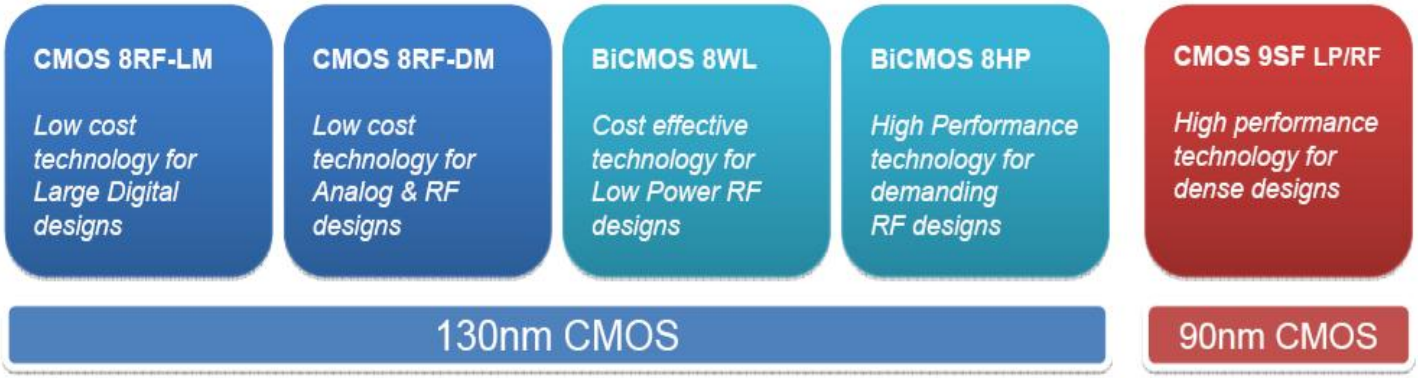


- The control of the transmission is very simple as the data are not analysed
  - Only number of bits transmitted is controlled
  - Packets from different events can be interleaved
- Note that we are not forced to have the data passing through all the chips; they could share a single bus FEICs à MC and only some arbitration mechanism is to be implemented
- Size of the Fifos optimised for keeping the level of data loss at the expected value

ASIC Technologies for the Upgrade

- What technology is most appropriate for a next generation detector.
  - Will it be available in 2014?
  - Will it offer acceptable low power operation?
  - Will it be affordable?

Overview of Technologies



- 130 (CMOS and BiCMOS) and 90 nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

CMOS8 RF Technology Tool Kit

Standard Features

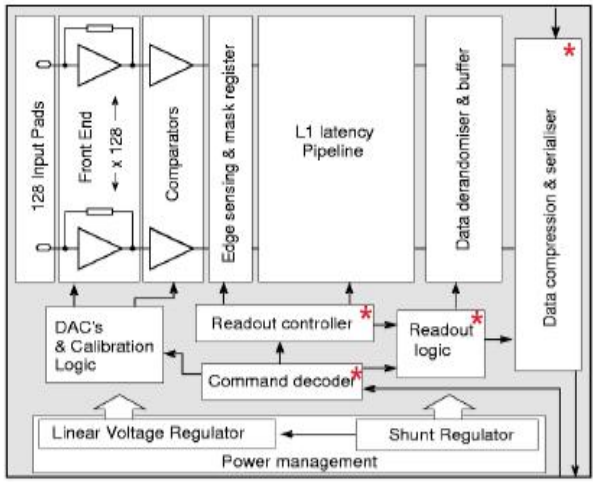
- **130 nm lithography, twin-well on 1-2 Ω-cm non-epi P- substrate, low K dielectric**
- **Thin Oxide (22Å gate) FETs (1.2 /1.5V)**
- **Thin Oxide MOS Varactors**
- **Forward bias diodes**
- **N-well resistor**
- **5 to 8 levels of metal**
  - Thin and thick Cu metal (~0.3/0.55 μm)
  - Last metal options:
    LM: Cu 0.55μm DM: 3 μm Cu + 4 μm Al
- **Vertical Natural Capacitor**
- **Spiral inductors, RF Transmission lines**
  - Series & Symmetrical inductors in DM wiring option only
- **Electrically programmable fuses**
- **Wire bond or solder bump (C4) terminals**

Optional Features

- **Triple-well NFETs**
- **Thin Oxide Low power FETS**
- **Thin Oxide Low-Vt FETs**
- **Thick Oxide (52Å) 2.5V FETS**
- **Thick Oxide (52Å) 3.3V FETS**
- **Thin and thick Oxide Zero-Vt NFETs**
- **Thick Oxide MOS Varactors**
- **Hyperabrupt Varactor**
- **Polysilicon and diffused resistors**
- **TaN metal resistor**
- **Single and dual-layer MIM capacitor (DM option only)**

Comparison of 250nm and 130nm Technologies

ABCN architecture in ¼ µm CMOS



250nm ABCn

128 Channels / chip 20 ABCn / Module	VDD @ 2.5V VDDA @ 2.2V	Current / chip	Power / chip	Power / module
Analogue Supply	VDDA	27 mA	60 mW	1.2 W
Digital Supply*	VDD	92 mA	230 mW	4.6 W
			Total	**290mW**

* SEU Tolerant Logic

Estimate for130nm CMOS version

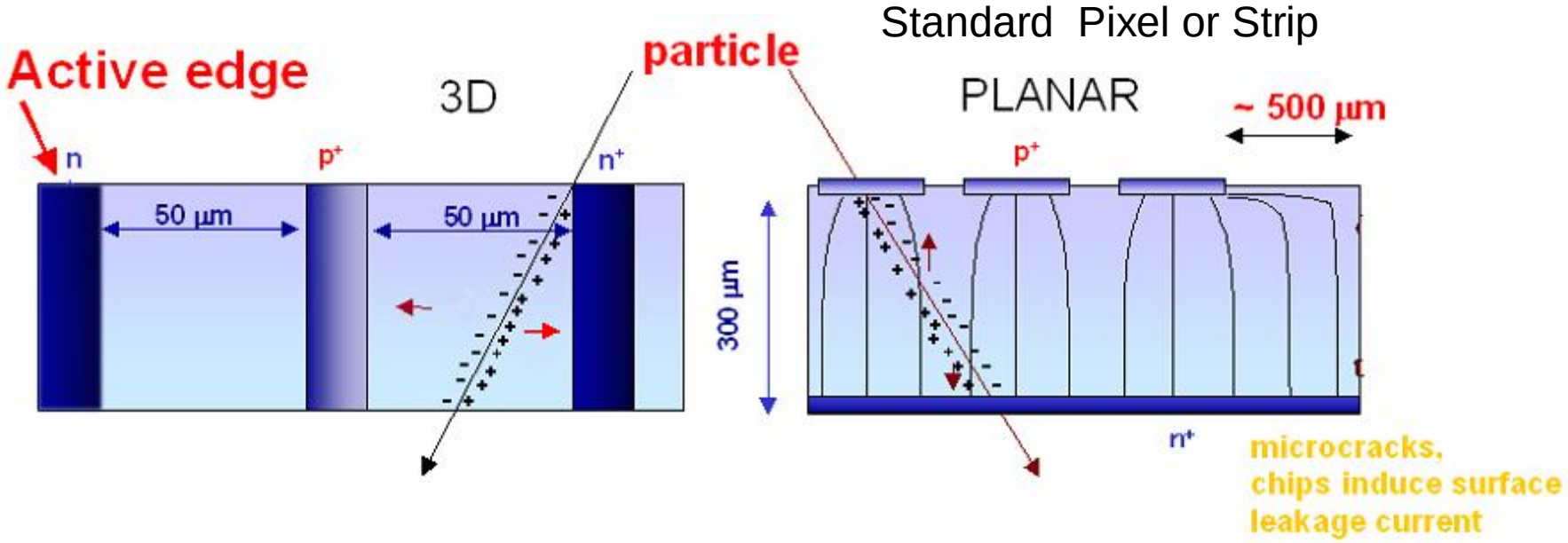
130 nm Estimate 128 Channels / chip	Supply	Short Strip Power, Current	Long Strip Power, current
Analog	VDDA @ 1.2V	20 mW, 16mA	39 mW, 32mA
Digital Supply	VDD @ 0.9V	46 mW, 51mA	46 mW, 51mA
Total Power* / Chip		66 mW	85 mW
Total Power * / 20 Chip Module		1.3 W	1.7 W

Novel Tracker Technologies

- 3D -- Pixels for the inner detector
- InGrid for a Non Silicon TRT

3D Silicon Tracking

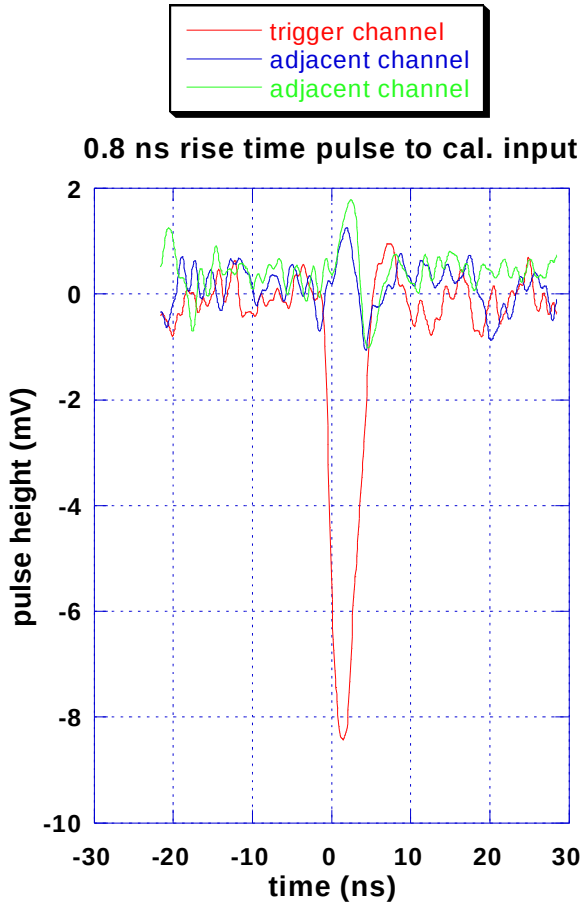
US Initiative -
Sherwood Parker – Hawaii, SLAC
S. Seidel - New Mexico
Kevin Einsweiler, Maurice Garcia-Sciveres (LBL)



3-D Silicon Tracking

- Low depletion fields
  Breakdown less likely
- Short Drift (50um)
  fast signals

Technology complex and still in development in the US and Europe.



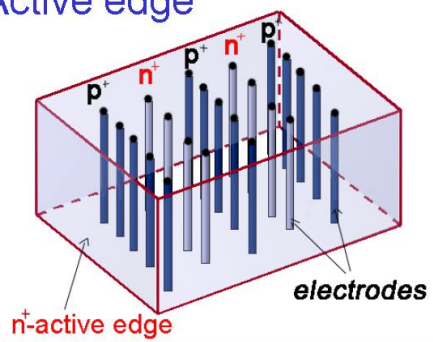
3d Pixel Sensor for the Inner tracking layers

Introduction

The 3D sensor's family

Cinzia Da Via', Manchester- B-Layer Replacement Workshop CERN 28-09-07

Full 3D
Active edge



3DC Fabricated at Stanford and tested with Atlas pixel Readout – and SLHC fluences Design at its 5th Generation

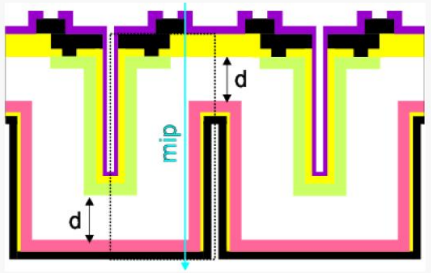
data of this talk

Being also fabricated at SINTEF in the ATLAS Upgrade framework as Part of the 3DC Consortium.
No data available yet

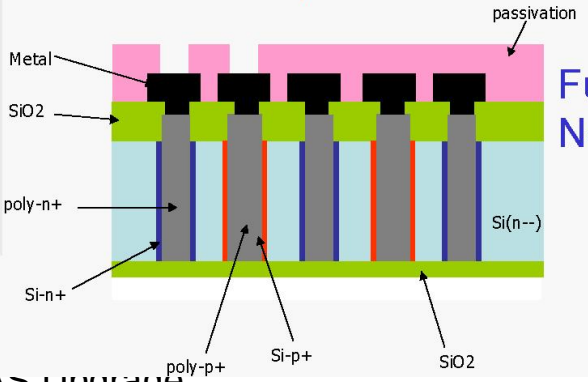
Genova

IRST and separately CNM. Being presently fabricated
no data available yet

Double column
No active edge



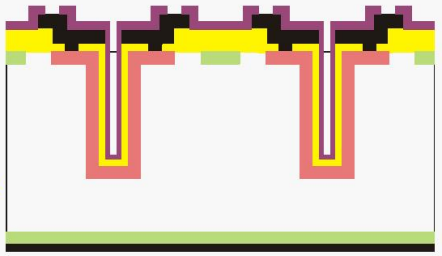
ICEMos- Being presently fabricated
Work performed in the RD50 framework
no data available yet



Full 3D
No active edge

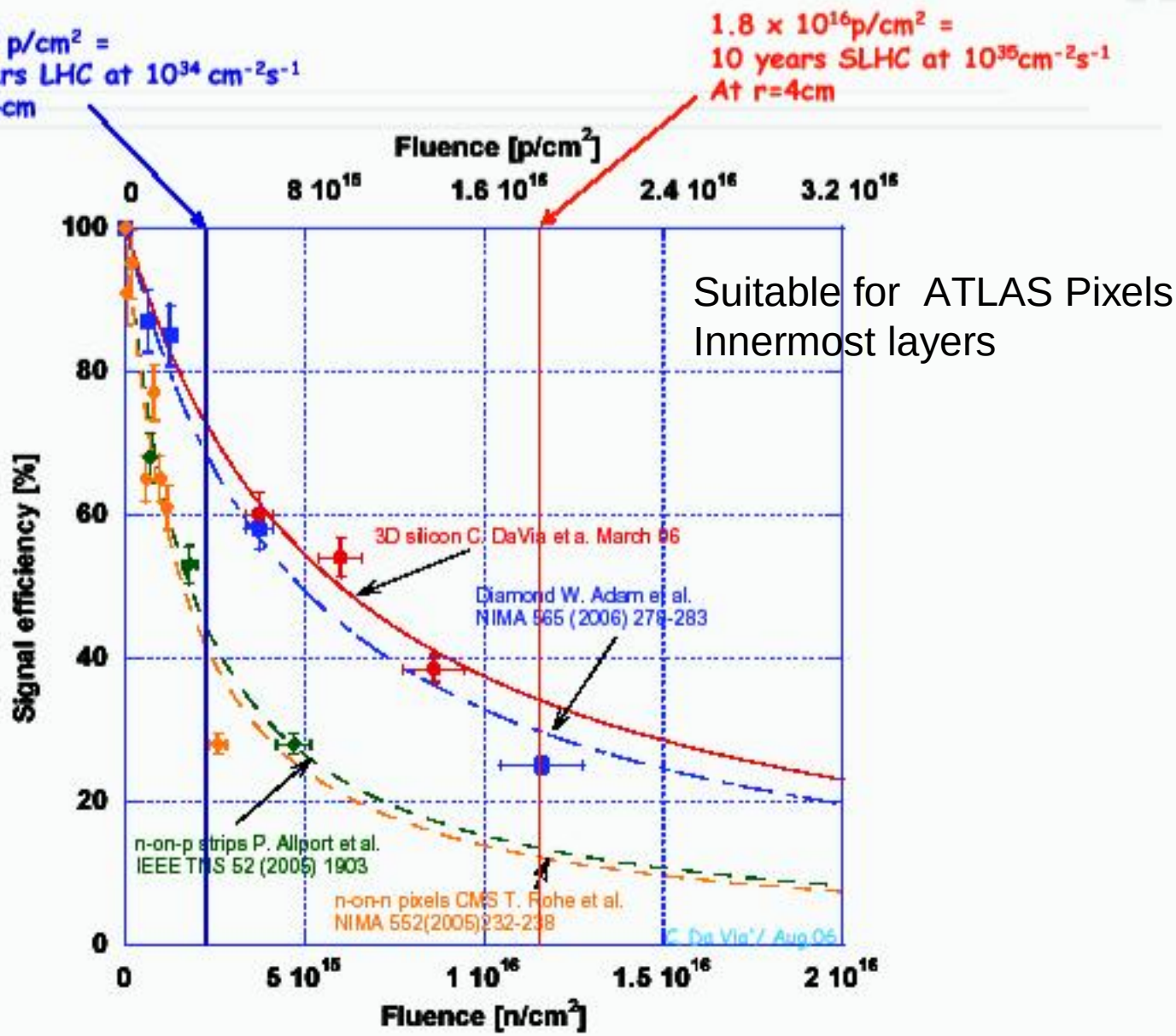
IRST/CNM fabricated in the RD50 Framework in 2005 Tested with SCTA readout Electronics. Data and Simulations show that the design is NOT radiation hard For B-layer replacement.

Single column
No active edge



Radiation Hardness

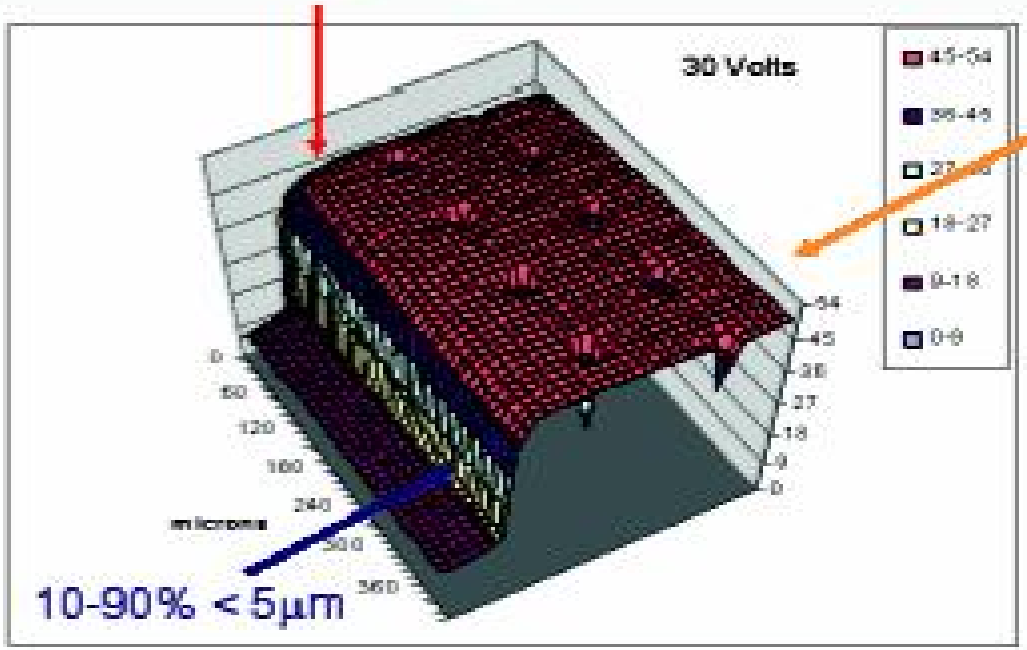
Silicon 3D Tracker

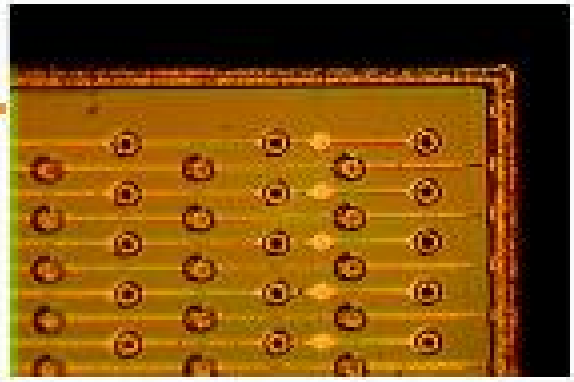


Suitable for ATLAS Pixels
Innermost layers

Sherwood Parker - Invited Talk NSS 2006

3D edge sensitivity using 13 keV X-rays at ALS-Berkeley





Measurement Performed using a 2 μm beam

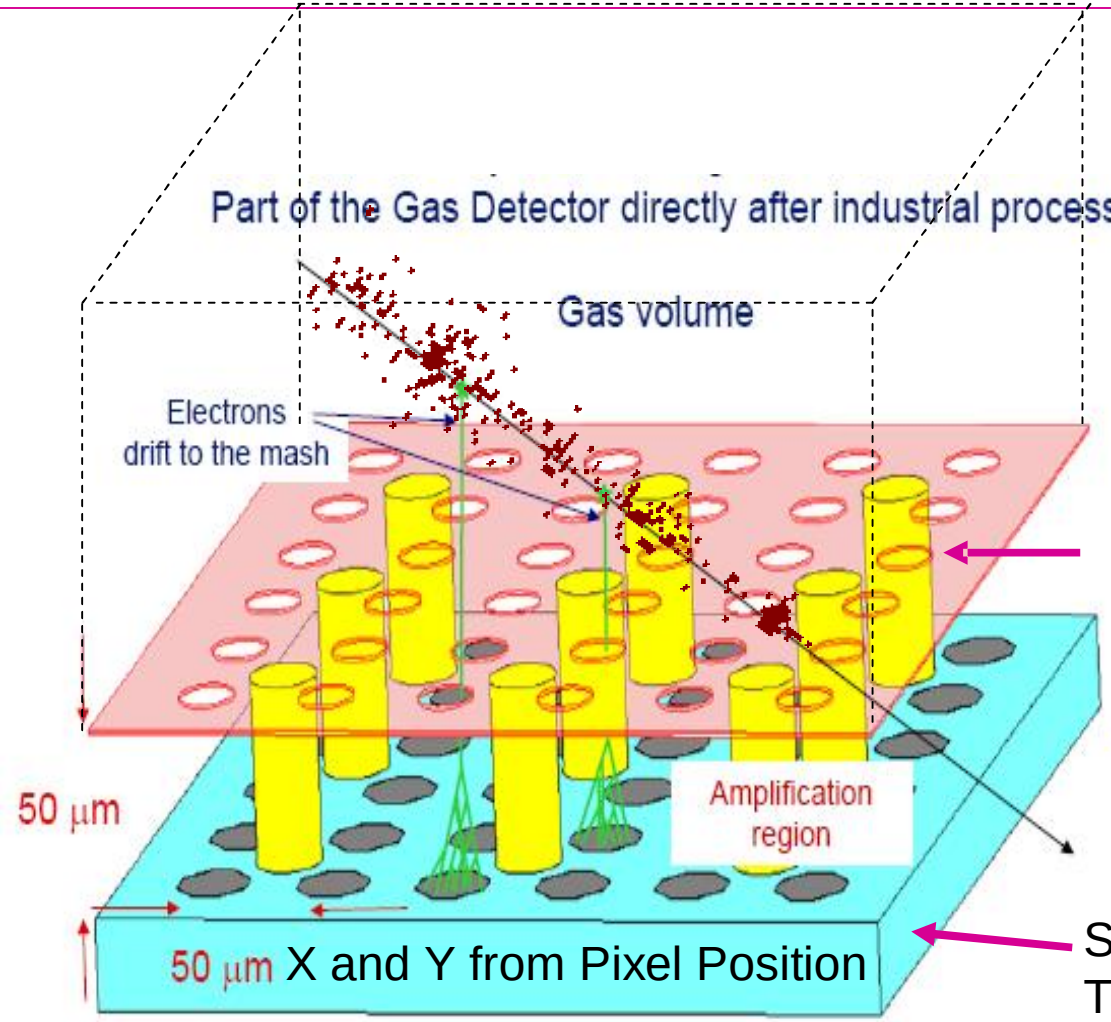
J. Hasi, C. Kenney, J. Morse, S. Parker

X-ray micro-beam scan, in 2 μm steps, of a 3D, n bulk and edges, 181 μm thick sensor. The left electrodes are p-type

Efficiency measured in test beam ~98%

Ingrid: Gas Filled Tracking for SLHC

One Gas filled Layer Provides all Track Coordinates



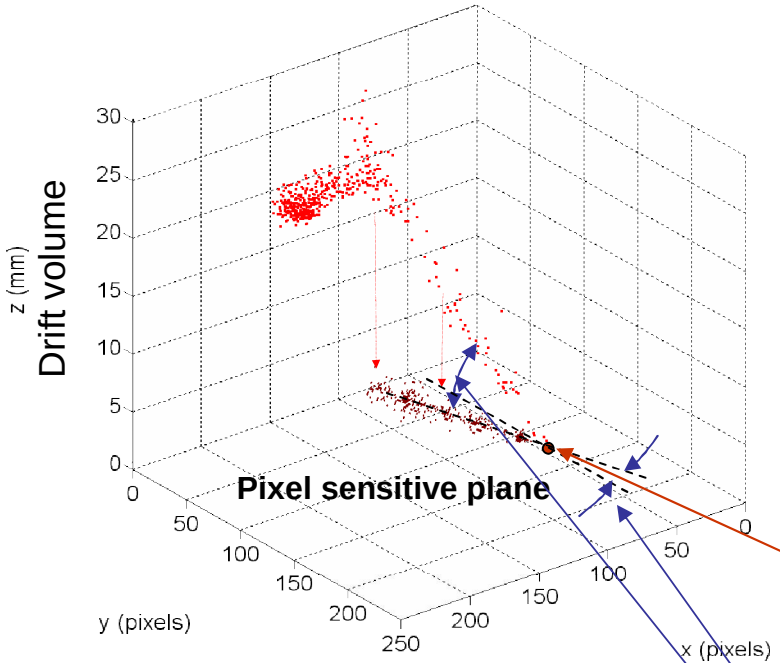
16 mm Ionization region

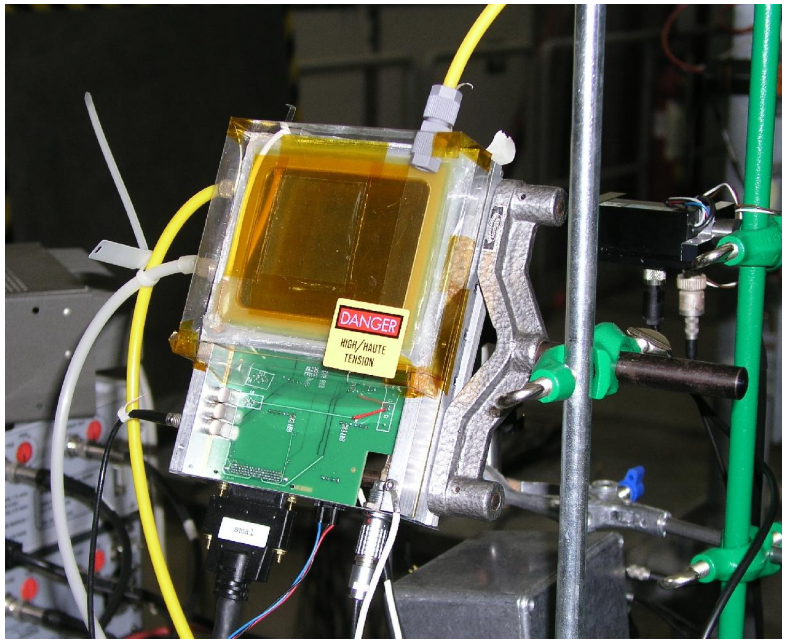
Post Processing Creates Grid Structure and mesh

Standard CMOS ASIC Technology with a Passivation Layer

Ingrid is essentially a High Rate mini - Time Projection Chamber

The tracking information it provides can be available within a few hundred ns making it suitable for Level 1 Trigger input.





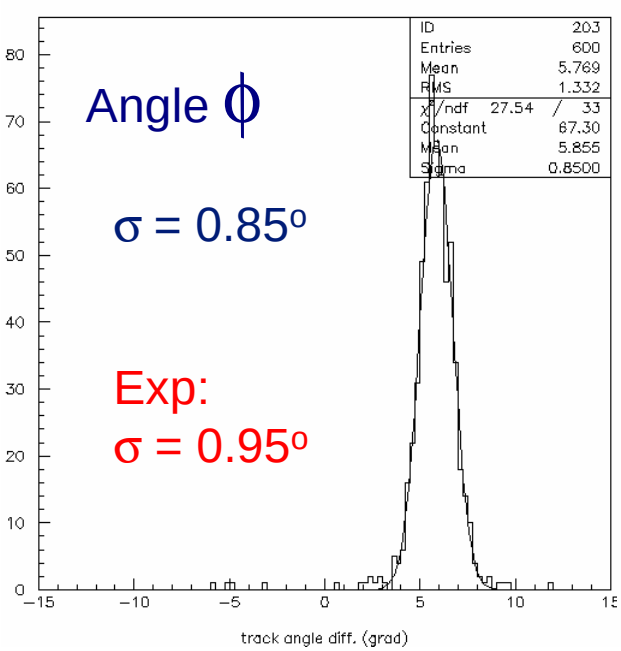
Space point and two angles are measured:

ϕ – In the pixel plane

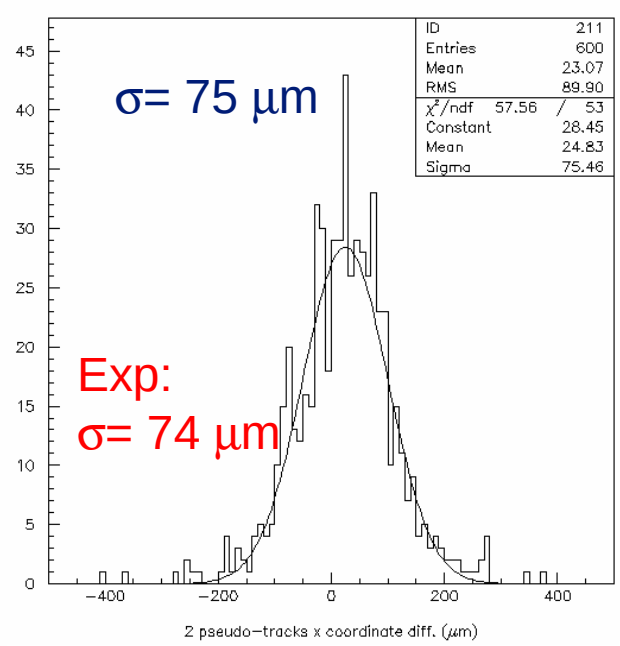
η – is and angle to the pixel plane

Test Beam results: comparison with MC

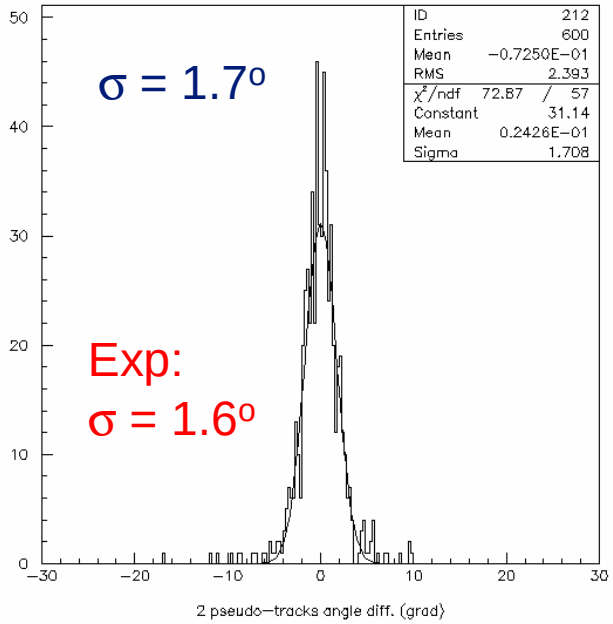
MC simulation: **Thr. = 1.5 el, σ_t = 300 μm**



Reconstructed angle of the track.



Difference between reconstructed space points for two pseudo tracks.

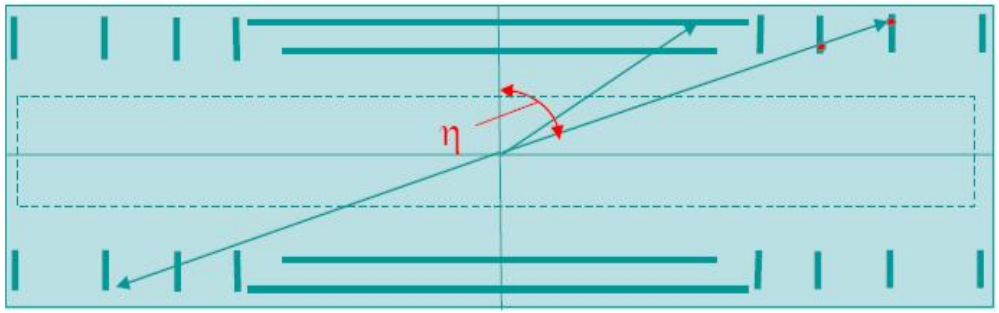


Difference between angle of the track for two pseudo tracks.

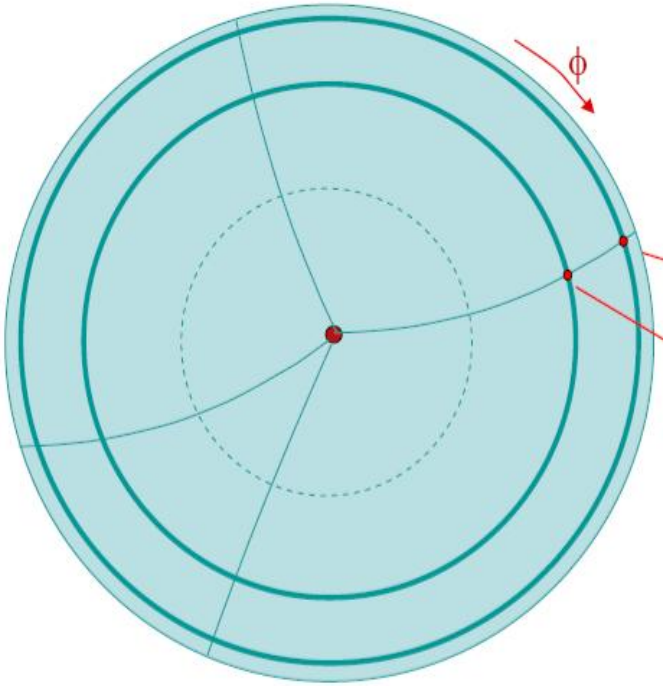
Anatoli Romaniouk (ATLAS TRT group)

INGRID
Gas Tracker

It is assumed that this detector will occupy the outer radii of the Inner Tracker.



Possible layout:
Two layers interleaved with moderator or dense TR radiator.



Why is that interesting?

A vector tracking !

(*TR information might be a complementary feature*)

1. Precision space points X,Y
2. Vector direction ϕ, η

InGrid Gas Tracker

Test beam studies (5 GeV).

May 2008 test chamber:

- InGrid technology
- Drift distance= 16 mm
- V_{drift} = 3800 V
- E_{drift}= 2000 V/cm
- V_{amp} ~470 V
- Gas gain ~ 800 – 3500
- Protection layer 30 μm
- Amplification gap - 50 μm
- Orientation: 20 degree to the beam and horizontal.
- Gas Mixtures
- Ar/CO2
- Xe/CO2
- He/Isobutane

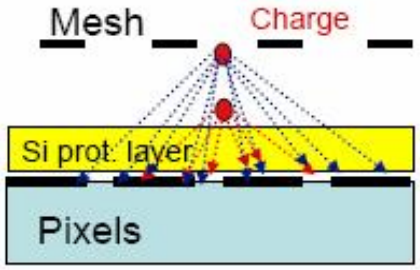
For the gas mixture 70%Xe+30%CO_2

Total drift time ~ 300 ns
Ion signal ~ 80 ns
Transverse diffusion σ_T ~220 μm/$cm^{1/2}$
Longitudinal diffusion σ_L ~120 μm/$cm^{1/2}$

Maximum gas gain achieved:

~ 2500

Operating threshold ~ 800 el.



Effective threshold > 1600 el.
+ induced charge effect

This corresponds to a primary electron threshold > 0.7 el

Anatoli Romaniouk

Conclusions

- A huge piece of work lies ahead and there is room and need for motivated participants.
- Although the exact schedule and magnitude of the upgrade is uncertain the need to upgrade will persist as beam intensity evolves over the next few years.

This talk has only covered the Inner Detector at ATLAS several additional sub-systems are seriously working on upgrade plans over a more relaxed time frame. In addition to what is discussed here, we are making and planning contributions to the Liquid Argon and MDT upgrade efforts.