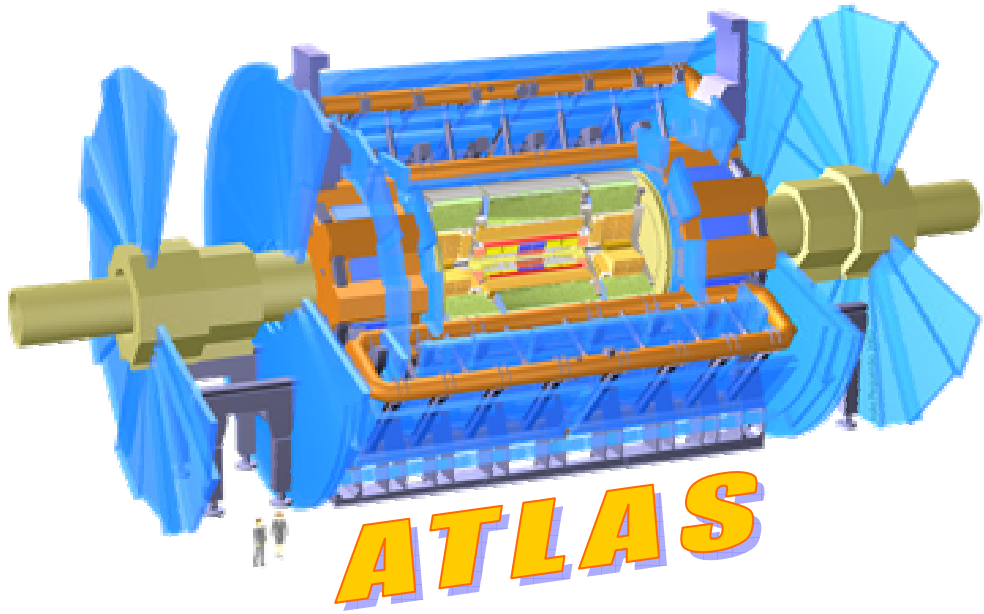


# The ASDBLR and DTMROC

## Detector Mounted Readout for the ATLAS TRT

**Mitch Newcomer for the ATLAS TRT Electronics Group**



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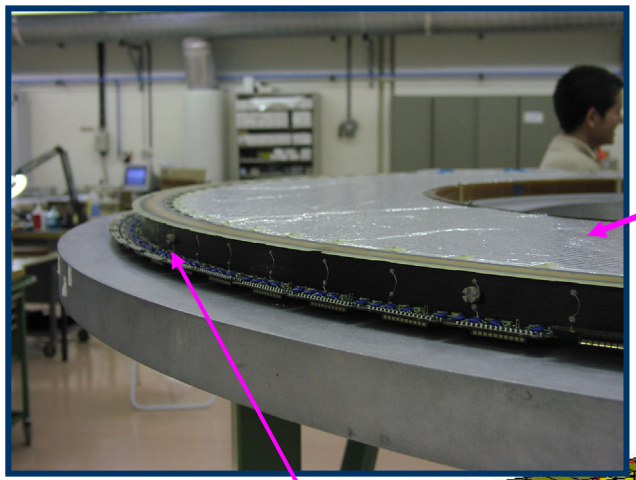
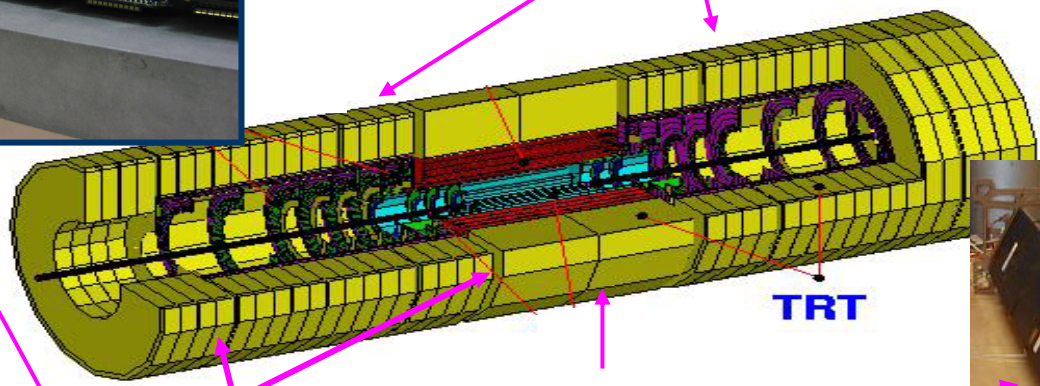
# TRT

ATLAS TRT
FEE2003



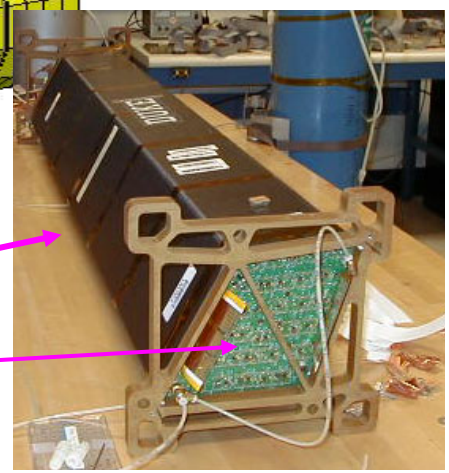
TRT Wheels

Radially Aligned Straws (320K channels)




Barrel Modules

Axially aligned 100K channels



TRT Front End Electronics



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# Detector Mounted Readout Objectives

ATLAS TRT
FEE2003

- Low Noise/Low threshold operation → ~2000e ENC
  < 300KHz spontaneous straw tube trigger rate
- 1ns time resolution → ~130μm position resolution
- High Rate operation → 20MHz with stable threshold
  (100:1 Signal variation)
- Radiation Tolerance → $3.5X10^{14}$ n/cm 5MRad
- Reliable operation of high bandwidth Analog and Digital readout ASICs without interference
- ATLAS Read Out Driver Compatibility


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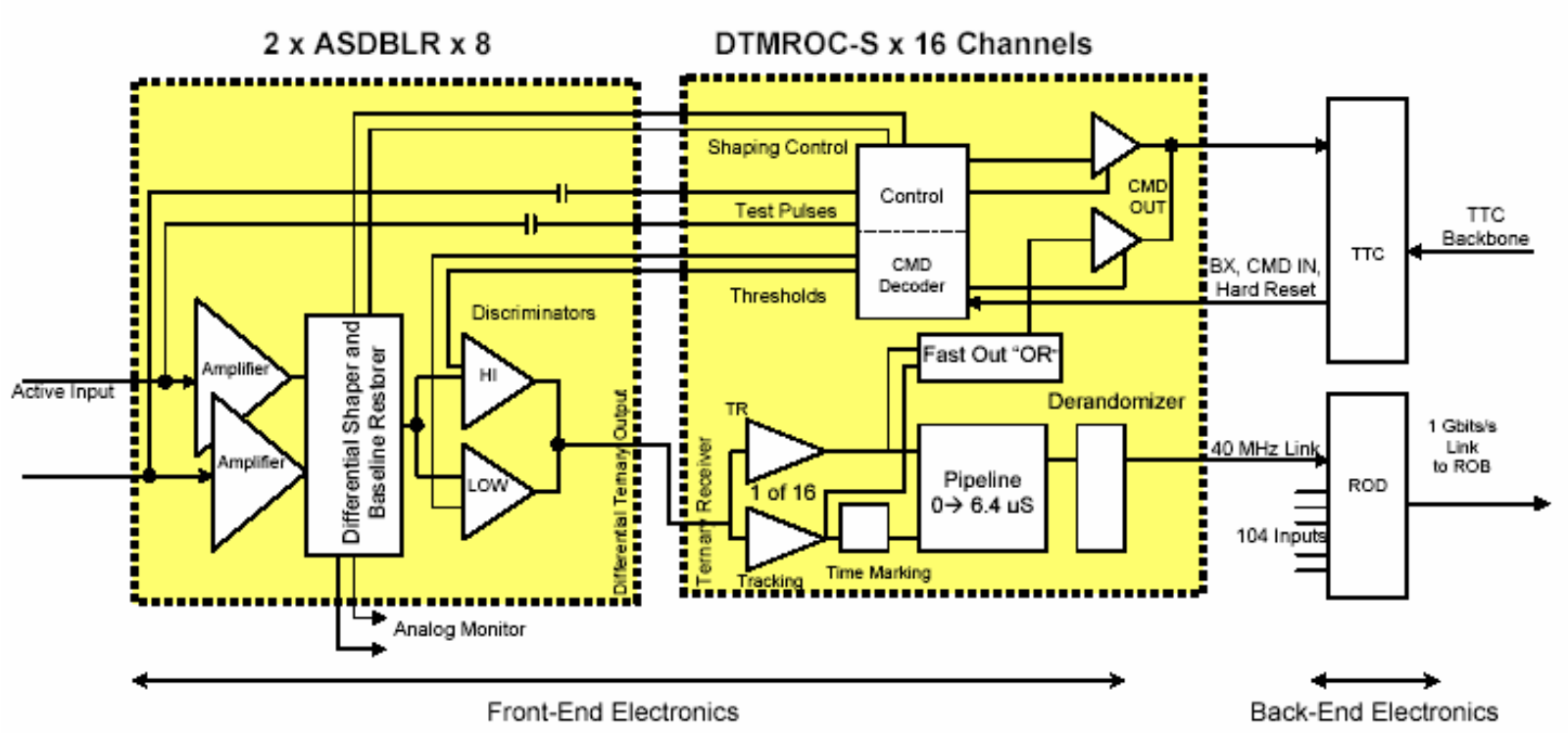
# Readout Electronics basic block

ATLAS TRT
FEE2003

## 16 channel custom ASIC triplet



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# ASDBLR References

ATLAS TRT
FEE2003

**Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL Technology**

N. Dressnandt, N. Lam, F.M. Newcomer, R. Van Berg and H.H. Williams

IEEE (2000) *Trans. On Nucl. Sci. V48 n4 p1239*

**An Amplifier-Shaper-Discriminator with Baseline Restoration for the ATLAS Transition Radiation Tracker**

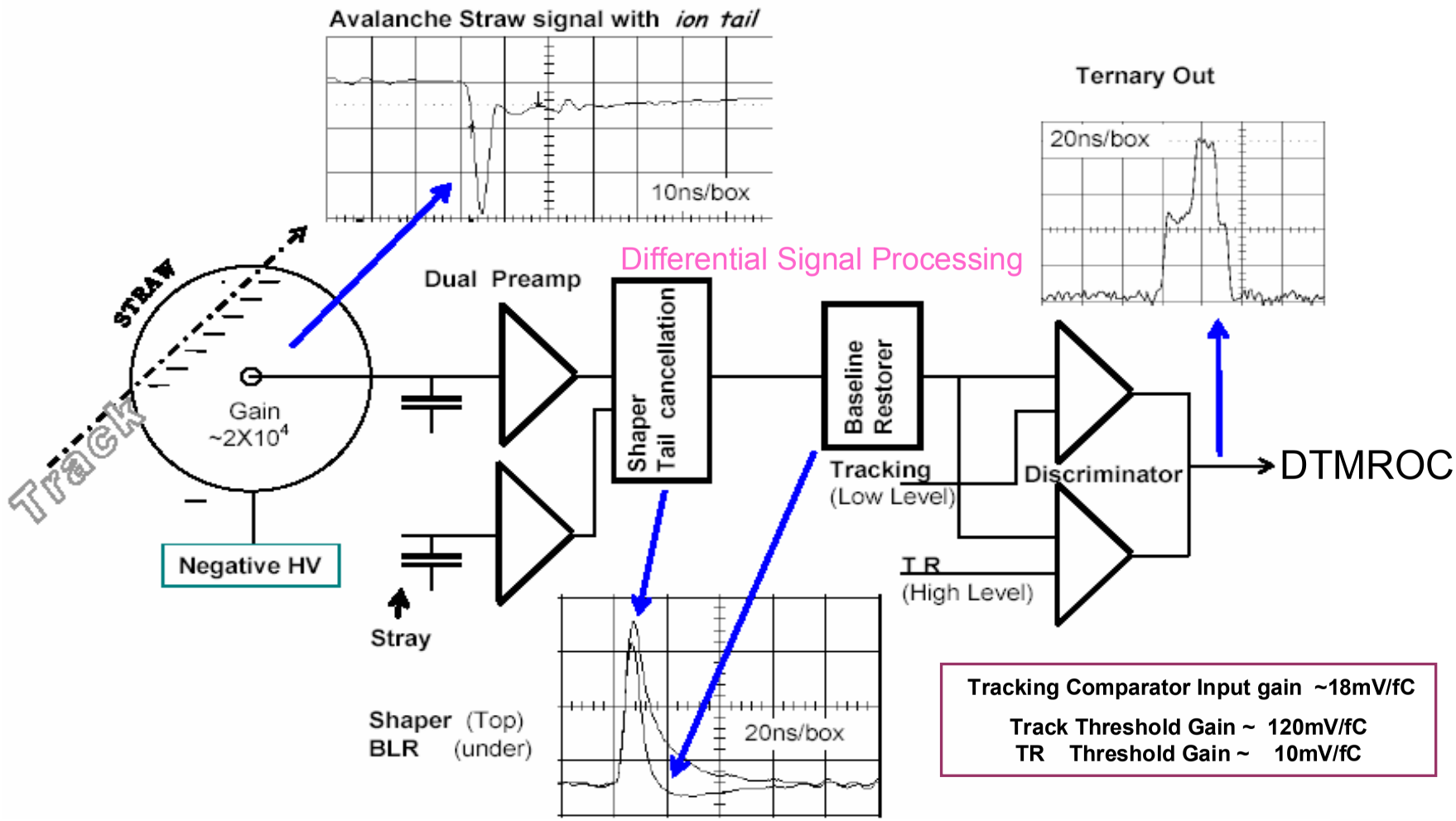
B. Bevensee, F.M. Newcomer, R. P. Van Berg and H.H. Williams

IEEE (1996) *Trans. on Nuc. Sci. V 43 p1725*

http://www.hep.upenn.edu/atlas

# ASDBLR
## 8 Ch Analog Front End

**ATLAS TRT**
**FEE2003**





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# ASDBLR Basic Design Spec

ATLAS TRT
FEE2003

- Power ~ 40mW/ch.
- Preamp Input protection ~ 2.8mJ.
- Analog Gain ~ 18mV/fC at Comparator input.
- Double Pulse Resolution ~ 25 – 50ns dependent on 1st pulse amplitude.
- Spontaneous Trigger Rate at 2fC threshold ~ 300KHz.
- High Threshold Maximum Range → 140fC.
- Ternary (comparator) output levels (nominal Design):

| Signal | Tern Pos | Tern Neg |
|---|---|---|
| Quiescent | -400uA | 0uA |
| Track only | -200uA | -200uA |
| Track & TR | 0uA | -400uA |


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# ASDBLR Implementation

ATLAS TRT
FEE2003

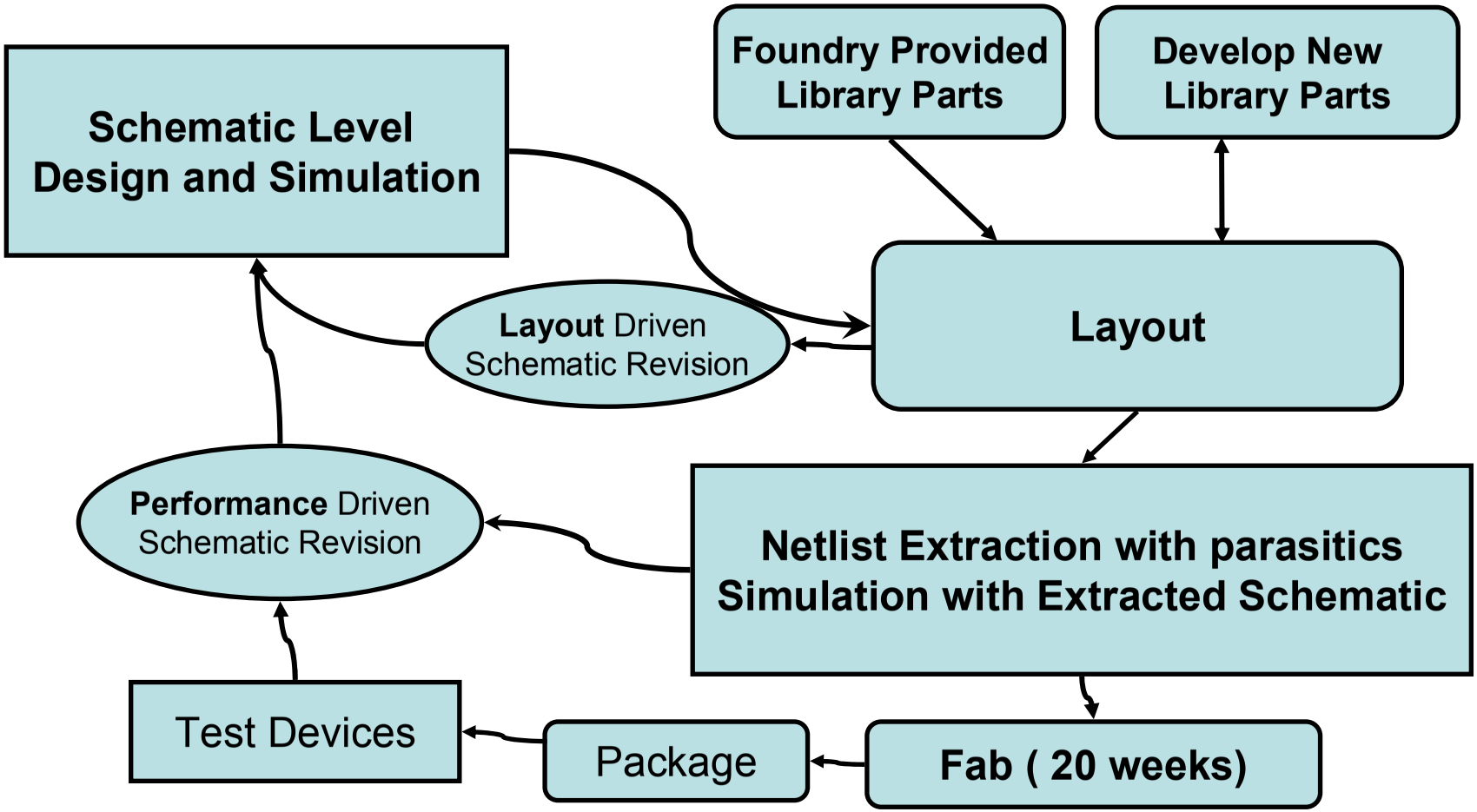
- Process - Rad Tolerant 0.8um BiCMOS Technology (DMILL)
- Designed at the discrete device level using SPICE for Simulation
- Channel Complexity 160 Bipolar Transistors / 10 CMOS Switches
  160 Resistors / 105 Capacitors

- Channel based Layout ~
  - Avoided metal runs over transistors/resistors.
  - Double vias where possible.
  - Separated Analog and Comparator/Ternary Driver Power
  - Dedicated power bus distribution at the channel level.
  - Substrate Contact and Power buss isolation between ch.
  - Preamp Supply filter on each channel.

- Eight (nearly) identical Channels on 340um Pitch

# ASDBLR design Cycle

ATLAS TRT
FEE2003





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# ASDBLR02 Final Design

ATLAS TRT
FEE2003

## Final Design Improvements

- Reduce area of input protection network → Reduce Capacitance 11pf → 5pF.
- Increase Input transistor current to 7.5uA/m reduce beta loss.
- Increase analog gain by 50% to reduce sensitivity to device matching in comparator. (56mV/fC at BLR output)

## Measured Results

- Input referred threshold matching good, RMS < .25fC
- Noise ~ 2100e ENC on board with ~5pF capacitance (100e/pf).
- Power ~ 40mW/channel.
- High Rate operation ~ demonstrated to 20MHz (pulser tests)


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# Production ASDBLR

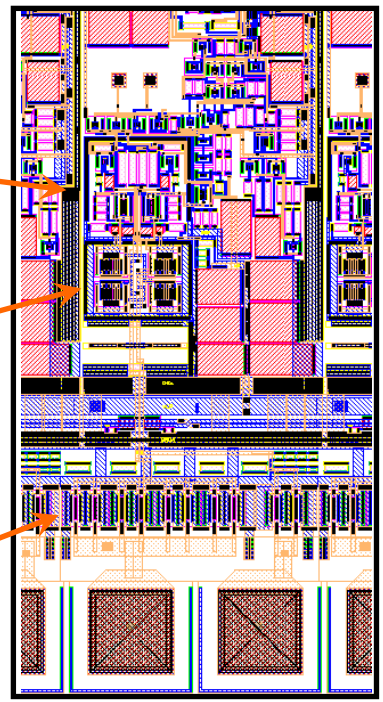
ATLAS TRT
FEE2003

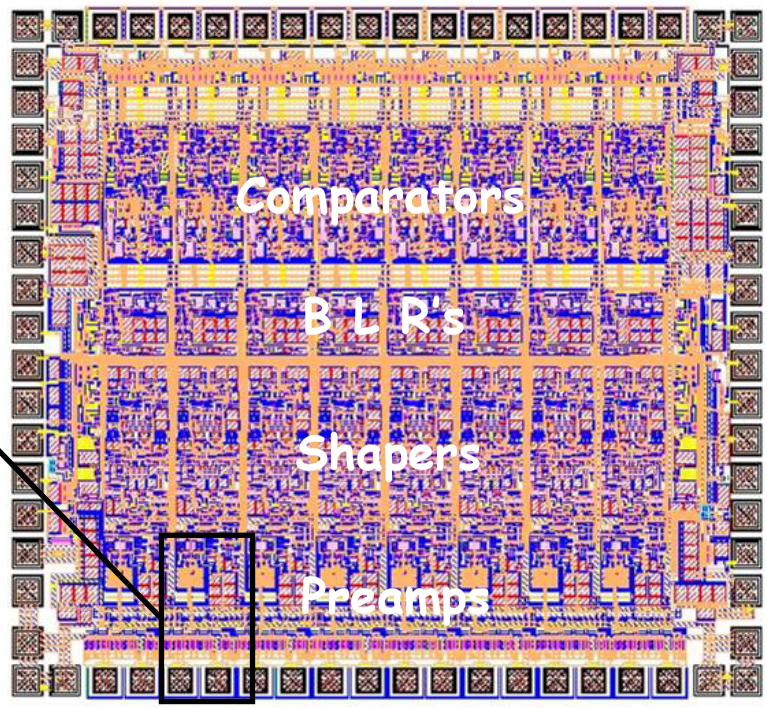
3.3 X 3.6mm

Dual Preamps intermingled layout

Input Transistors in cross Quad Configuration

Input protection NPN Transistors Expanded Geometry Emitter Stripes 4 x 30 um





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# ASDBLR Radiation Testing

ATLAS TRT
FEE2003

- **Gamma Testing up to 7MRad with no significant performance degradation.**
- **1MeV NEIL Neutron Testing to $5X10^{14}$ (10 year with saftey factor) shows a significant reduction in beta resulting in lower gain and increasing the channel to channel threshold offset. At Beta = 30 the gain is lowered by ~ 50%.**
  - DMILL NPN Beta is sensitive to Thermal Neutrons
    More study needed. Moderator re-evaluation?


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# Neutrons

ATLAS TRT
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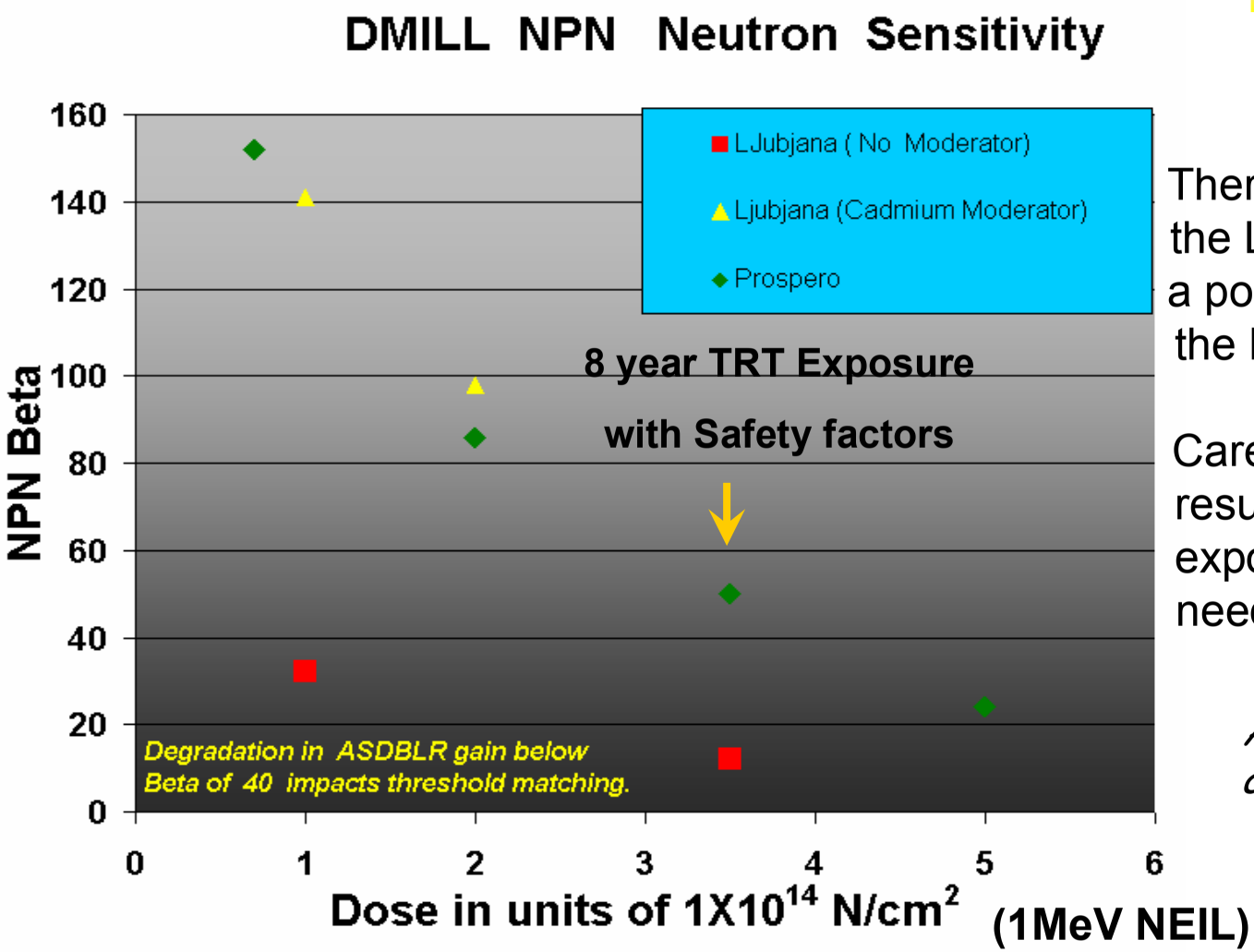


Thermal Neutrons present at the Ljubjana facility point out a possible weakness using the DMILL Process.

Careful comparison of these results with the expected exposure in the ATLAS ID need to be performed.

*All devices annealed at 150° C for 48 hrs.*



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# ASDBLR Radiation Testing report NSS 2002

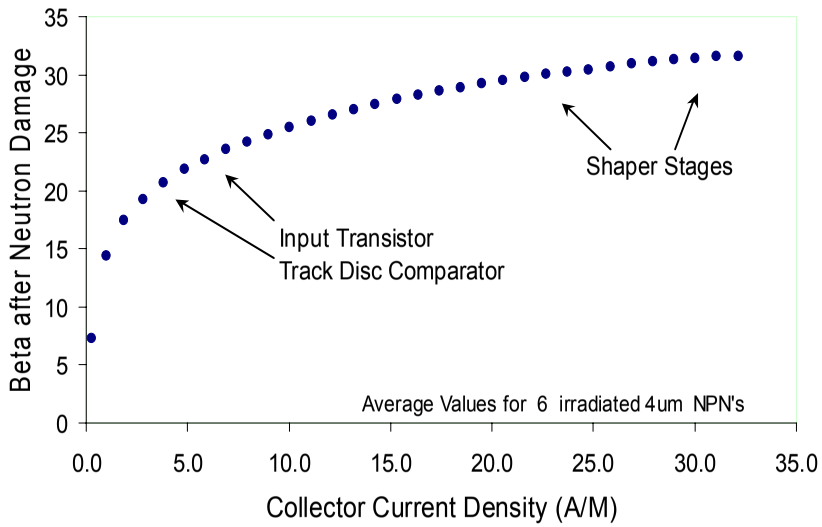
ATLAS TRT

FEE2003

## Summary of Device tests to 11 / 2002

| ASDBLR | # chips | Power on | Date | Type Dose[1] | Change in Resistance | Post Rad NPN Beta |
|---|---|---|---|---|---|---|
| 99 | 3 | | 4/00 | $5X10^{13}$ n | NA | 84 |
| | 3 | | 4/00 | $1X10^{14}$ n | NA | 52 |
| | 6 | x | 5/01 | 5Mrad γ | 5% | 180 |
| 00 | 9 | | 10/01 | $3.5\ X10^{14}$ n | 1.5% | 55 [3] |
| 01 | 6 | x | 6/02 | $1.5X10^{14}$ p | 5% | 70 |
| 01 | 16 | x | 7/02 | 7MRad γ | 8% | 130 |
| 01 | 10 | | 5/02 | $3.5X10^{14}$ n | 10.4% | 11 [2,3] |

[1] n and p dose is in units of particles/cm$^2$.
[2] Thermal neutron dose high ~$10^{14}$ n/cm$^2$.
3 After annealing 23hrs@150C




The measured current gain of DMILL NPN transistors after exposure to 3.5X1014n/cm2 and prior to annealing. The arrows show the operating points chosen for various parts of the ASDBLR channel design. After annealing the beta increased by a factor of two.

**From: Radiation Hardness: Design Approach and Measurements of the ASDBLR ASIC for the ATLAS TRT**

*Nandor Dressnandt, Mitch Newcomer, member IEEE, Ole Rohne and Steven Passmore*

**See NSS 2002 Confrence Record**



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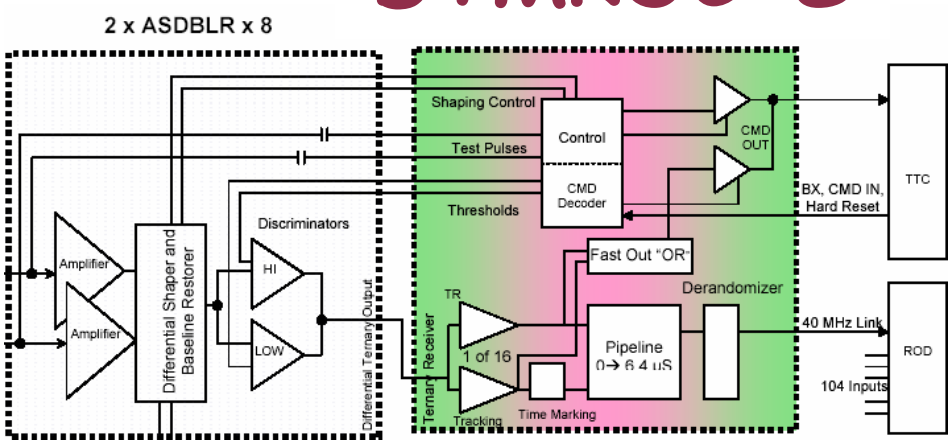
# DTMROC-S

ATLAS TRT
FEE2003





## CERN MicroElectronics and Penn

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***F.Anghinolfi, Ph.Farthouat, P.Lichard***

*CERN, Geneva 23, Switzerland*

***R.Szczygiel***

*CERN, Geneva 23, Switzerland and INP, Cracow, Poland*

***N.Dressnandt, P.T.Keener, F.M.Newcomer, R.Van Berg, H.H.Williams***

*University of Pennsylvania, Philadelphia, USA*

# DTMROC References

ATLAS TRT
FEE2003

***Implementation of the DTMROC-S ASIC for the ATLAS TRT Detector in a 0.25µm CMOS technology***

***V.Ryjov, F.Anghinolfi, Ph.Farthouat, P.Lichard, R.SzczygielN.Dressnandt, P.T.Keener, F.M.Newcomer, R.Van Berg, H.H.Williams, T.Akesson, P.Eerola***

***NSS 2002 Confrence Record***

***Progress in the Development of the DTMROC Time Measurement Chip for the ATLAS Transition Radiation Tracker (TRT)***

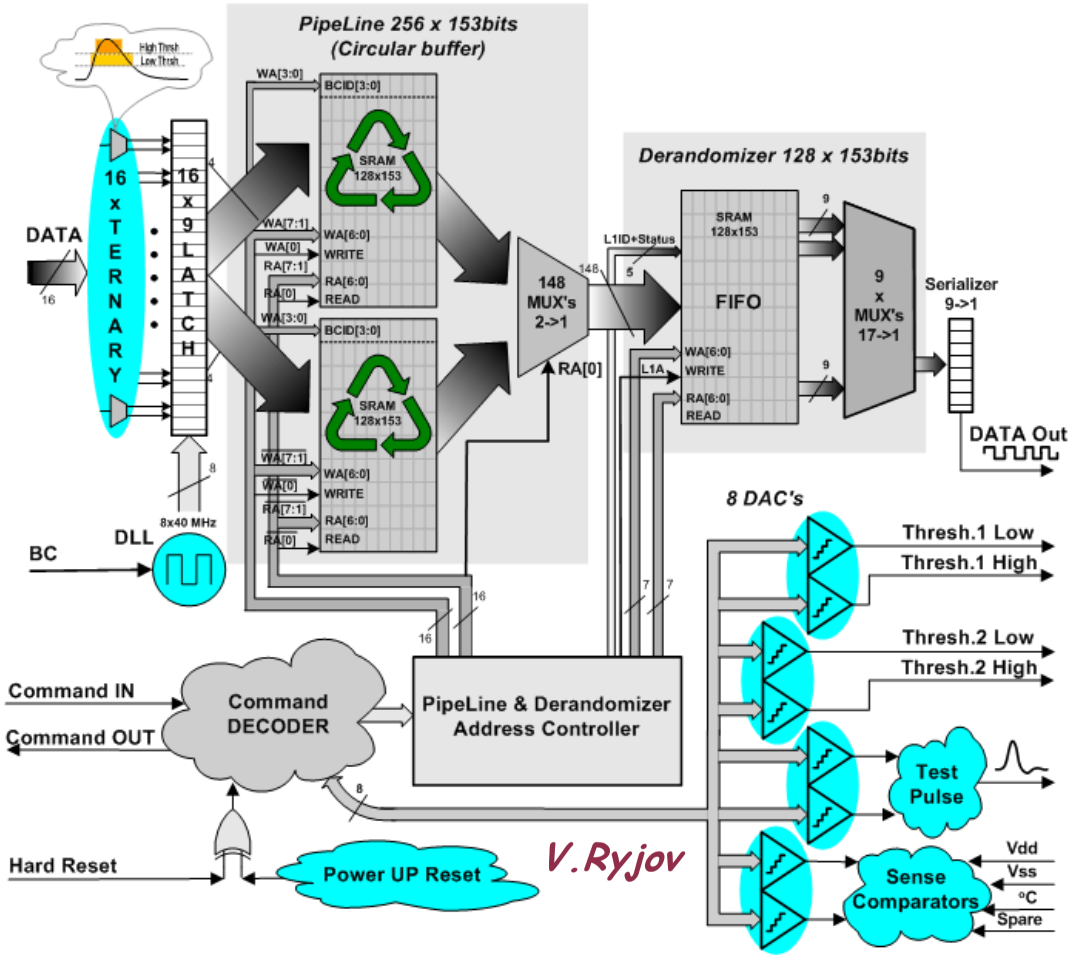
C. Alexander, F. Anghinolfi, N. Dressnandt,
T. Ekenberg, Ph. Farthouat, P. T. Keener, N. Lam, D. La Marra,
J. Mann, F. M. Newcomer, V. Ryjov, M. Soderberg, R. Szczygiel,
V. Tikhomiro, R. Van Berg, H.H. Williams

**IEEE (2000)** ***Trans. On Nucl. Sci. V48 n3 p514***

**http://hep.upenn.edu/atlas**

# DTMROC *functional Blocks*

ATLAS TRT
FEE2003



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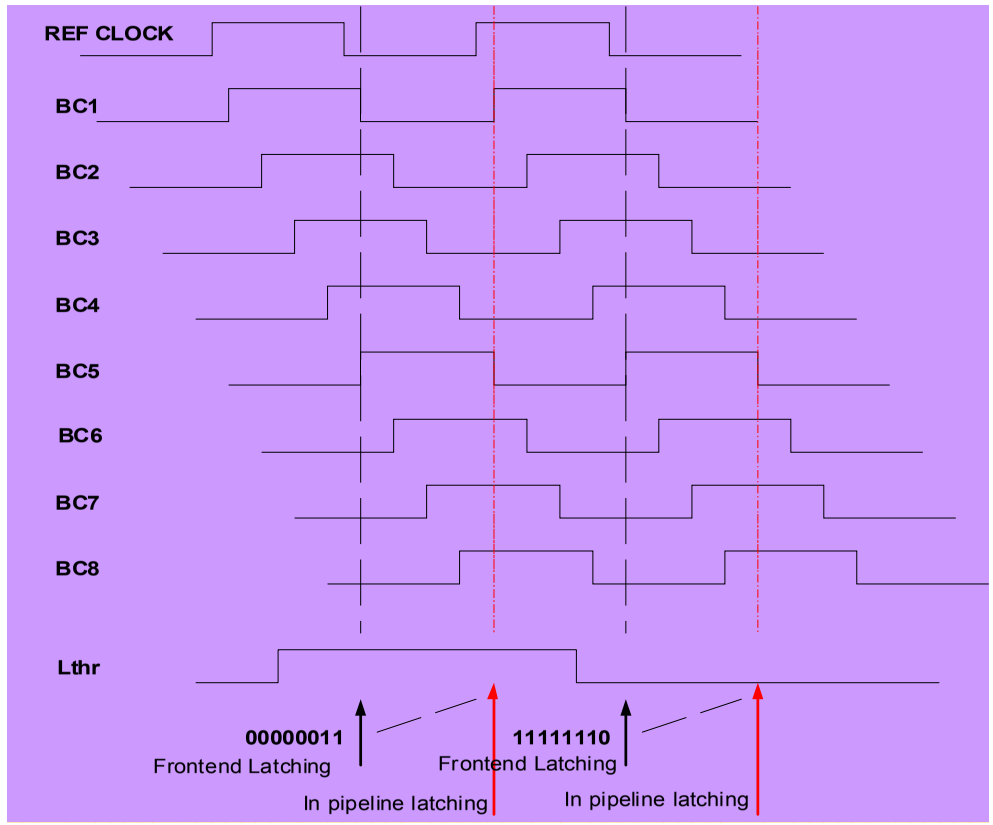
# DTMROC-S
## *Time Marking*

ATLAS TRT
FEE2003

### *32 elements delay chain, phase detector, charge pump*

40MHz Clock → 3ns time bins

- *8 equally spaced clock outputs used to sample straw track pulses*
- *50% duty cycle clock regenerated to run the chip core logic*





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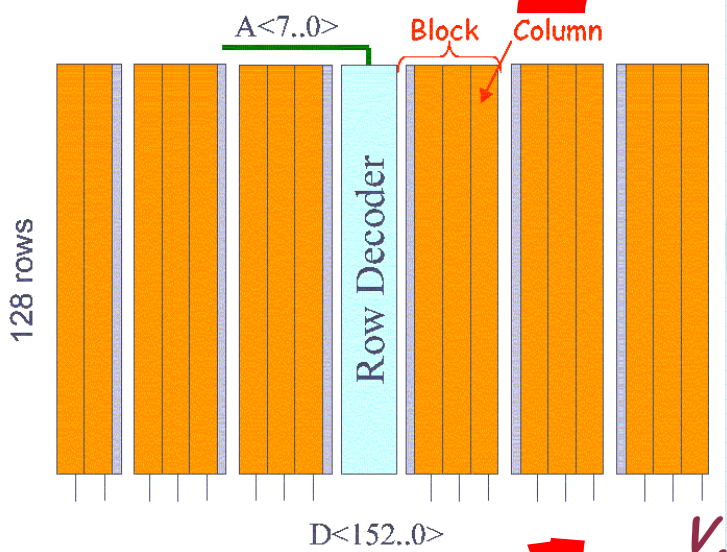
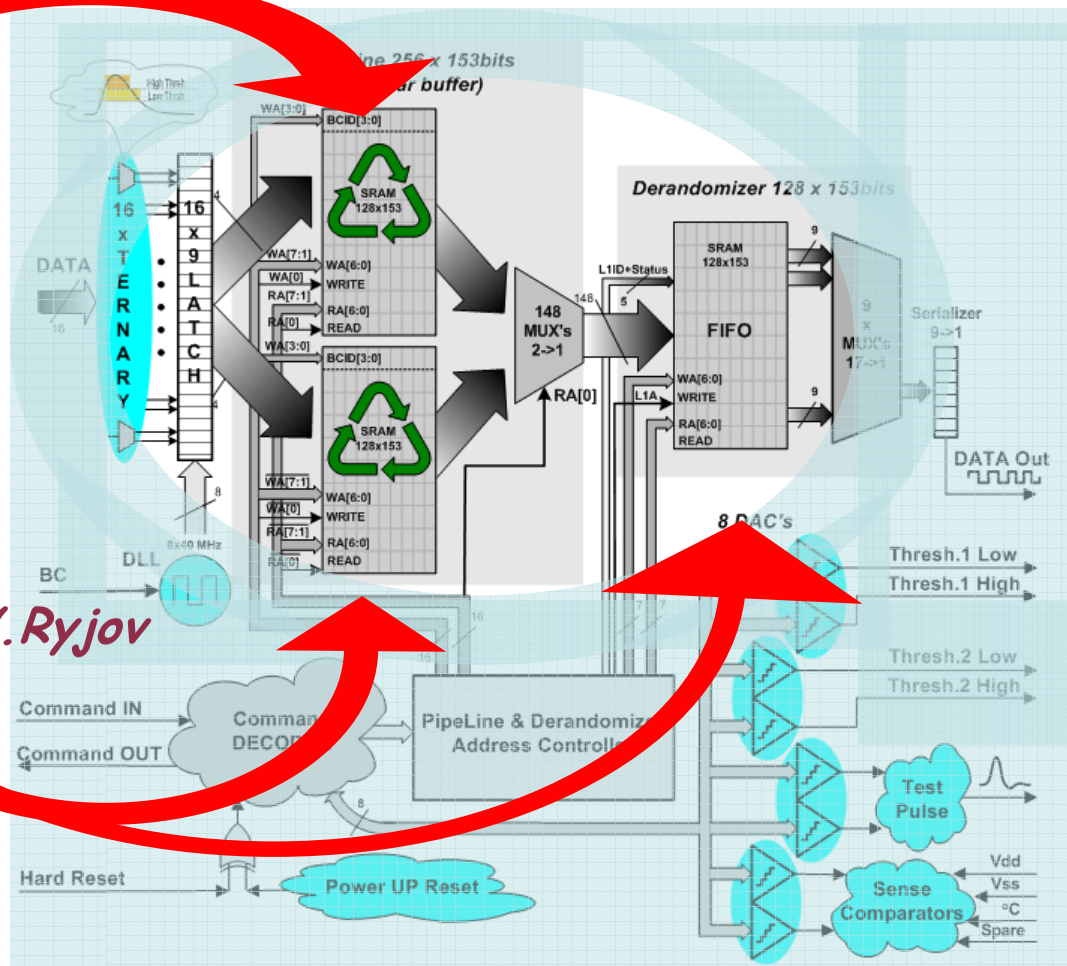
# DTMROC-S
## *Memory / Pipeline*

**ATLAS TRT**
**FEE2003**




*Dual-port 128×153-bit SRAM*
*(2.39kB)*

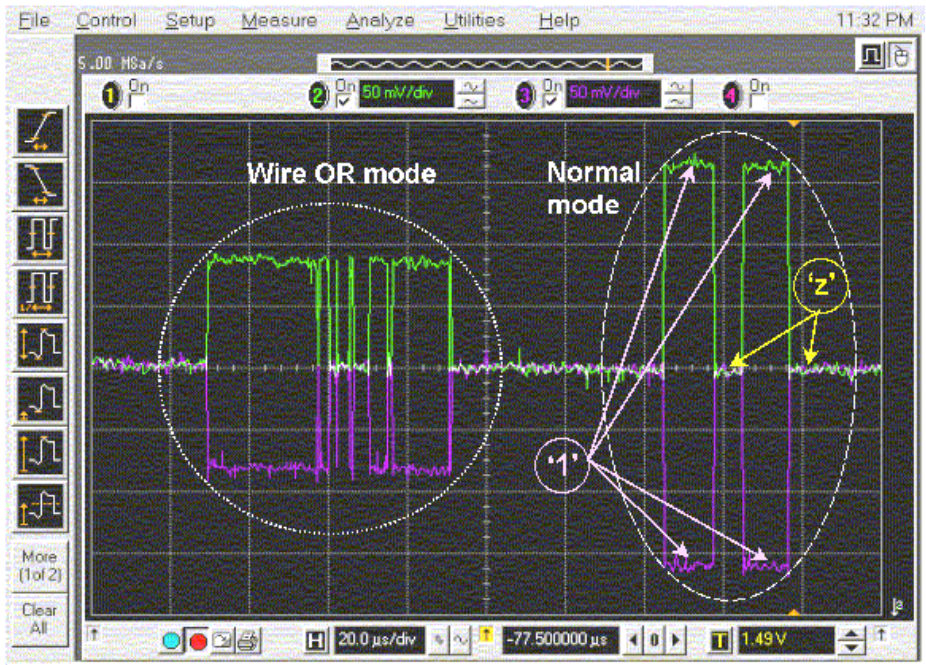
*V.Ryjov*



# DTMROC-S I/O

ATLAS TRT
FEE2003

- *Full/Reduced read-out : 444/380 bits per event, including Header*
- *LVDS-compatible, tristate drivers -> 40 Mbits/s copper links*
- *Wire-OR" – for self triggering fast-out option - selected ternary inputs contribute to the chip-level trigger Up to 15 DTMROCs can be "OR'ed on a common buss*





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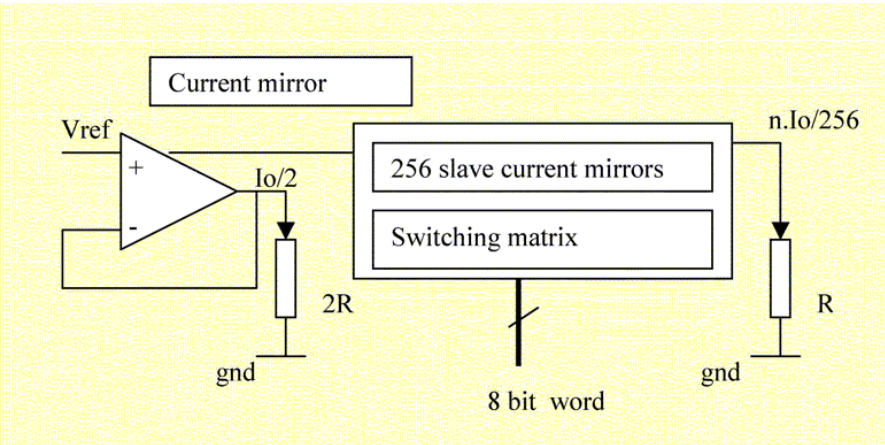
# DTMROC-S DAC's

ATLAS TRT
FEE2003

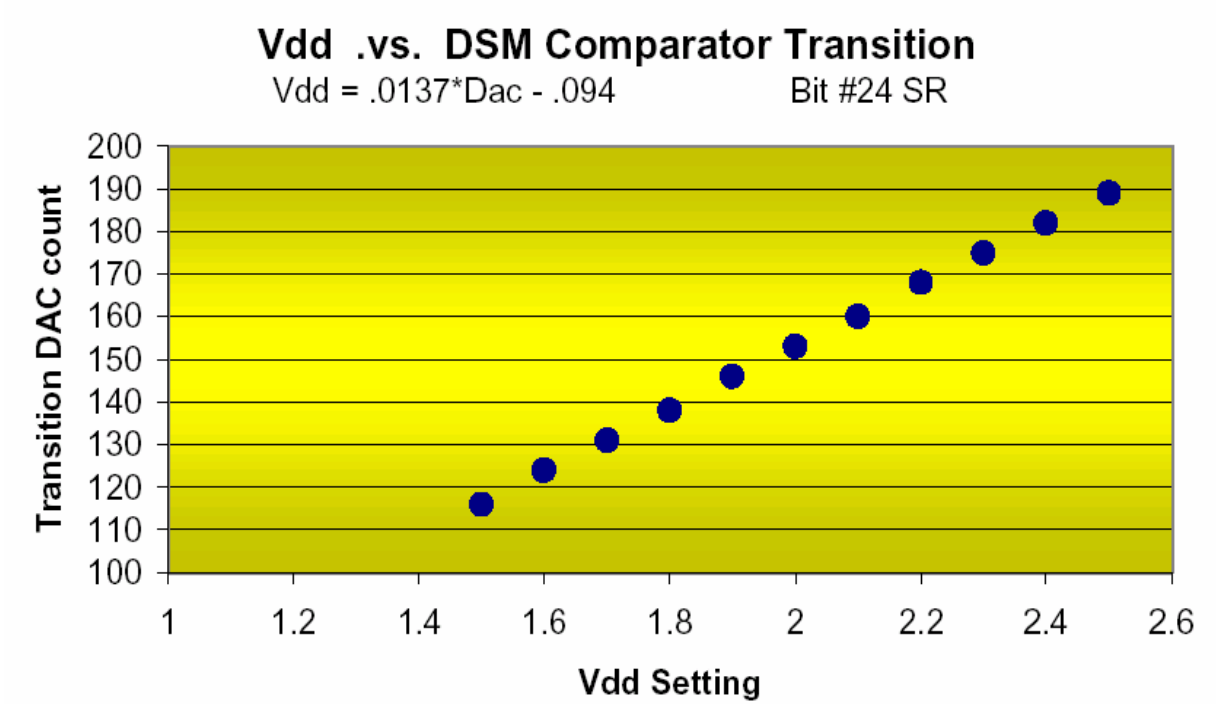
- *Internal bandgap reference 1.26V*
- *Current mirror master - 128 PMOS unit devices (L=8um,W=5um)*
- *256 identical PMOS slave current mirrors per DAC*




# DTMROC-S
## *Analog Sensing*

ATLAS TRT
FEE2003

- *Two DACs*
- *Four Comparators*
  - *Temperature*
  - *VDD*
  - *Ext Voltage 1*
  - *Ext Voltage 2*




*Vdd Sense remained at 191 from 26 – 55 C*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# DTMROC-S *testability*

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FEE2003

- *General-purpose 32-bits Status Register*
- *Logical OR of all DTMROC error indicators in the Data Header field*
- *Parity check logic for all internal registers*
- *Lock status, a "watch dog" and a "dynamic" check circuitries examine the DLL*
- *JTAG Boundary-Scan*
- *Special scan mode - configures all DTMROC flip-flops as a large shift register controlled via JTAG interface*
- *Memory Build-In-Self-Test (BIST) controlled via the Configuration register and JTAG interface*


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# DTMROC-S
## SEU Protection

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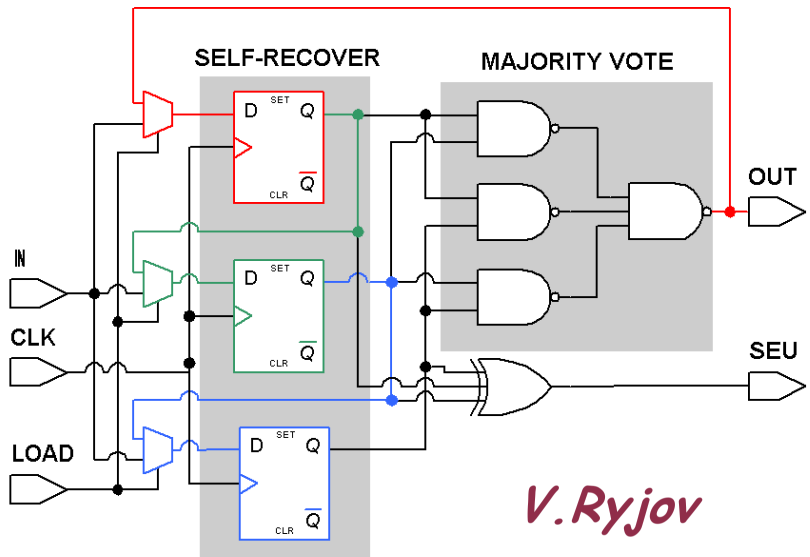
FEE2003

- Internal registers are equipped with parity error check
- The most critical parts are built of the SEU resistant and self-recovering elements based on triple logic with majority vote.
- Statistics circuit monitors the number of detected SEU's

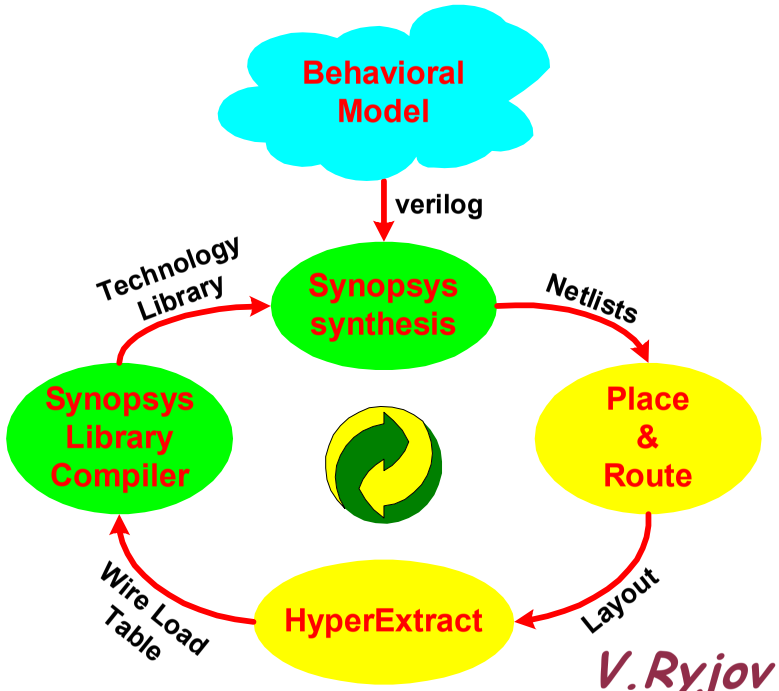



V.Ryjov

# DTMROC-S Design Tools (CERN based)

ATLAS TRT
FEE2003

- *Verilog modelling*
- *Synopsys synthesis tools*
- *Silicon Ensemble Place&Route tools*
- *Completely scripted physical design flow*
- *Number of synthesis-layout cycles to predict post-route timing during RTL synthesis*
- *NC Verilog Simulator – Interleaved Native Compiled Code Architecture*

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# DTMROC-S
## *Layout*

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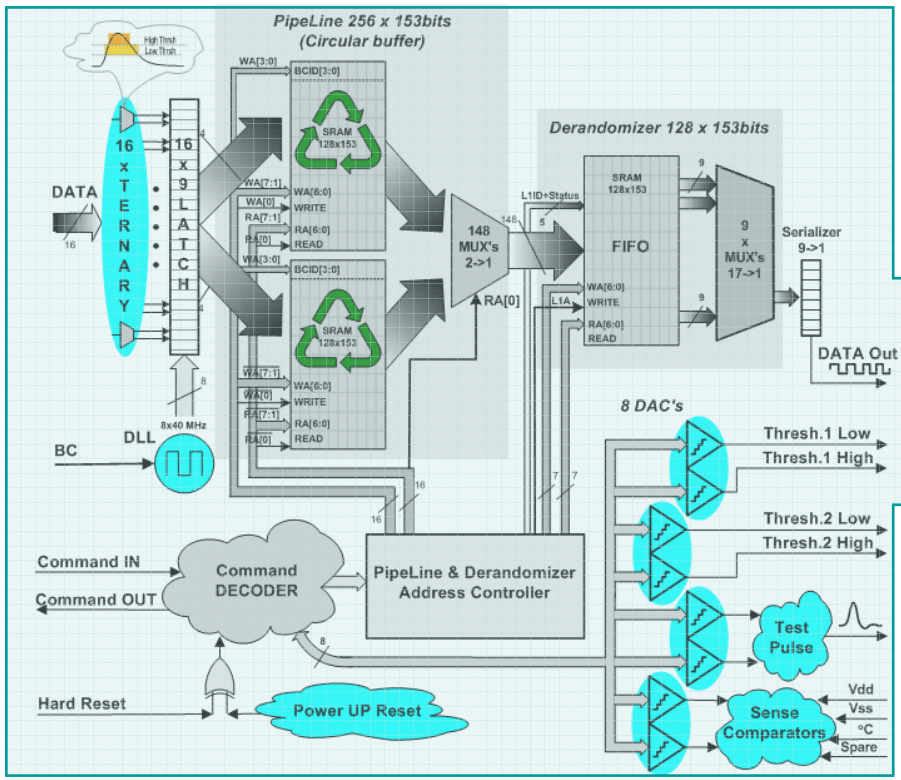
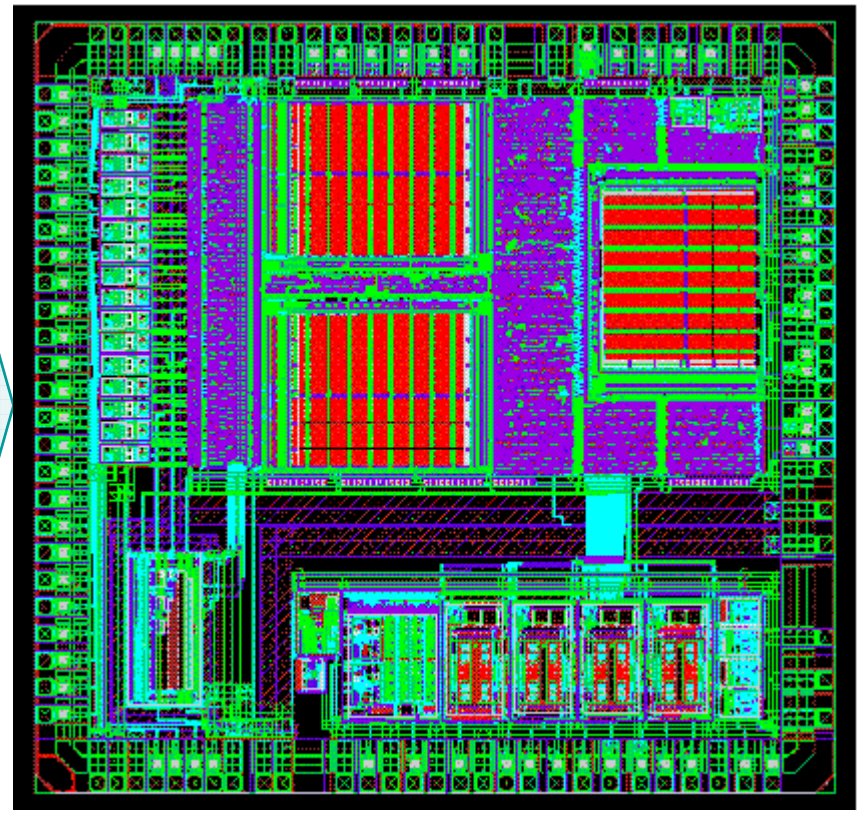
**FEE2003**



*~500k Transistors*

*Die size 5.2×5.0 mm²*



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# DTMROC-S
## Fab

ATLAS TRT
FEE2003

- Submitted/fabricated (.25um process) in Jan 2002
  - Wafer size 8" (350μm) → 1017 useable dies per wafer
- 850 chips tested on the mixed signal IMS Tester at CERN
- 5 process corner (85/92/100/115/125%) evaluated
- 87% Yield for 850 chips
- Irradiation tolerance test at CEA Saclay Pagure facility in July 2002
- SEU sensitivity evaluated at the CERN PS in July 2002
- Test Beam at the CERN H8 in August-September 2002

# DTMROC-S Radiation Testing

ATLAS TRT
FEE2003

## Total Ionizing Dose tolerance

- Tested at CEA Saclay Pagure facility in July 2002
- 7 Mrad total dose / 1.33 MeV gamma radiation
- ~10% increase in the DAC's output voltage after irradiation, no DNL change
- No variations in the power consumption and the chip performance

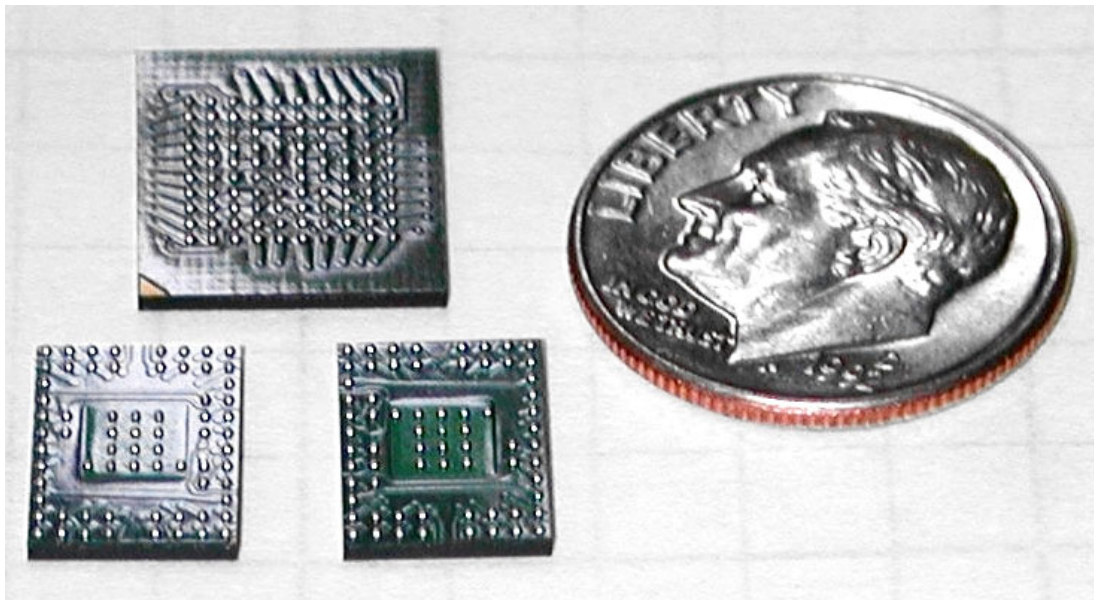
## SEU sensitivity

- Evaluated at the CERN PS irradiation facility in July 2002
- Integrated fluence of $1.8 \times 10^{14} p/cm^2$ on 24GeV beam
- SEU cross-section for a single D flip-flop in different internal registers varies from $0.8 \times 10^{-14}$ to $1.2 \times 10^{-14}$ $cm^2$
- Impact of SEU's in the vital components is suppressed by self-recovering logic

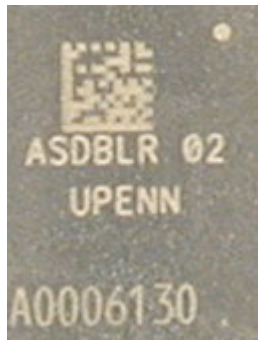
# ASDBLR & DTMROC Packaging Labeling

ATLAS TRT
FEE2003

## Fine Pitch Ball Grid Arrays




Laser Marked packages
2D Bar code
Human Readable numbering



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# ASIC Testing

ATLAS TRT
FEE2003



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# ASDBLR
# DUT Board on IMS

ATLAS TRT
FEE2003

# IMS Tests on ASDBLR

ATLAS TRT
FEE2003

**Read Bar code and record test (event) Number**

- Supply Current
- Input voltage/resistance
- Output current / switching
- Low Threshold response to 0, 2, 3 fC input
- High Threshold response to 30 fC.

**Write Results to SQL data base**


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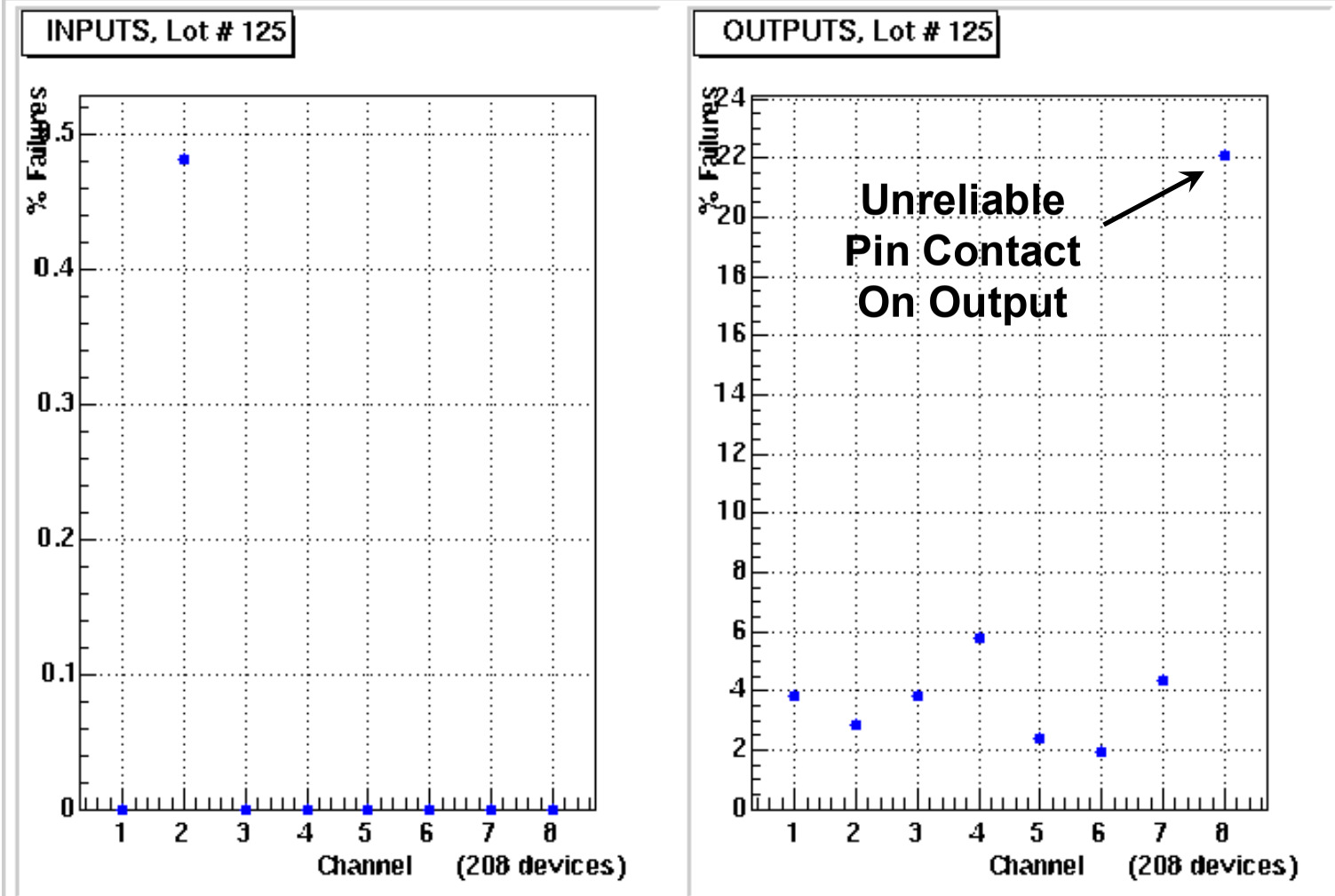
# Failures Due to Socket Pin Reliability

ATLAS TRT
FEE2003



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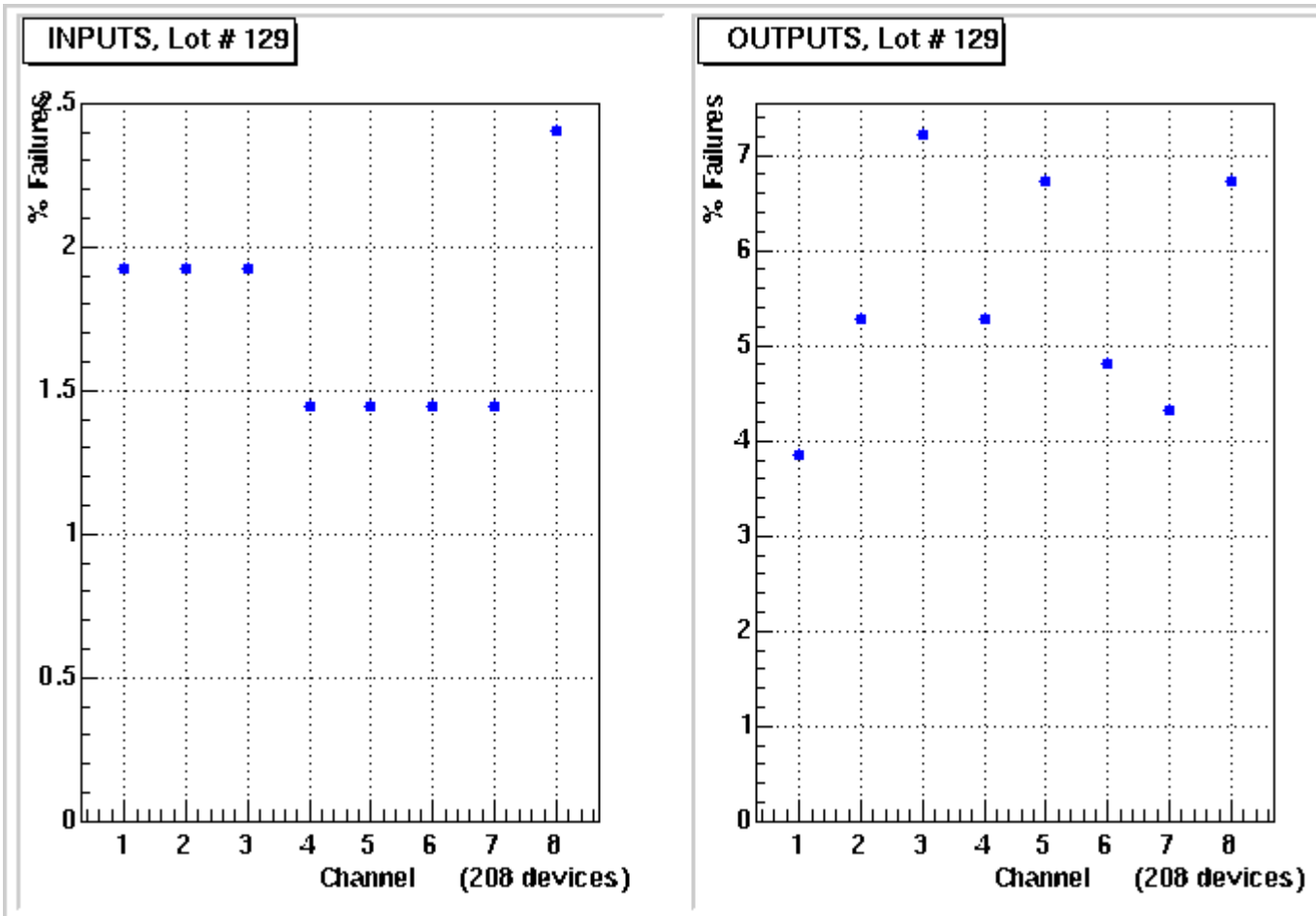
# Using Forced Air to clean pogo pins

ATLAS TRT
FEE2003



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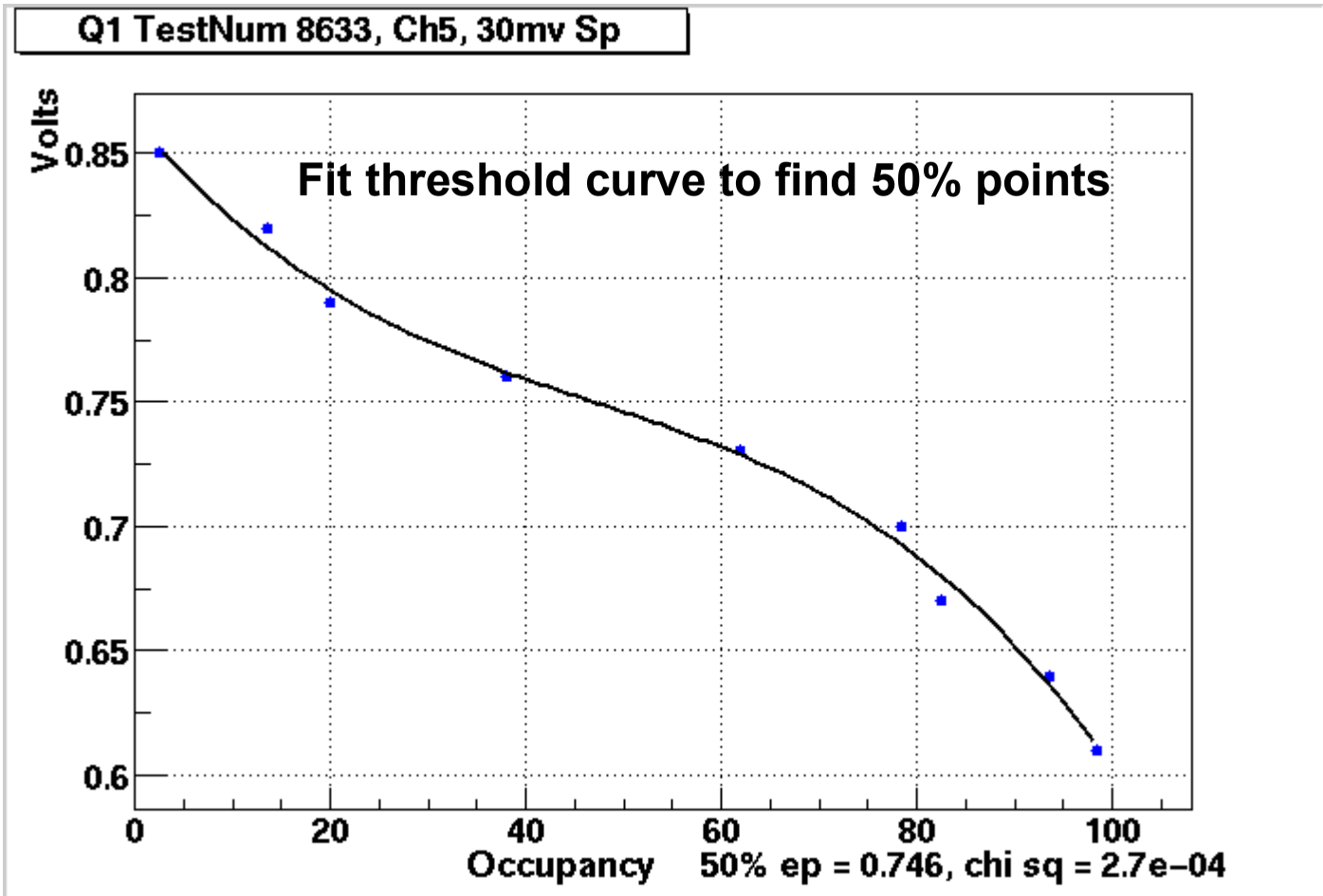
# Finding ASDBLR 50% Threshold

ATLAS TRT
FEE2003



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# IMS Beta Stage Testing Experience

ATLAS TRT
FEE2003

- First 3000 chips demonstrate minor problems.
- Socket Pins must be cleared with forced air daily.
- Some wandering of the Threshold 50% points day to day.
- Bar code too close to chip label, leads to ~5% read errors.

**False failure rate ~10% presently**
**Should improve over time.**


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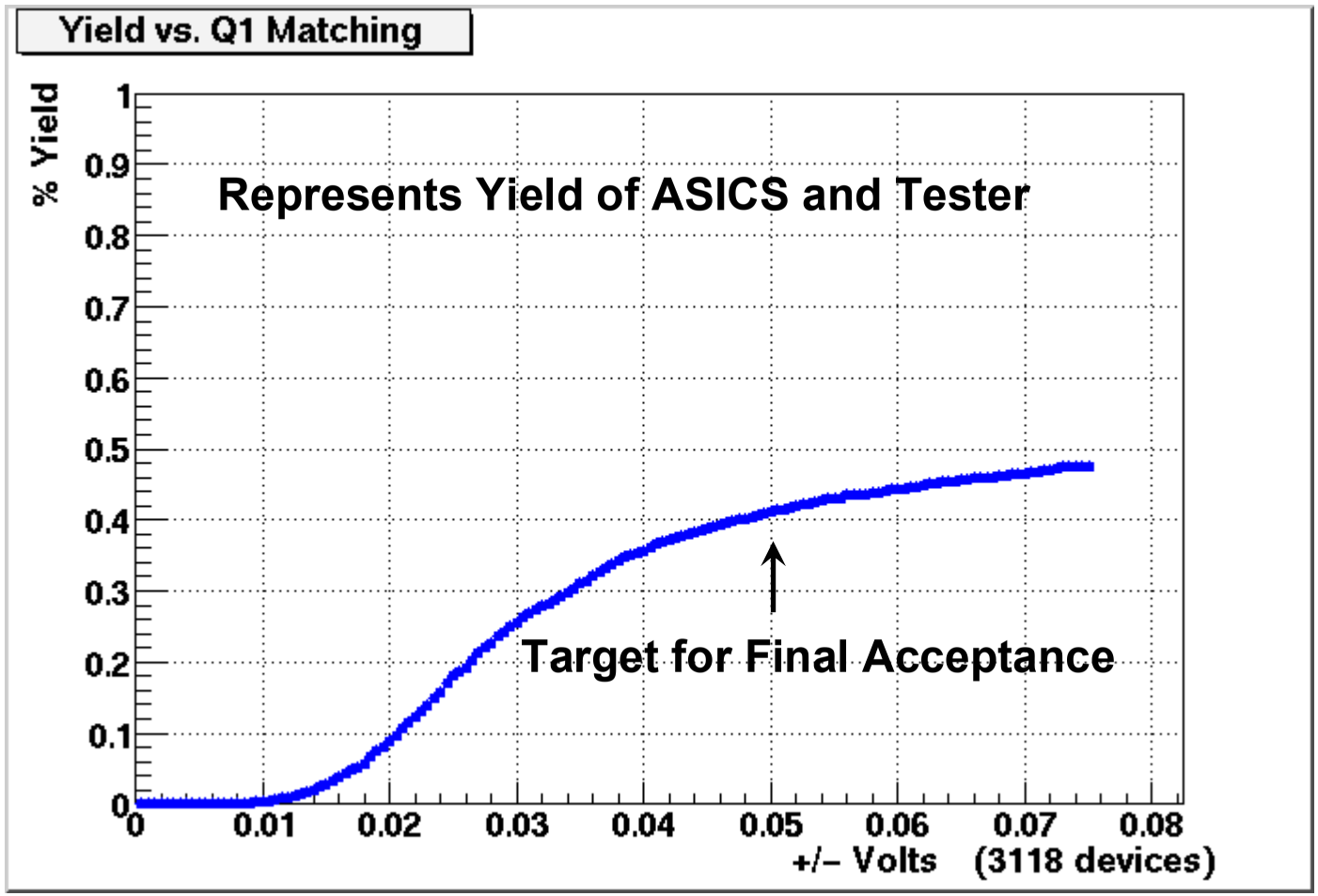
# Yield on First 3000 Devices with Beta Testing version

ATLAS TRT
FEE2003





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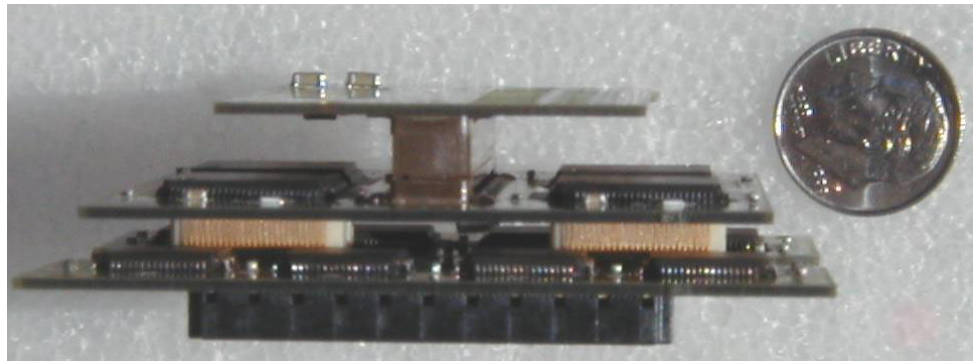
# End Cap Wheel Boards

ATLAS TRT
FEE2003

- 192 channels per assembly
- 2 DTM Board's = 1 virtual module.
  - 1/32 of endcap type A wheel
- Flexible interconnect between 64 channel DTMROC boards allows 192 channel board to follow curvature of wheel tread.
- Initial noise measurements on prototype detector show operation at 2fC possible.

Side view of the stackup of one 64 channel ASD board, one (old) 64 channel DTM board, and a connector board



**192 channel DTMROC board**



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# Barrel Module Board with 15 ASDBLR / DTMROC triplets

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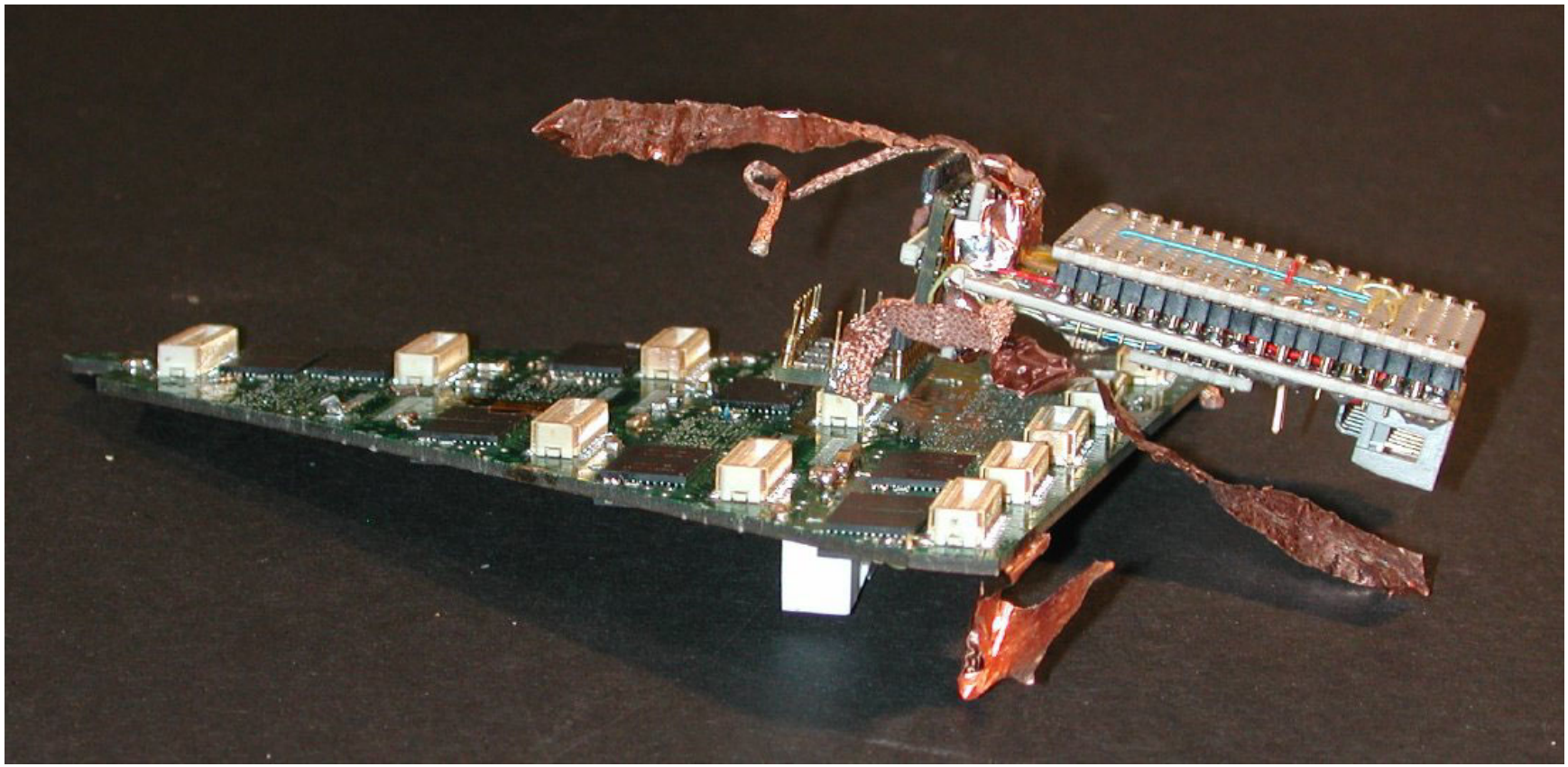
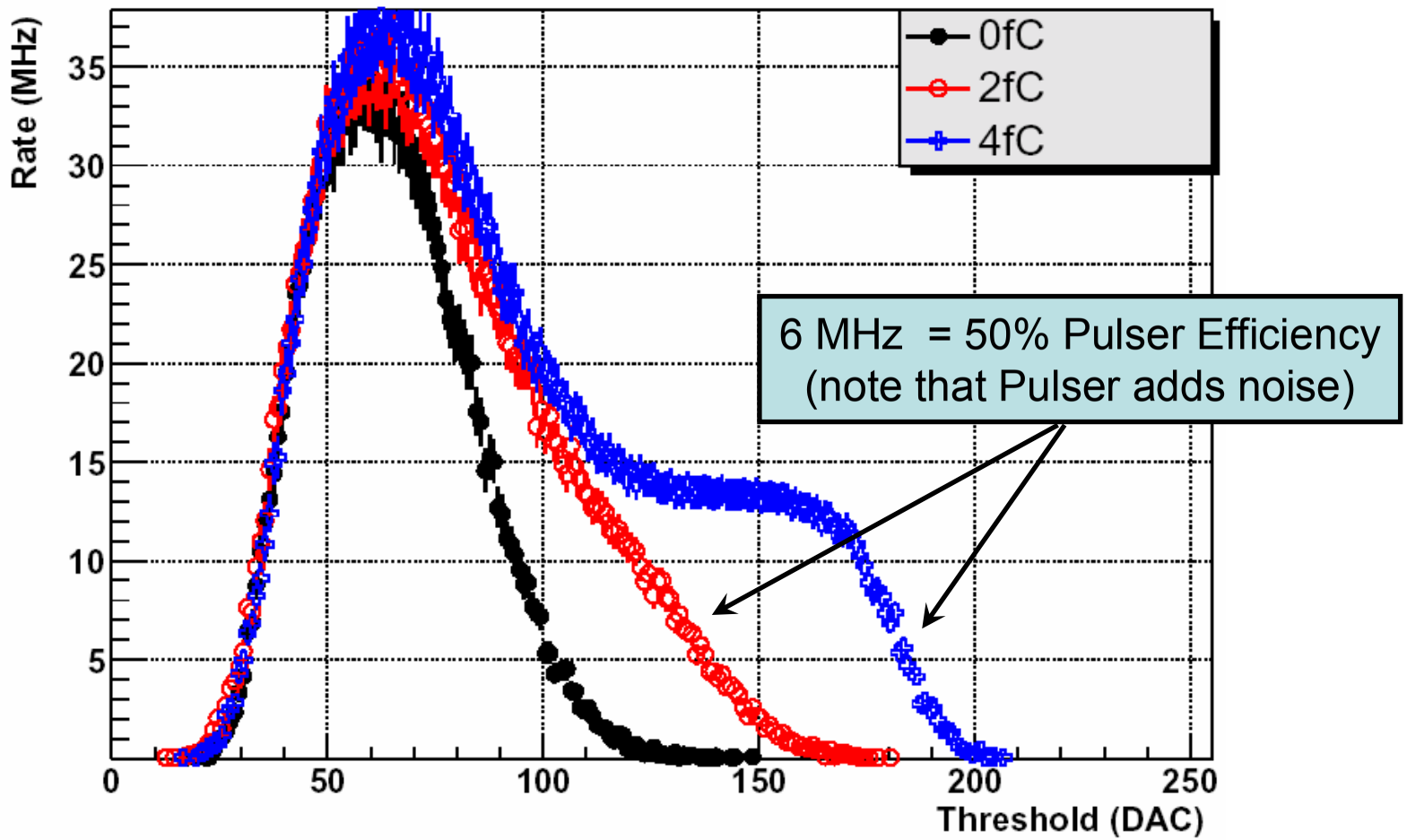


# Noise Rate Plot with Barrel ModuleBoard and Pulser

ATLAS TRT
FEE2003



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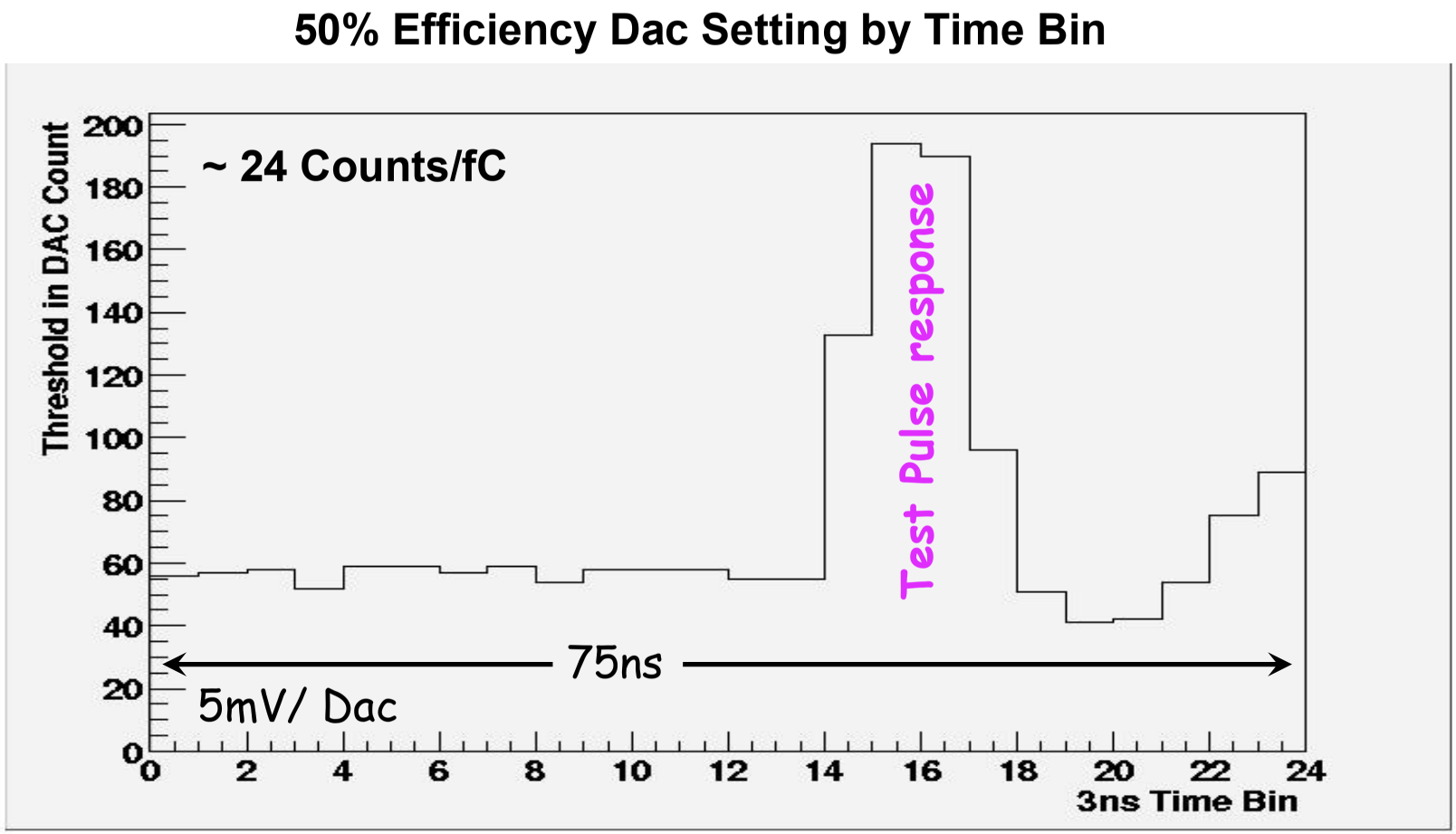
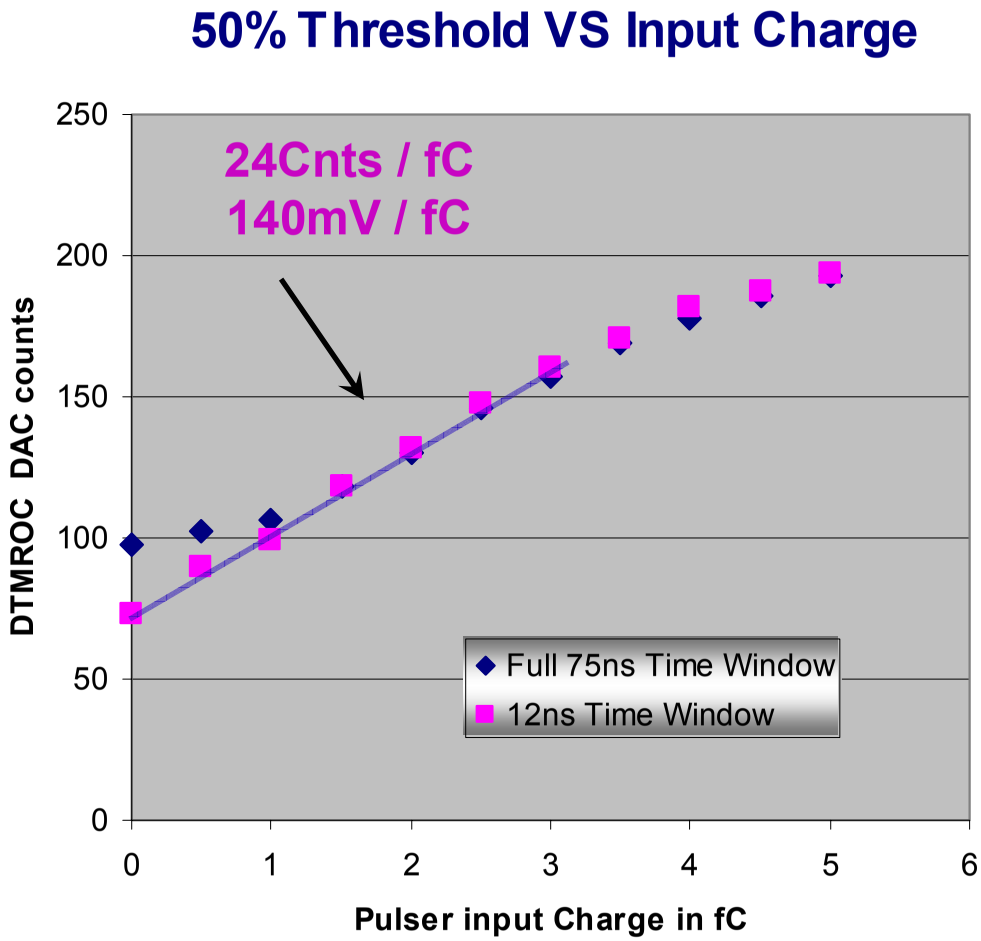
# Analog and Digital Readout on the Barrel Module Board (good Channel)

ATLAS TRT
FEE2003



# Beating Down Pulser Noise using DTMROC Timing window

ATLAS TRT
FEE2003



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# Test Beam Measurements Spatial Resolution

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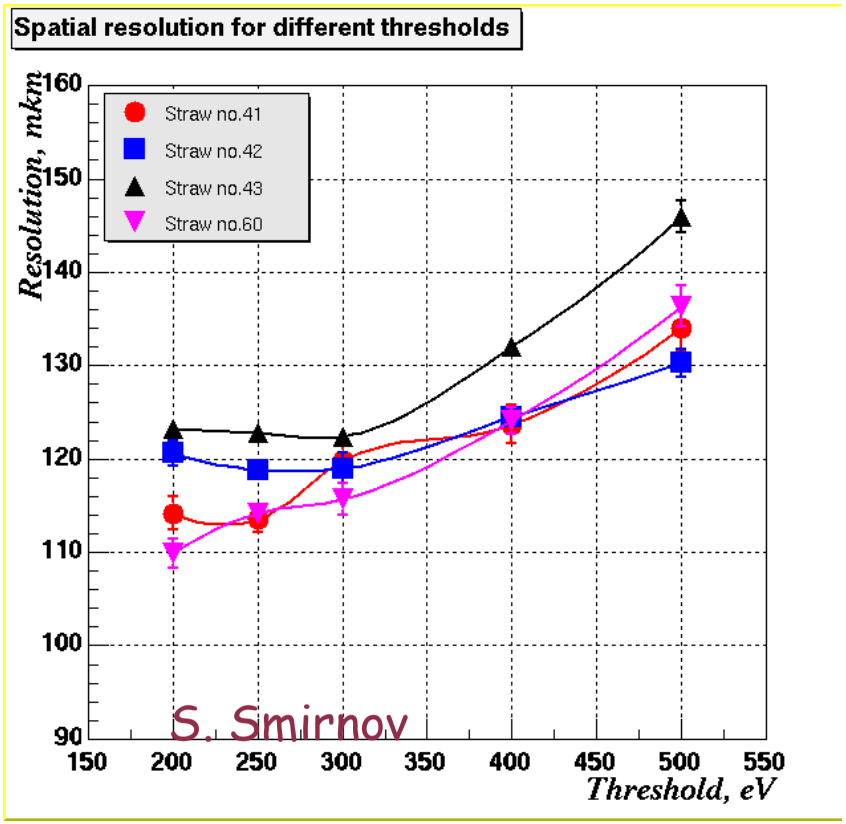


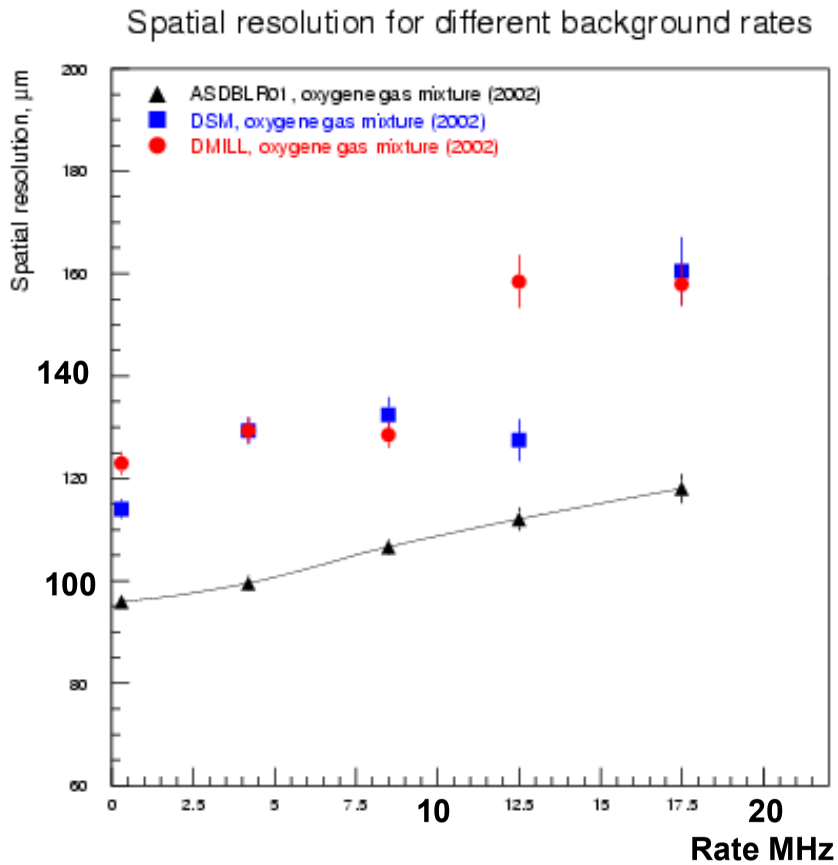




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# Test Beam Performance of Production ASICS and near final prototype boards.

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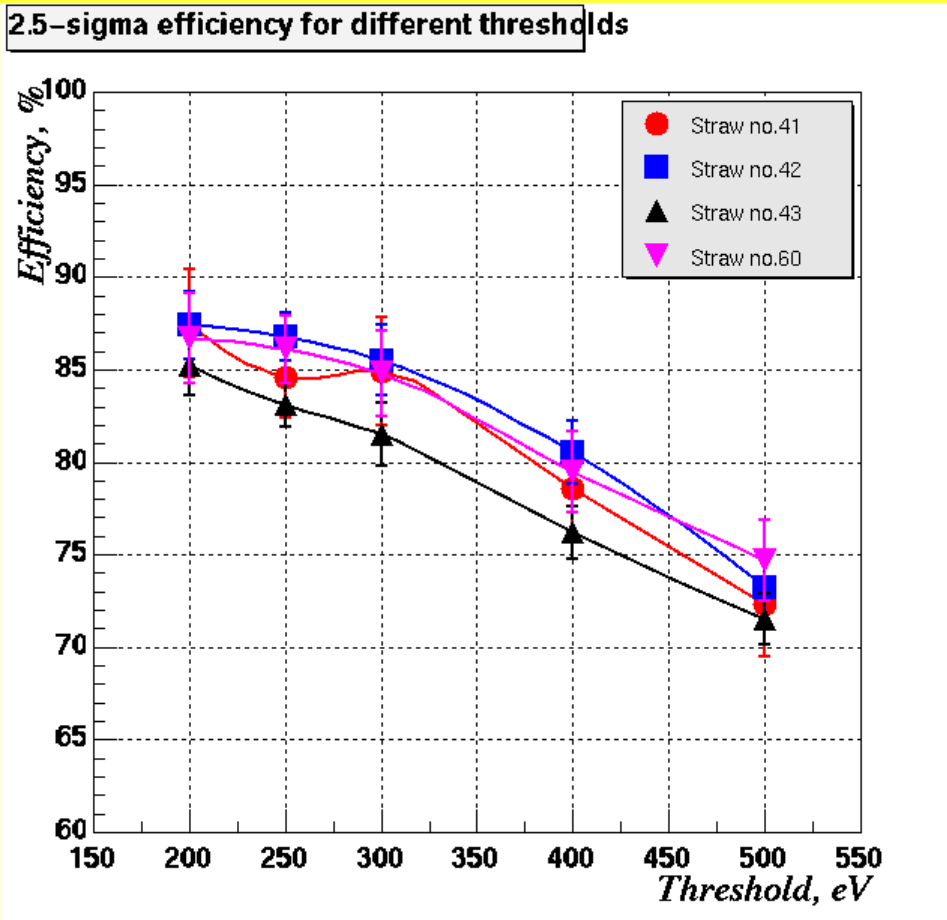


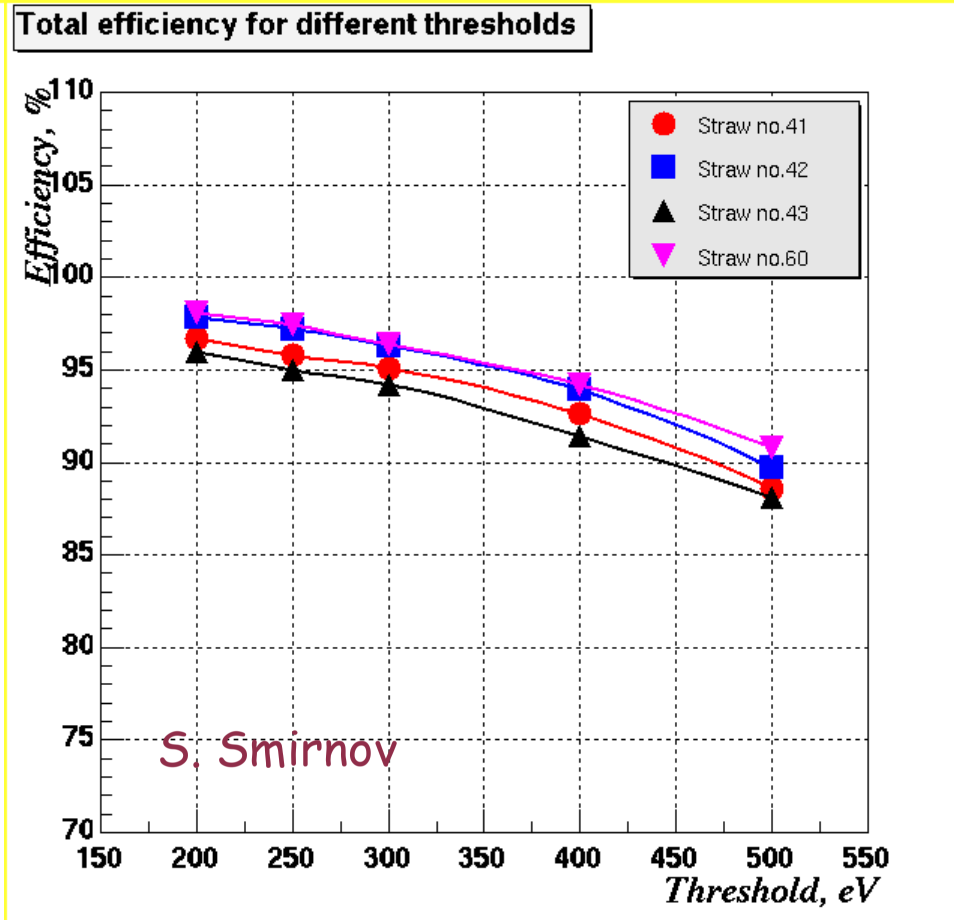



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# Summary

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- **ASDBLR** and **DTMROC** ASICs are in production and have been shown to meet TRT design objectives.
- Development of Production ASIC Testing Facility is nearly finished.
- Design of Boards with both analog and digital ASICS on them is underway and we have very promising results to date.
- Radiation Testing of ASDBLR ASICS indicates npn neutron sensitivity that may limit lifetime to ~8 years when safety factors are considered.
- Thermal neutron content of TRT environment needs study.