ABCn  Driver Receiver and Shunt Blocks
a Preliminary Look

Nandor Dressnandt
Mitch Newcomer
Devyn Schafer
130nm Transceiver

Separable Digital Logic power.

OUTPUT CURRENT CONTROL

\[\begin{array}{c|c|c|c}
\text{Output Current Set} & 06 & 12 & 30 \\
\hline
X & X & X & 2.5mA \\
X & 0 & X & 2mA \\
\end{array}\]
Major Transceiver Sub-Blocks

* < 20 Ω port res.
  0-3mA driver
  Rcvr 0-1.2V CM

POWER
Rcvr 330uW
Driver 1.5mW + drive current pwr
Rail to Rail Receiver
Driver
Driver Common Mode Adjust
Common Mode Range @160MHz  Vdd=1.2V

Input  Hi Z  
± 75mV
Common Mode
Input 0 – 1.2V
Output OK over full CM Range

Internal Receiver
OK over Full CM Range

CMOS Digital  Rcvr Output
Expanded View@160MHz  Vdd=1.2V
Mixed TW and Standard Transistor

What is the appropriate Convention for T3 / TW?
Status

• Cadence Schematic entered
  – Finish error checking
  – Recheck process variation/temp
  – Need to run local variation Monte Carlo

• Layout ??
  – Shape preference?
  – With Pads, without??