Serial Power & Protection ASIC for
1 to 2.5V Hybrid Operation

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Serial Power and Protection ASIC

Independently powered remote and local SP control.

- Addressable “off” “on” commands by hybrid.
  - Expandable command set.
- Local Band Gap for autonomous hybrid regulation.
- Single Line for power and command.
- Provides control for distributed shorting and shunt regulation. Robust against single device failures.
- Autonomous hybrid shut-down on Over V condition.
Serial Power & Protection Block

** “External FET gate” to accommodate Shutdown mode when used with ABCn**
Four Module Serial Powered Hybrid Sim Model

10-256 Ch ABCn 130

250mA Current Spike @ 200uS

1.6A Current Source
Ten 256 ch ABCn 130nm

ABC 130 Behavioral Model

Behavioral Model of 256chan ABCn 130nm current
Analog 20mA Digital 55mA for 128 ch chips @ 1.2V Switch in Trigger Current

Shunt Switch

Shunt Regulator Slave

Cntrl

Pulse(0 3 230u 50n 50n 100n 500n 5)
I*e(0.015v(vraw.Lciref)**2) 
.model smplSW SW (Ron=1 Roff=1meg Vt=1 Vh=-1)
I*min(1(vraw.Lciref)-1)**.032_086)
I*0.7v(vraw.Lciref)**2 + .004v(vraw.Lciref))
Serial Power & Protection (2.4V) Logic

XOR

oneshot

Penn
Bandgap Shunt Regulator  Hybrid OV sense

Hybrid OV sense / Latch

1.2V or 2.4V

SPP  Bandgap Regulator with Buffered output

2.4V
Serial Power Shunt Regulation

2.4V

Hybrid Voltage Sense
Fab version will have 1.2 and 2.4 V select

Shunt Control Voltage

1.2V Reference

Dual Output OpAmp
From SPI Design

Shut Down

Serial Power Shunt Regulation
Simulations of a Serial Powered Stave

Objective is to gain experience operating a serial powered system.

- Chose a 4 hybrid sim to maintain reasonable processing time. Only three modules have full addressing logic. Varied ramp up time from 1us to 500us. No problems observed after Band Gap wakeup is fixed.

- Ramp up SPP Voltage $0$-$18V$ first then current source for $ABCn$ $0$-$1.6A$
SPP Addressing & Decoding

Data in

Module 1 Off

Module 1 On

Module 1 On

Penn

10
Absolute Voltages \( V(\text{hybrid}), V(\text{spp}) \)

4 Hybrids serially connected **Normal Operation**

- **Vdd SPP Chips**
- **Ramp Voltage for SPP Reference 10us**
- **Vdd Hybrids**
- **Ramp up hybrid Current 0 – 1.6A**

Graph showing voltage levels:
- **6V**
- **2.4V**
- **4.8V**
- **1.2V**
Serial Power Regulator Block

Values for all 4 Modules relative to their reference Voltage superimposed,
Cascade Failure Hybrid Reference too Low
Vdd hybrid Sense Comparator Input

Hybrid Voltage Sense Comparator Input

Short Mod 1

#1 #2

Short Mod 3

#3

#4

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All 4 Comparators Input

Voltage Spike from Module #1 Shut down Over Reference Causes Other 3 to shutdown.

Solution is to raise threshold External control should be Available in prototype.
Reference Threshold Raised, re-run sim on the 4 modules. Shutdown commands Only affect addressed modules
Currents and Voltages

- Power in SPP Pwr resistor
- SPP regulator Shunt Current
- Current in SPP Pwr resistor
- ABC chip current
- Total ABC current
Status

• Cadence OA schematic entered, simulations underway
• Dual Output OpAmp layout complete, waiting for fully operational OA environment to continue layout.
• Ready for a May submission with the objective of using it on ABCn Stavelet.