B wheel Board Gain Differences

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Motivation

- Gain differences have been observed for a number of B wheel boards from ALGEN.
- Smallest Division ASD ASIC
- Typical - Board or DTMROC

Two boards have been examined in detail.

<table>
<thead>
<tr>
<th>Board</th>
<th>Chip</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>V656</td>
<td>A0053011(d)</td>
<td>Typical</td>
</tr>
<tr>
<td>V660</td>
<td>A0156162(d)</td>
<td>Low</td>
</tr>
<tr>
<td>V660</td>
<td>A0157867</td>
<td>Low</td>
</tr>
</tbody>
</table>

(d) Indicates Chip is oriented below Silk screen diode symbol.
External Pulser Response at BLR Output
for two low gain and two typical channels 4fC
External Pulser $\rightarrow$ BLR Monitor Out

Differential Output at Monitor vs External Pulser Input Charge

External Pulser: Standard 32 channel "odd/even"

Low Gain ASD B wheel board V0660
Normal Gain ASD B wheel board V0656

Input Charge in fCoul

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Internal Pulser $\rightarrow$ BLR Monitor Out

Test Pulse DAC Counts VS Measured Differential Voltage at BLR Monitor

- Low Gain ASD B wheel board V0660
- Normal Gain ASD B wheel board V0656

- DAC Counts
- Diff mV

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Internal Pulser to 50% DAC threshold

Internal Pulser vs 50% Threshold Difference Values
Referenced to Internal pulser Data taken at 5 counts

Range values shown are the difference between measured 50% threshold data and 50% threshold for an internal pulser setting of 5 DAC counts for each channel shown. This helps eliminate offsets in data among channels.
Test Pulse Response at BLR Output
TP Value set to 60 (11fC)
Test Pulse Input to ASDBLR from W0223 Triple Jumper Position #8 to Typical and Low Gain ASD
Preliminary Conclusions

1. Low Gain Channels are \(~10\%\) lower for External pulser and \(~25\%\) lower for the Internal pulser when measured at BLR monitor output.

2. Gain is constant down to \(~1\) fC. Low Gain channels do not present risk that BLR will operate in a highly NL range for near threshold signals.

3. Using the same DTMROC to compare measurements of the whole signal processing chain indicate only a small gain difference between Low Gain and Typical ASDBLR boards. Examination of several chips has shown that the gain difference is relatively constant implying a batch difference.

4. Pulse shapes observed at the BLR output for low gain and typical chips are qualitatively the same from \(2\) fC to \(80\) fC of injected charge.

5. The maximum test pulse range is only about \(12\) fC. Setting the DTMROC BLR bias resistor to a smaller value would increase this range.

6. Low Gain and Typical ASD’s exhibit nearly identical test pulse shapes as observed at the Test pulse input to the ASDBLR.