

Effects of Duty Cycle Variation of 'BX' at PP end of 100m cable

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Mitch Newcomer

Setup

- New TTC
- 100M cable TTC to PP (old and new)
- Test Beam PP with Laia's termination
- Input to AD9687 Dual Comparator
3uA quiescent input current measured with inputs @ 1.2V

Problem - No or poorly shaped clock output from PP LVDS driver to AR boards. (old 100m cable)

Comparator Input and LVDS Output

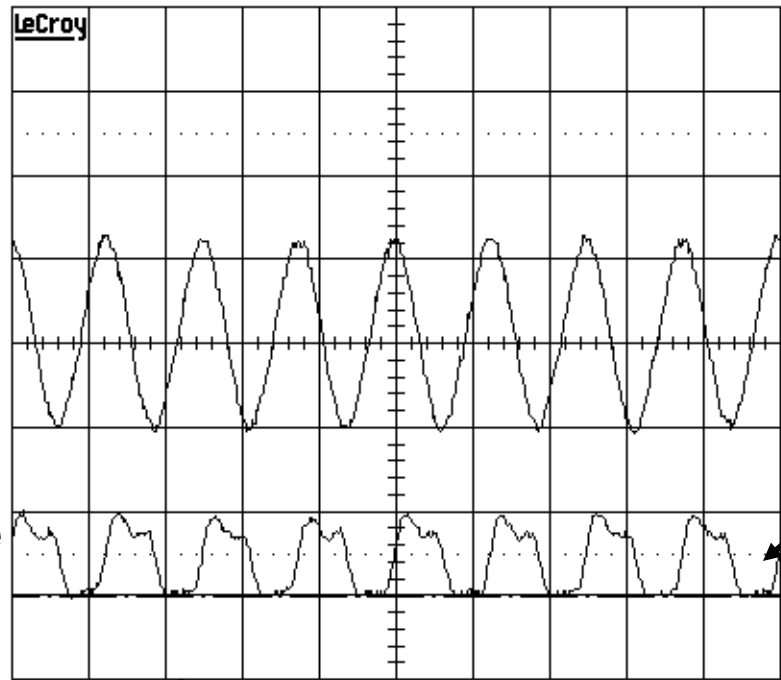
TTC set for 50% Clock Duty Cycle
Old Cable

1-Mar-05
13:32:55

2
20 ns
50 mV
300 mV

3
20 ns
50 mV
300 mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

Note 10X
Scope Probe
not recognized

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only

2 AC 0mV

Comparator Input and LVDS Output

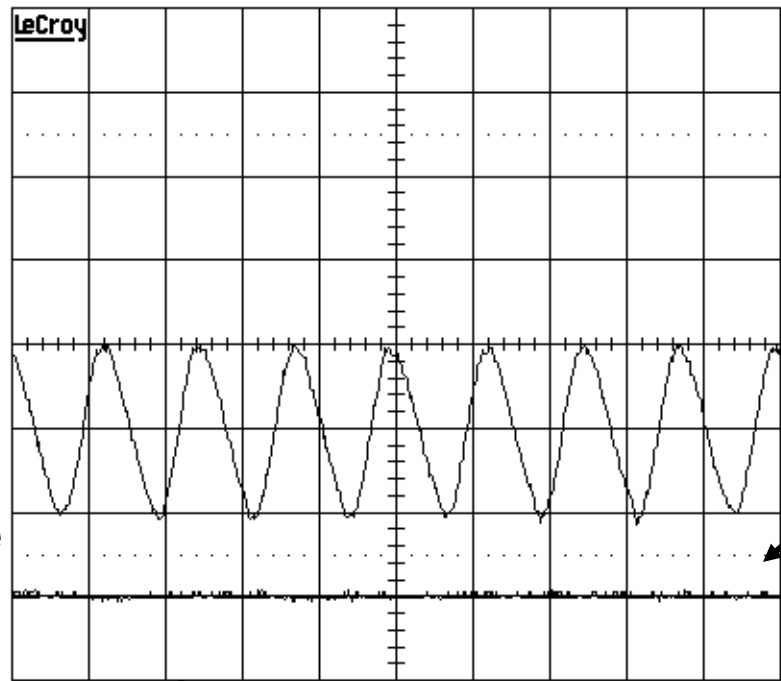
TTC set for 35% Clock Duty Cycle
Old Cable

1-Mar-05
13:33:25

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



2

AC 0mV



Comparator Input and LVDS Output

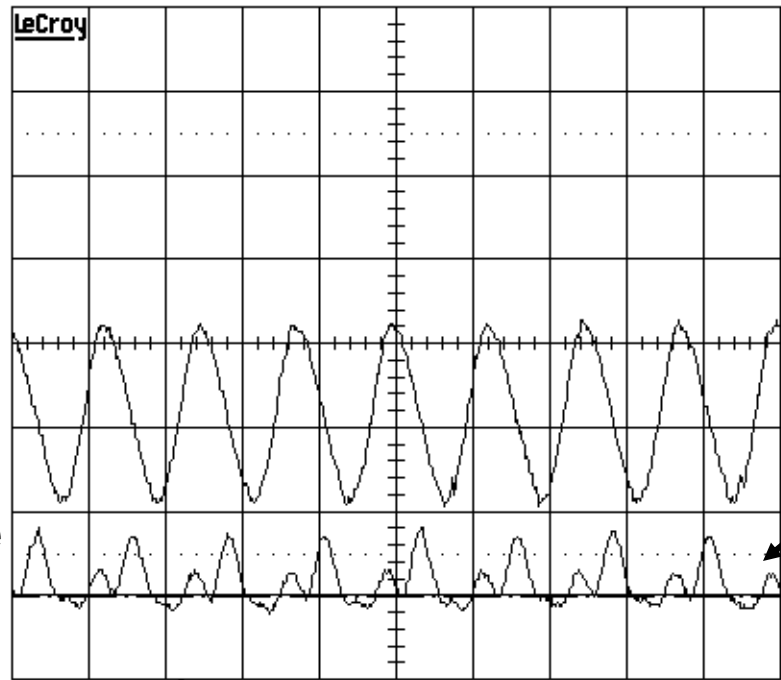
TTC set for 40% Clock Duty Cycle
Old Cable

1-Mar-05
13:34:10

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



2 AC 0mV



Comparator Input and LVDS Output

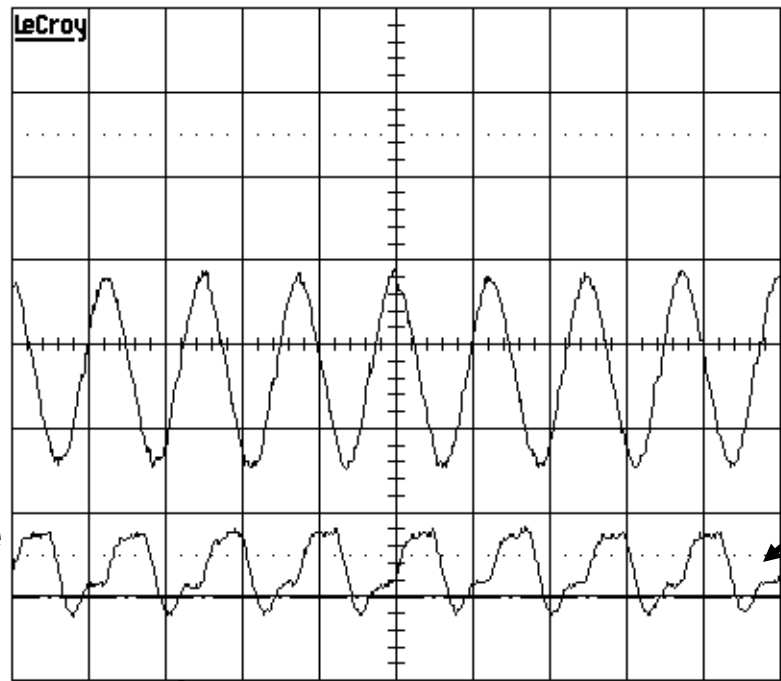
TTC set for 45% Clock Duty Cycle
Old Cable

1-Mar-05
13:35:37

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns
1 trig only
2 50 mV DC
3 50 mV DC
4 trig only

2 AC 0mV

Comparator Input and LVDS Output

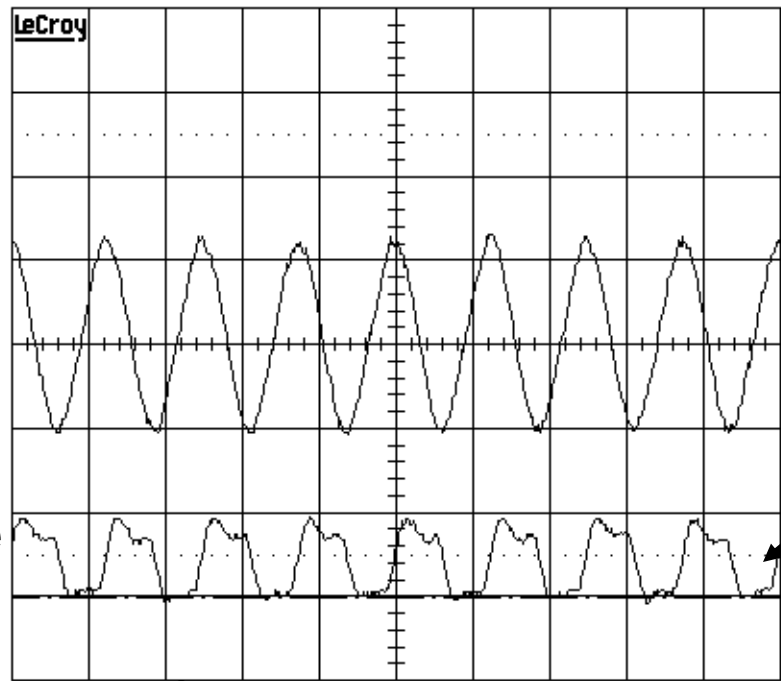
TTC set for 50% Clock Duty Cycle
Old Cable

1-Mar-05
13:36:21

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



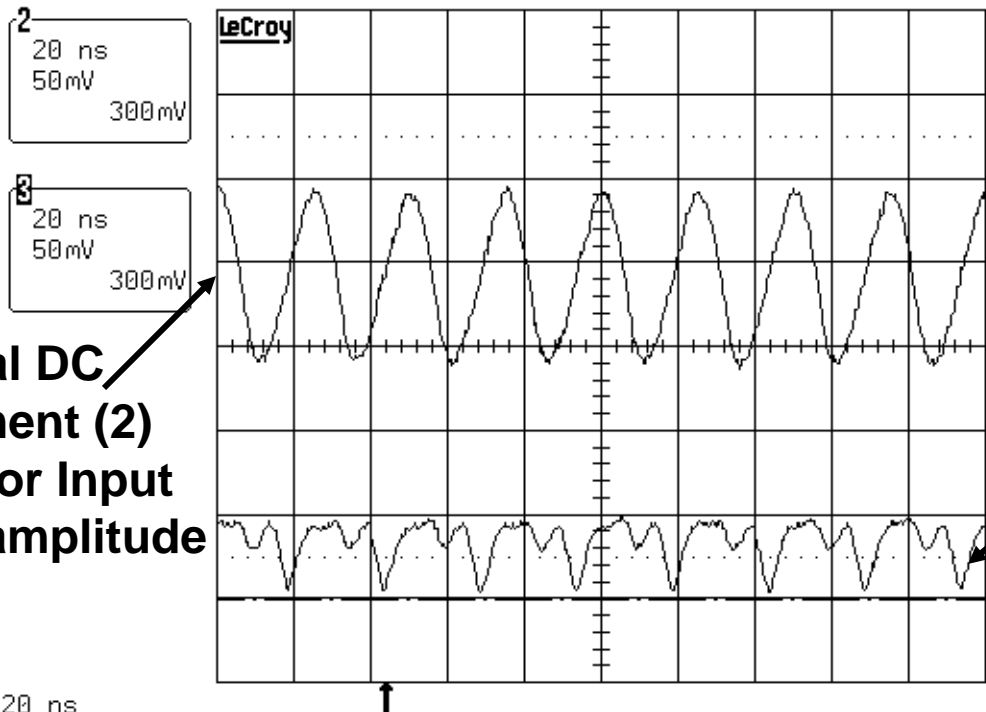
2 AC 0mV



Comparator Input and LVDS Output

TTC set for 55% Clock Duty Cycle
Old Cable

1-Mar-05
13:34:17



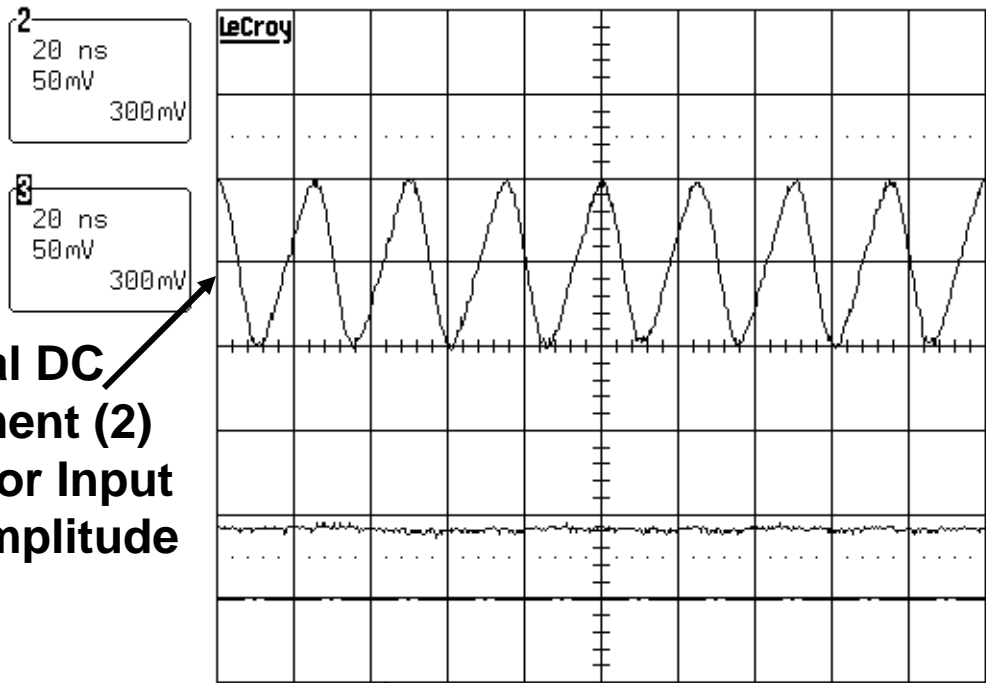
Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude

Single Ended DC
Measurement (3)
LVDS output to AR
Boards

Comparator Input and LVDS Output

TTC set for 60% Clock Duty Cycle
Old Cable

1-Mar-05
13:33:38



Differential DC Measurement (2)
Comparator Input
100mV amplitude

Single Ended DC Measurement (3)
LVDS output to AR Boards

20 ns
1 trig only
2 50 mV DC
3 50 mV DC
4 trig only

2 AC 0mV

Comparator Input and LVDS Output

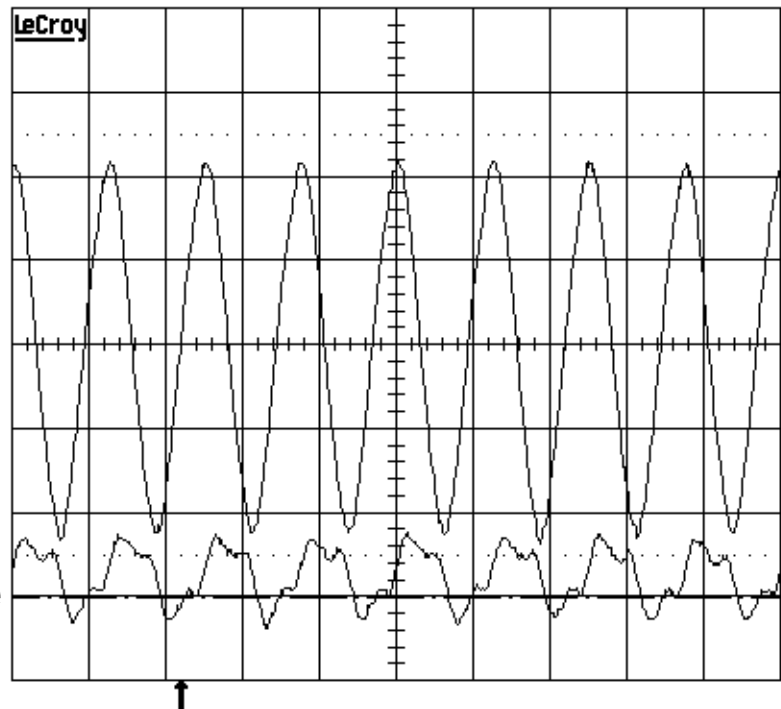
TTC set for 50% Clock Duty Cycle
NEW Cable

1-Mar-05
15:58:21

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC Measurement (2)
Comparator Input
>200mV amplitude
> 2X old amplitude



Single Ended DC Measurement (3)
LVDS output to AR Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



2 AC 0mV



Comparator Input and LVDS Output

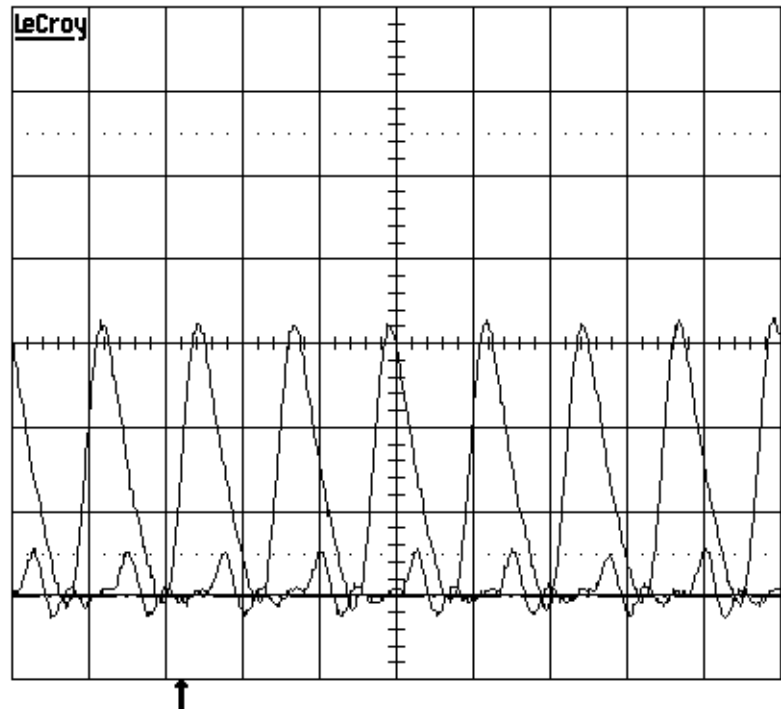
TTC set for 25% Clock Duty Cycle
NEW Cable

1-Mar-05
15:56:47

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns
1 trig only
2 50 mV DC
3 50 mV DC
4 trig only

4 GS/s
AUTO

Comparator Input and LVDS Output

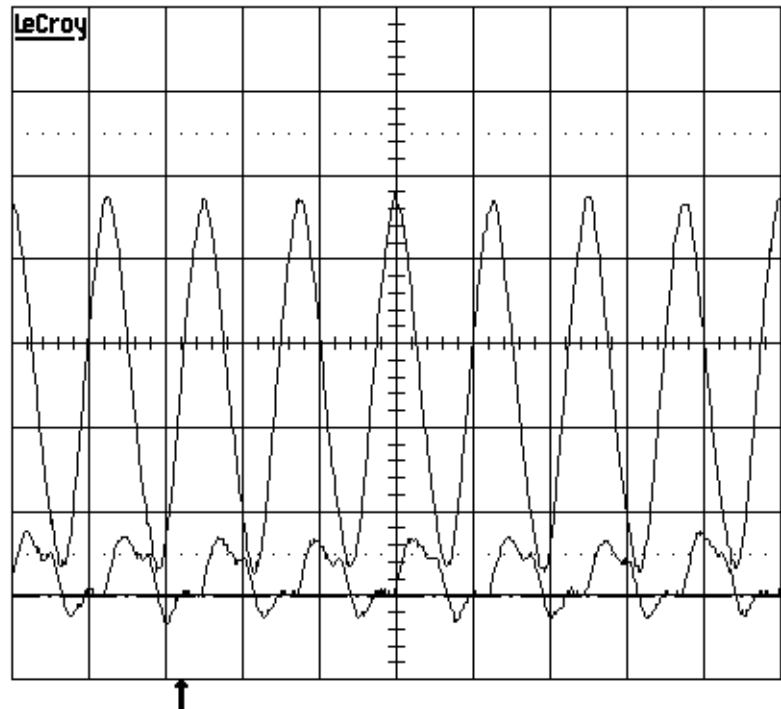
TTC set for 45% Clock Duty Cycle
NEW Cable

1-Mar-05
15:59:44

2
20 ns
50 mV
300 mV

3
20 ns
50 mV
300 mV

Differential DC
Measurement (2)
Comparator Input



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns
1 trig only
2 50 mV DC
3 50 mV DC
4 trig only

Comparator Input and LVDS Output

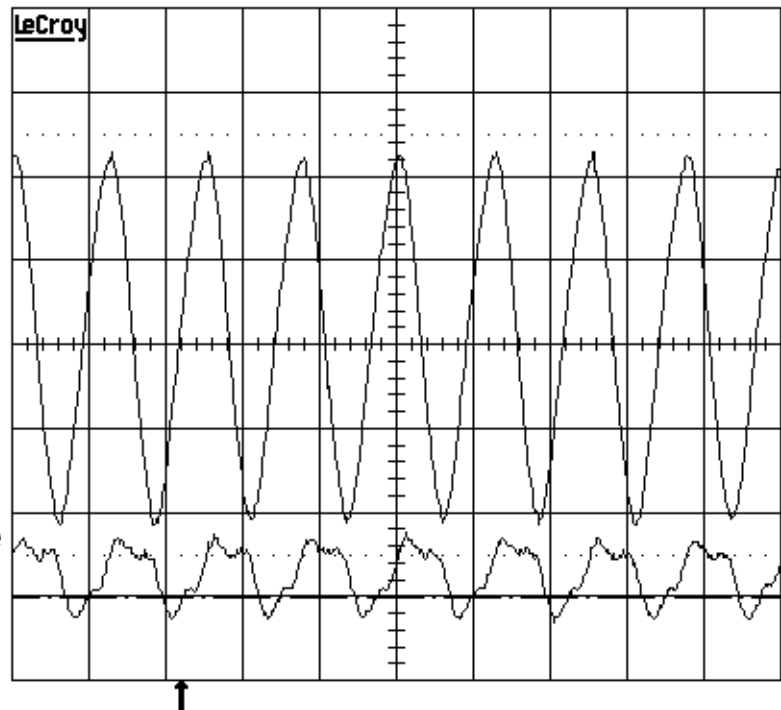
TTC set for 55% Clock Duty Cycle
NEW Cable

1-Mar-05
16:01:12

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input
> 100mV amplitude



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



2 AC 0mV

4 GS/s

AUTO

Comparator Input and LVDS Output

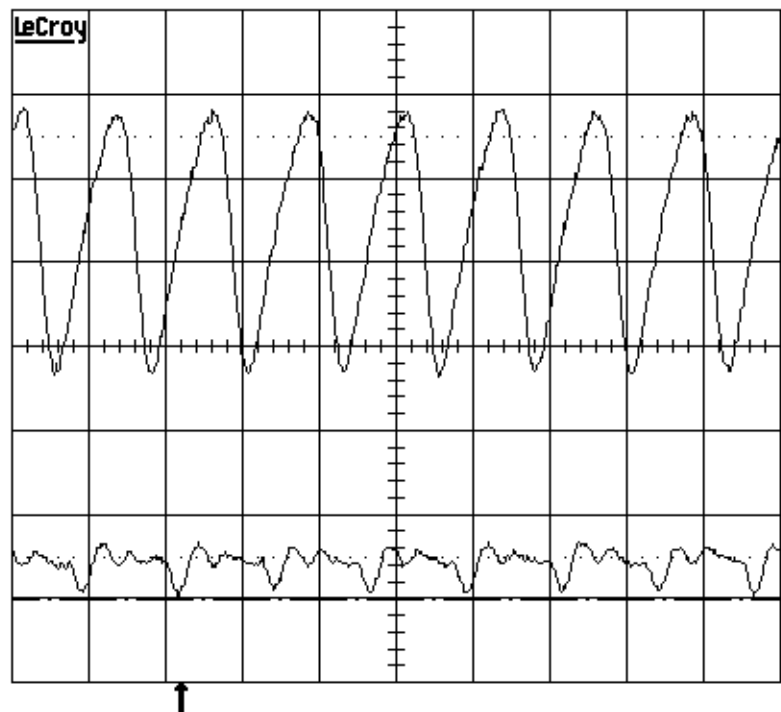
TTC set for 70% Clock Duty Cycle
NEW Cable

1-Mar-05
15:57:06

2
20 ns
50mV
300mV

3
20 ns
50mV
300mV

Differential DC
Measurement (2)
Comparator Input



Single Ended DC
Measurement (3)
LVDS output to AR
Boards

20 ns

1 trig only
2 50 mV DC
3 50 mV DC
4 trig only



2 AC 0mV



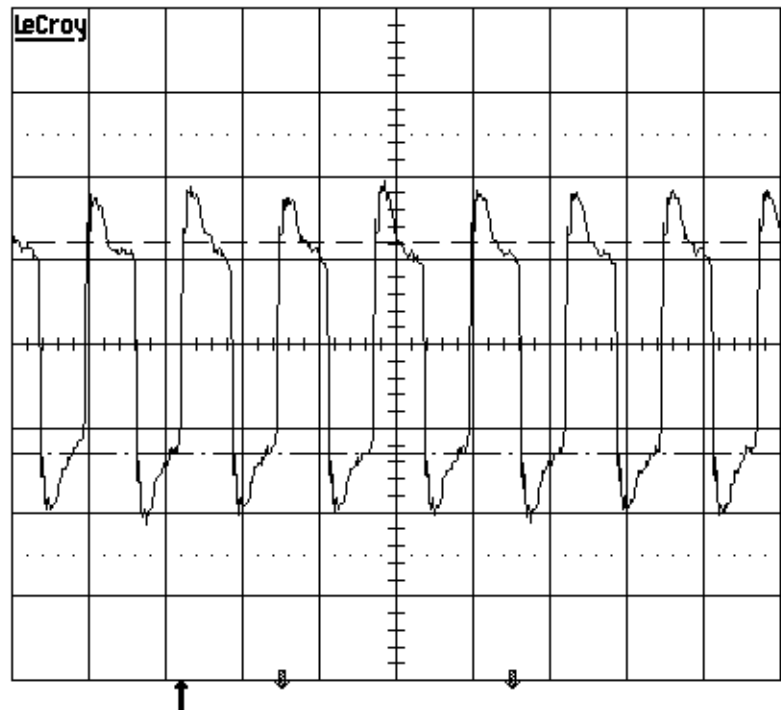
Comparator Differential LVDS Output

TTC set for 50% Clock Duty Cycle
PP LVDS Out

1-Mar-05
16:04:29

2
20 ns
200mV
501mV

Differential DC
Measurement (2)
PP LVDS
Output drive



20 ns

1 trig only
2 20 mV DC \times
3 50 mV DC
4 trig only



2 AC 0.000 V



Preliminary Conclusions

- The DC level for the clock may be varied by +/- 150mV by varying the duty cycle while DC connected.
- New cable has 2X larger signal at PP end. This certainly helps, but does not eliminate sensitivity to DC offsets at receiver end.
- We need to understand the implications for both 'BX' and 'CMD IN' signals and perhaps re examine the types of cable termination or drive that we are using.
- An **AC** coupling may be appropriate for BX between TTC and PP.