ATLAS TRT
Front END Board Debugging Guide
with a detailed look at
Critical Components on AR1FS

Mitch Newcomer
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**Note that this is a work in progress and will be
updated from time to time. Example plots for a variety
of detected problems may be found at:

higgs.hep.upenn.edu/systest/TRT/dsm/dev/GALLERY
Introduction

Penn has assumed responsibility for repairing TRT front end boards that fail basic test programs at Neils Bohr Institute where “burn in occurs and at CERN where boards are tested prior to installation on the TRT detector. There are 15 basic front end board types that all use the DTMROC and ASDBLR chip set, so while board topology is different, the chip set remains the same and therefore there is a significant overlap in the debugging and test approach.

The largest difference between board types is between the End Cap Wheel boards (~200,000 channels) where the chipset is split with the Analog signal processing being done on ‘A’ and ‘B’ wheel boards and the readout and control being done on a ‘triple jumper board.

This manual will begin to inform people involved with testing and debugging about tests and expected responses from the chipset.
ASIC Triplet (ASDBLR)

- **ASDBLR** 8 dual input, dual output channels (2 per triplet)
- Supply Voltages - +3V - 3V
- **A and B inputs** - input Voltage ~.7V  Input Resistance ~26kohms
- **Two Thresholds** - Low, High level threshold. Usually one is held fixed while the other one is ramped by test programs.
  Threshold input range 0 – 1.25V. (set by DTMROC)
- **Outputs** - Differential three level encoded output  No Lo Hi output.
  Two, fixed 200uA currents are switched between the two outputs

<table>
<thead>
<tr>
<th></th>
<th>P Out</th>
<th>N Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>No</td>
<td>400uA</td>
<td>0</td>
</tr>
<tr>
<td>Low</td>
<td>200uA</td>
<td>200uA</td>
</tr>
<tr>
<td>High</td>
<td>0</td>
<td>400uA</td>
</tr>
</tbody>
</table>

**Test Pulse** - Two inputs are used to strobe Odd and Even channels on the chip. Each channel couples to the test pulse line through a 200fF capacitor and 4K ohm resistor in series. If the capacitor is shorted internally the test pulse input will have a resistance to gnd of ~ 10K ohms
# ASIC triplet (ASDBLR)

## Continuity Tests

<table>
<thead>
<tr>
<th>Signal</th>
<th>Resistance</th>
<th>PWR Up Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, B inputs</td>
<td>24 – 28 K ohm</td>
<td>.7V</td>
</tr>
<tr>
<td>Threshold (Hi, Lo)</td>
<td>Diode Protection</td>
<td>1.28 (dtmroc) @ 1uA</td>
</tr>
<tr>
<td>Outputs</td>
<td>Diode Protection</td>
<td>Diode Protection</td>
</tr>
<tr>
<td>Test Pulse</td>
<td>Should be Open</td>
<td>~ 2.5V from DTMROC</td>
</tr>
<tr>
<td>Shaper Control</td>
<td>Diode Protection</td>
<td></td>
</tr>
</tbody>
</table>
ASIC Triplet (DTMROC)

- **DTMROC** –
  - Supply Voltage 2.5V (+/-0.2V)
  - 16 Differential Ternary Channels input.
  - 4 SE Threshold Outputs.
  - 2 SE Test pulses (odd and even).
  - Clock Differential Low level input.
  - CMD IN Differential Low Level.
  - Data Out Dedicated Single line to Patch Panel.
  - CMD Out Tri-State.

**CONTINUITY TEST**

- Diode Protection
- 5K ohm output Resistance
- 7.5K Output Resistance
- Diode Protection
- “ ”
- “ ”
- “ ”
- “ ”

Nominal Threshold Voltage output is 5mV (1uA into 5K) per DAC count. The default power up is a max DAC setting of 255 (~1.25V).
## DTMROC

### Continuity Checks

<table>
<thead>
<tr>
<th>Description</th>
<th>Resistance</th>
<th>Voltage/Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 Diff Ternary Inputs</td>
<td>prot. diode</td>
<td>~ -100mV</td>
</tr>
<tr>
<td>4 Threshold Outputs SE</td>
<td>5K Ω</td>
<td>Pwr up ~1.25V</td>
</tr>
<tr>
<td>2 Test Pulse Output SE</td>
<td>7.5K Ω</td>
<td>~ Vdd (2.4V)</td>
</tr>
<tr>
<td>CMD IN</td>
<td>100Ω on bd. /diode</td>
<td>1 – 1.5V</td>
</tr>
<tr>
<td>Clock (BX)</td>
<td>100Ω on bd. /diode</td>
<td>1 – 1.5V</td>
</tr>
<tr>
<td>Data Out</td>
<td>120Ω on bd. /diode</td>
<td>1 – 1.5V</td>
</tr>
<tr>
<td>CMD Out</td>
<td>100Ω on bd. /diode</td>
<td>1 – 1.5V</td>
</tr>
</tbody>
</table>
Ramping Programs

Board Ramping Programs -- ‘thrater’ ‘tpscan’ ‘tphigh’

Each DTMROC has 4 programmable D/A converters used to set thresholds in the ASDBLR. These Threshold D/A’s are ramped over values (max 0-255) and the number of times that a Ternary Output over threshold is detected is logged in a histogram. Additional information such as the Common Program Ramp controls - start value, step size, number of steps

These control the speed at which the program will operate. For a detailed examination of channel behavior set step size to 1 and number of steps to be > 100 as required.

thrater -- ramp ‘low’ threshold with no input signal.
tpscan – ramp ‘low’ threshold with constant test pulse input.
tphigh – ramp ‘high’ threshold with constant test pulse input.
thrate
Sample Output

Typical

Unexpected Data on Ch 0, 1

Good

Good Rate Plot
thrate

HOS
High offset

Low offset OK
Borderline High Gain

HGL
Large High Gain

LGL
Large Low Gain
Probably input short
Very low response all channels. Missing preamp 4.7Ω supply filter resistor.

Candidate short on threshold line Of one ASDBLR (either threshold)
One Test pulse line shorted Several Log gain channels.

Ternary Output open

Low offset channel
tpscan

Typical ‘A’ or ‘B’ wheel TP even SCAN

Test Pulse Line Shorted on Two ASDBLR ASICS at same Location
tphigh ramp

Typical ‘A’ or ‘B’ wheel response

Channel  | 12  | 14  | 1625  | 200  | 150  | 100  | 50  | 0
Threshold (DAC)  | 5  | 10  | 20  | 25  | 20  | 10  | 5  | 0

Hits
DTMROC ‘CMD Out’ based Programs

Test_vt nn - nn board specific name
readout on chip voltages and temp.
DLL_lock boardname.txt - test DTMROC DLL
Board Test Flow

Receive Board – Log into www database,
Create local log text file:
~systest/TRT/dsm/dev/repair_log/boardtype/boardserial#.txt
Locate Board in CERN DB read comments and log summary into local file. Decide on first action:
Repair → Board goes to Godwin with a note
Test → Diagnosis uncertain, Board goes into ‘to be tested’ box

Local Test Suite - ‘thrate’ ‘tpscan’ ‘tphigh’ ‘test_vt’ ‘DLL_lock’
report test results in log. ‘OK’ if board is within limits.
copy ‘test_vt’ result into log.

Passing boards - put ‘board passed’ and date on top line of local log.
write board number on sheet in box.
put summary of local log including test_vt result into visual inspection comments in CERN database.

Ship Board - Log shipment and date into CERN DB
Basic Ramp Program Passing Criteria

**thrate** - no channel lower than 25 counts from chip wide ‘eye-ball’ average. No channel higher than 12 counts above chipwide average. No channels always ‘OFF’ or ‘ON’.

**tpscan** – no channel lower than 30 counts from chipwide average.

**tphigh** – no channel always off or always on. No more than one channel with significant differences >15 cnts in response.
Active Roof Board Testing

• AR1FS, AR1BS AR1FL, AR1BL
• AR2FS, AR2BS AR2FL, AR2BL
• AR3FS, AR3BS AR3FL, AR3BL

These are triangle shaped 14 layer boards that house the DTMROC and ASDBLR asics. They require special cables for the data lines, between the data connector and the patch panel usually labeled as specific to a board type.

32 boards of each type provide the front end readout of the TRT barrel
AR1FS Active Roof Board Debugging Guide

• Diagnostic test programs often indicate symptoms that are not sufficient to uniquely identify board problems. This guide provides expected measured values at key locations on AR1FS for chip and board control functions. Since all active roof boards use the same ASIC triplet, values will be the same for all boards although topology will be different. It should be a simple matter to identify locations on other boards by using silk screen indicators and measured values from this guide to match up with locations on the board of interest.
AR1FS  DTMROC Side UP

- Vertex
- Termination area
- Power Connector
- DTMROC #1
- Data Connector
AR1FS Termination Area

Each Leg of the termination resistors connects through a 50 ohm resistor to a common node. BX, Cin have a 0 ohm in series with 50 ohms.

Cin +,- .86V, 1.2V
BX +,- .99V, 1.02V
Reset +,- .88, 1.2V

TEST (pwr off) across +,- nodes
Without data cable plugged in 100 ohms. Test at far end of Cable for full continuity test
Add ~ 20 ohms for cable.

Cout +,- 1.12V, 1.13V
Two 60 ohm resistors to independent node.
TEST (pwr off) Across +,- connection
data cable unplugged 120 ohms, plugged to patch panel = 60 ohms
AR1FS (top) DTMROC Control

Stuffed, (Meas Res), Pwr up Voltage to gnd.

TP Bias 18k, (16k) 1.13V
TP Even 10, (7.5k) 2.4V
TP Odd 10, (7.5K) 2.4V
Lo Th 1 1k, (6.5k) 1.3V
Hi Th 1 1k, (6.5k) 1.3V
Lo Th 0 1k, (6.5k) 1.3V
ADJ12 1k, (7.9k) 0V
Hi Th 0 1k, (6.5k) 1.3V

Xenon Select 1k, (11.8K) 0V
(location varies side to side of DTMROC)

Data Out Resistor
120 ohms Data Connector “off”
60 ohms Data Connector “on” and attached to PP

Pos # 5

Active Roof Repair Aids
**AR1FS (top) DTMROC Control**

Pos # 8  In other layouts Threshold resistors can be here

- TP Bias 18k (16k)
- TP Even 10 (7.5k)
- TP Odd 10 (7.5K)
- Lo Th 1 1k (6.5k)
- Hi Th 1 1k (6.5k)
- Lo Th 0 1k (6.5k)
- Hi Th 0 1k (6.5k)
- ADJ12 1k (7.9k)

Xenon Select 1k (location varies side to side of DTMROC)
1FS Bottom Side Resistors

Stuffing errors that affect the performance of a whole ASDBLR ASIC.

4.7 ohm Preamp Filter Green box.
Lo gain Thresh. Ramp
No test pulse response.

12K ohm Ternary Output reference Red box
Outputs always high if missing.
Board Level Problems

Communication:

BX (40MHz clock) or CMDIN or Reset not present
look for double termination resistance on the PP (~66Ω)
(see PP connector sheet)
CMD OUT missing look for double termination at PP
ASDBLR chipwide problems

1. Symptom - very low gain, low noise all channels.
   PROBLEM → Unstuffed 4.7 ohm resistor. Check preamp input pins for expected value of ~700mV, if resistor is not stuffed, expect ~0mV.

2. Low or no gain on one channel of the ASDBLR - low value of test pulse resistor. ASDBLR test pulse capacitor short. Replace 10 ohm resistor on DTMROC side with a capacitor. The channel with a broken capacitor will be very sensitive to the test pulse. This will still “pass”.
DTMROC associated Chipwide Problems

1. **No response from Chip** - check for double termination at DTMROC chip. Locate (only) 120Ω resistor near corner of DTMROC often visually near a pair of top side traces that take the data out lines to the data ‘NAIS’ connector. With data connector to PP attached find ~ 60Ω If not, then data line is open. OR see if voltage agree with nearby chip.

2. **RAMPS always HIGH** - Quite likely that either high or low threshold is non responsive or shorted to gnd.

3. **No Test Pulse odd and even** - missing/open/short TP bias (18K) resistor.

4. **No test Pulse even or odd**
   a. TP line short
   b. TP filter cap is much larger than 10pF
   c. 10 Ω jumper resistor missing/open/short
   d. Bad BX / DX program timing offset combination readout selects data from wrong time bins.
ASDBLR
Ternary Current Setting Resistors

**Symptom:** Outputs High for one (or more) ASDBLR’s (Whole Chip)
→ 12K resistor shown (red box) on previous page broken disconnected to ball of ASDBLR.
→ OR - Low Threshold problem shorted to gnd or open.

**Check:**
Measure resistance. 12k? If yes then…
Measure voltage on each side of 12K (+3 and -1.99V)
missing -1.99 V at +3V → chip is not connected or bad resistor solder joint.
one side at – 2.3V → broken resistor or bad solder joint to +3V.
if OK
check 1K threshold resistors for 1.28V on both sides.