ASDBLR: Progress Report on Input Protection and Noise

Update on the Status of DMILL ASDBLR Design
Februray 2002

(Updated Table II March 22, 2002)

Summary - We report the results of recent measurements on the ASDBLR99, 00 and 01 concentrating on comparisons of measured intrinsic noise and input protection among the various fabricated parts. These are viewed as the only significant concerns remaining for the ASDBLR design. We believe that all TRT production criteria have been met and that a production layout can be implemented without further prototyping. For a recent description and performance summary of the DMILL ASDBLR see *Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL Technology* TNS V48, number 4. (p 1239).

History -

The DMILL ASDBLR has undergone two major design cycles and most recently a re-metalization to implement various levels of input protection. The first complete prototype in the DMILL process, the ASDBLR99, met all performance criteria but had lower than expected yield (30-40%) and did not offer the same level of input protection as the original version of the ASDBLR fabricated in MAXIM's analog bipolar process. The ASDBLR00 submitted the following year contained several changes intended to improve yield, input protection and maintain an acceptable level of noise. The fabricated ASDBLR00' s showed improvement in yield and a some improvement in input protection but had significantly higher than expected intrinsic noise. Measurements made in the summer of 2001 showed that the noise could be tracked to a higher than expected input capacitance in the input protection structure. This structure consisted of a parallel array of poly resistors followed by ten large NPN transistors wired in parallel as protection diodes (collector-cathode and base-anode). The input capacitance (18pF) was measured by observing the rise time at the input when connected by a series resistor to a pulser.

In September, 2001 we took advantage of an opportunity to revise the ASDBLR00 design with metal only changes. Only the wiring of the input protection devices was changed. Half of the channels were wired utilizing the NPN collectors as the cathode of the input protection diode and half were wired using the emitter as the cathode. Additional variations were made by wiring different numbers of transistors in parallel. This design is referred to as ASDBLR01. More detailed discussion of input protection can be found in Appendix A.

Measurements on Noise and Input Protection -

The fabricated ASDBLR01 ASICS have significantly lower input capacitance and lower noise than the ASDBLR00. All three ASICS have been measured for noise, input capacitance and input protection utilizing the same setup. The results are presented in Table 1. The ASDBLR01 has comparable noise to the ASDBLR99 and only small differences in noise performance are observed among channels. Emitter protection configurations offer lower capacitance than collector protection with comparable noise and somewhat better input protection capacity. Given that the input protection does not improve dramatically going from the 3E to 5E case (see table), a conservative approach might be to utilize four large diode connected NPN's configured with emitter cathodes. This would make the total input capcacitance ~10pF and improve the protection by 50% over the ASDBLR99. Eliminating

the poly resistors and extra NPN transistors in ASDBLR00 should allow us to reduce the area of the chip by at least 10%.

Table I. Summary of Noise and Capacitance Measurements

	Prot. Type	Emitter Length (μm)	Input Cap (pF)	ENC 0pF (electrons)	ENC 10Pf (electrons)	Protection (Volts)
99	C	180	5pF	1900	2850	1100
00	E	600	18pF	2600	3700	1500
01 3E	E	180	9pF	1935	2900	1300
01 5E	E	300	11pF	1960	2845	1400
01 2C	C	120	8.9pF	1930	2800	900
01 4C	C	240	11pF	2065	2975	1300

The input protection test is performed using a switch to discharge a 560pF capacitor attached on one side through a large value resistor to a high voltage supply and on the other to a 20 ohm resistance connected in series with the ASD input under test. The test is performed while a pulse injector is asynchronously triggering the channel under test. The threshold is adjusted to a 50% triggering efficiency level. At intervals increasing by 100 volts the capacitor is discharged into the ASD input 50 times. Numbers listed in the table above reflect the highest voltage at which 50 discharges did not affect the triggering efficiency. In most cases the channel failed as a short or low impedance to ground. The normal input impedance is ~26KΩ.

Yield-

Significant effort went into improvement of the threshold matching of the ASDBLR00. The gain entering the comparator was boosted by ~20%, the comparator input transistors were increased in size and configured in a cross quad layout and the ground reference for the differential attenuator network at the input to the tracking comparator was eliminated. Table II below, compares the yield of the ASDBLR99 and the ASDBLR01. The top row indicates functional yield placing wide limits on threshold and basic power (±30%) constraints. The second row shows the effect of somewhat tighter limits that are at the upper limit of acceptable and the bottom row shows the yield for the original design goal of ±1/4 fC. The 16% increase in yield can be considered to be largely due to circuit improvements. For production we hope to be able to maintain ±1/3fC.

Table II. Comparison of Yield between ASDBLR99 and ASDBLR01**

Threshold Range		Total Yield	
Low (3fC)	High (30fC)	Asdblr99	ASDBLR01
±1.5fC	±12fC	79%	79%
±0.42fC	±12fC	53%	61%
±0.25fC	±12fC	23%	39%

** Table revised March 22, 2002 to reflect results of recent work attempting to carefully compare data cuts on very similar data sets. High threshold cut is large and not what is finally expected to be used. The table is intended to reflect the differences in yield in the Low or Track Threshold.

Appendix A

Input protection structures – The input protection structure is connected in parallel with the input signal. To ensure fast response, diode connected NPN bipolar transistors are used. Since the quiescent input voltage of the common emitter preamp is regulated by the base-emitter voltage of the input transistor, ≅700mV. Two configurations are possible as shown in **A** and **B** schematically below:

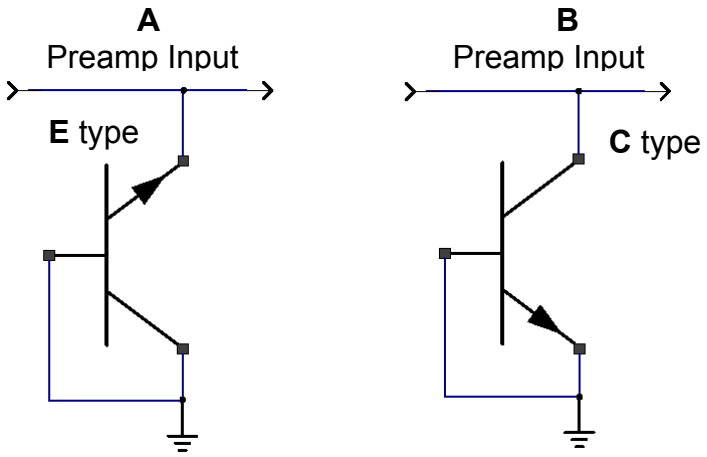


Figure 1 Two configurations of the DMILL NPN transistor used for input protection of the ASDBLR. The large input transistors in the Common Emitter preamp assure that the input will not rise much above 800mV so the potential difficulty of exceeding the maximum V_{be} reverse specification of a few volts is not a problem for configuration A.

In each case the input is protected by a reverse biased PN junction. The collector is usually used for input protection (**C** type in Figure 1). This configuration was implemented in ASDBLR99 utilizing standard DMILL NPN transistors that were stretched to 30um of emitter length (see top figure 3). A total of 180μm of emitter length was used on each input. Physical details of the DMILL NPN transistor structure make emitter protection (**E** type) a potentially favorable implementation. Figure 2 shows the basic NPN layout. Contacts from the two outer stripes connect to the large, trench isolated (outer) rectangle that defines the perimeter of the collector. It is fabricated from n+ material just above the SOI (insulator) layer and has a capacitance of about 800fF/μm^2 to the back substrate. It is therefore a potential node for substrate feedback when connected to the preamp input as in the **C** type input protection**.**

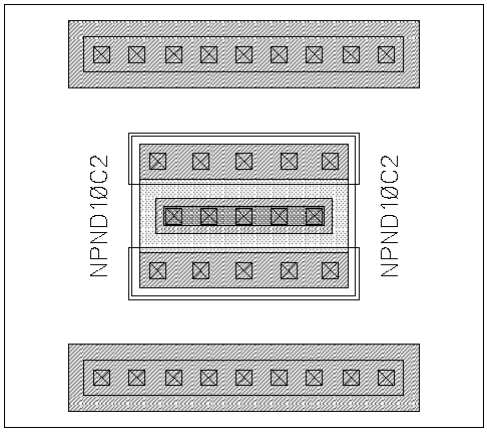


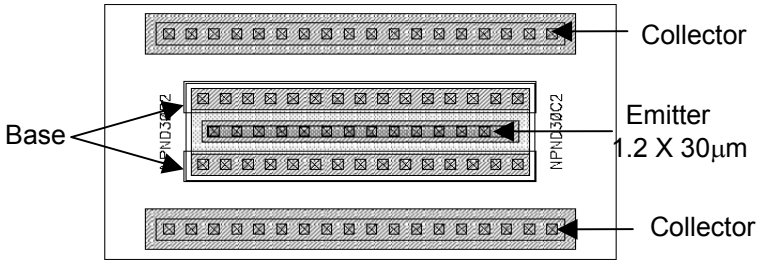
Figure 2 Layout of Standard DMILL NPN transistor. Emitter stripe contact, center, base contact stripes on either side of emitter and collector contacts are the outer two stripes.

The collector is grounded for **E** type input protection and acts as a shield from signals on

the back substrate. Since the emitter lies above the base and collector and is the smallest physical node its only capacitance is to the (grounded) base of the NPN transistor. Its perimeter is shown as the innermost long rectangle in figure 2 above (10 X 1.2μm). As shown in the figure it is usually connected to a minimum width poly stripe and has the disadvantage of having poor current carrying capacity when stretched for input protection.

To better understand the alternatives for using DMILL NPN's as input protection devices we submitted several test structures in a 1999 DMILL multi-project run. Of particular interest to us was the **E** type configuration with a slightly altered the design of the NPN. The width of the poly emitters was expanded from 1.2μm drawn to 3.4μm drawn to increase their current carrying capability and the distance between the emitter and base stripes was increased adding small increase in resistance to help avoid thermal runaway within the device or with several devices connected in parallel. The latter change has the additional benefit of lowering the field between base and emitter for a given voltage. Twenty-one instances of this device were wired in parallel giving an effective emitter length 180μm. Measurements of the fabricated device showed reliable protection against impulse discharges of up to 350μJ, a significant improvement over ASDBLR99 input protection but not enough to be used as stand alone protection. We have shown previously with the ASDQ in a bulk process that it is possible fabricate on chip protection of up to 2.3mJ and decided to attempt similar levels of protection in the ASDBLR00. We utilized both on chip resistance and an increased diode area. A large NPN (shown in the lower part of Figure 3) was designed for the ASDBLR00 input protection to efficiently utilize silicon area and provide good current carrying capability. Ten of these NPN's were connected to the active, (A) inputs and two to the dummy (B) inputs. The NPNs were paired on the A inputs and each pair connected to a large 10Ω poly resistor in series with the input pad. The five parallel input protection structures offered a total of 2Ω of series resistance preceding the input protection and 600μm of emitter protection. A series 10Ω resistor was connected between the input protection structure and the preamp input as a safety precaution to reduce the possibility of oscillation. Unfortunately neither our modeling nor the parasitic extracted netlists showed the magnitude of the parasitic capacitance, about 15pF. The input protection offered was increased by about a factor of two, still less than half of what would be required for stand alone input protection.

Layout of Standard DMILL NPN Transistor
sed for C type Input Protection in ASDBLR99



Expanded DMILL NPN Transistor
Used for E type Input Protection in ASDBLR00, 01

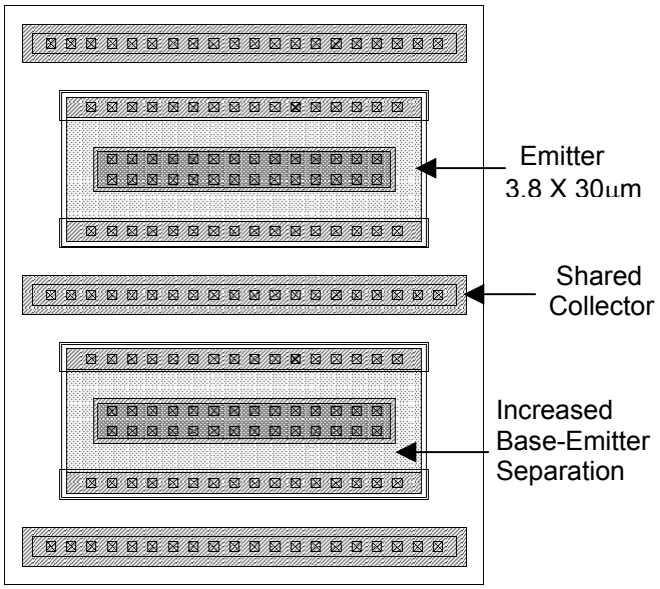


Figure 3 The layout of a stretched DMILL transistor used for input protection in the ASDBLR99 is shown at the top of the figure. In ASDBLR99 the collectors were connected to the input (C type protection). The lower part of the figure shows a revised NPN layout implemented in ASDBLR00 for E type protection. In ASDBLR01 these (lower object) transistors were rewired and configured differently on different channels. Both E and C type protection have been implemented.

ASDBLR01 Input Protection Configurations

As mentioned previously the ASDBLR01 is a rewired version of the ASDBLR00 discussed above. In this version the ten NPN's at each ASDBLR "A" input were selectively wired to test the effect of input configuration type and the number of devices. Four versions were implemented with and without the series 10Ω resistor between the preamp and input protection. The numbers of each type were chosen to match input capacitance. Table III summarizes the configuration and their measured capacitance.

Table III

Channel	#NPN's and Diode Type	Series Resistance to preamp	Measured Input Capacitance
1	3E	0	9pF
2	3E	10Ω	9pF
3	2C	10Ω	9pF
4	2C	0	9pF
5	5E	0	11pF
6	5E	10Ω	11pF
7	4C	10Ω	11pF
8	4C	0	11pF

Channels with the series 10Ω resistance exhibit higher series noise and do not appear to offer noticeable difference in resistance to harmonic disturbances. We do not observe self induced oscillations in any channel at expected operational thresholds.