DESCRIPTION of I/O for the ASDBLR02
Production Version

Power - The ASDBLR has been designed to operate on ±3V supplies. Thresholds are voltage sensitive so care should be taken to keep supplies stable. Although we have characterized the ASIC for ±3V operation, symmetric setting of the supplies between ±2.7 V to ±5V result in acceptable operation. In general the ratio +V/-V should be 1±0.05. The total current required from the positive and negative supplies varies depending on the programmed value of the Ternary and Monitor outputs. The typical power requirement with monitors off and the Ternary outputs set to 200μA is:

 40mW/ch. (~47mA –3V, 57mA +3V, 10mA into GNDA)

Supply	#pads	Description
VCP	2	Preamp positive supply. Both should be used.
VCS	2	Shaper positive supply. 1 may be used.
VES	2	Shaper negative supply. 1 may be used.
VCD	2	Discriminator (comparator) positive supply. 1 may be used.
VED	2	Discriminator negative supply. 1 may be used.
VEDR	2	Output Drive negative supply. Both should be used.

Pads for supplies connect internally across the ASIC we have only utilized the ASDBLR with all pads redundantly connected. It may be possible to connect from only one side.

Grounds - The ASDBLR grounds are separated into analog and digital domains. One bond wire per pad is recommended. Outside the chip a single low inductance ground is expected.

GNDA	8	pads on input side.
GNDD	4	on output side.

Preamp inputs - Inputs are self biasing at ~750mV and have a power up impedance of ~250Ω. Leakage current into input must be less than 1μA. Negative input protection is implemented.

InAx   n=1-8 Active preamp input → straw anode connects here.
             Negative current pulse up to 1pC.   Input capacitance ~ 8pF
             Negative input protection to 0.5mJ
InBx   n=1-8 Dummy preamp input or Positive Input.
             Negative input protection to 0.2mJ
             This input may be useful for Common Mode Rejection on board
             Implementations. Input capacitance ~5pF

Ternary Outputs -   Current outputs may be referenced to any voltage between 0V and +3V. Programmed current can be adjusted from 0 to 1.8mA (typ). 200μA is nominal setting.   Each output has a diode clamp to 0V to accommodate open connections.

tqfp   fbga

OAn or **TRP**n   n=1-8 Positive-going (observed voltage) discri minator ouput.   Open collector drive NPN will release current when discriminator fires. Connects to DTMROC pins TERNxx_T (xx -> 00 to 15)

OBn or **TRN**n   n=1-8. Negative-going(observed voltage) discriminator ouput. open collector drive NPN will sink current when discriminator fires. Connects to DTMROC pins TERNxx_C (xx -> 00 to 15)

PVCDS   Input to set current reference for ternary output currents.
10K sets all outputs to 230µA
11.5K sets all outputs to 200µA   (430µA current)

Thresholds –   Threshold inputs provide a reference for all channels on the chip for the Tracking (Low) and Transition Radiation (TR, High) comparators. Inputs are voltages between 0V and +3V.   Currents are below 10µA pre rad and may be as high as 30µA after neutron irradiation.   The true zero reference (maximum triggering rate) has been adjusted to ~ 100mV for both comparators.

PTH_D   Track comparator threshold input. (~ 720mV for 3fC).
                             Connects to LOWx (x = chip number 0 or 1) on DTMROC.
PTH_TR   Transition Radiation comparator threshold. (~390mV for 30fC)
                             Connects to HIGHx (x = chip number 0 or 1) on DTMROC.

Tail Cancellation Shaping Control Inputs -   Three digital inputs are provided to allow control over the ion tail compensation.   These inputs are protected against static discharge and have 30KΩ internal pull down resistors (to 0V) to assure a determined state when not connected. Current at any input is less than 1µA.

Table 1 Logic Switch point at Vcs = 3V

Low	Typ	High
1.4V *(sf model)*	1.5V *(tt model)*	1.75V *(fs model)*

XESEL - Selects between two shaping stages within the shaper.
PADJS1 – Adds   integration network in collectors of the Second Shaper Stage.
PADJS2 – Adds integration network in collectors of the Third Shaper Stage.
- We expect PADJS1 and PADJS2 to be tied together in most instances. The name PADJS12 will be used as shorhand for the connected pair PADJS1, PADJS2

Table 2 Optimization used for Tail Cancellation Shaping Adjustments

	XESEL	PADJS12
Xe/CO$_2$/CF$_4$ 100%e[**]	Lo	Lo
Xe/CO$_2$/CF$_4$ 50%e[**]	Lo	Hi
Xe/ CO$_2$/C$_2$H$_6$	Hi	Lo
Ar/ .... (t_0 = 1.5ns)	Hi	Hi

** fast component of signal due to electron attachment at wire.

BLBIAS   Adjust current in Baseline Restorer bridge. Diagnostic input. No
                     connection usually.   Nominal voltage ~.8V

Test Pulse Inputs - The ASDBLR partner ASIC, the DTMROC provides two shaped test
pulse outputs. A final shaping stage is integrated into the ASDBLR. No connection to the
ADBLR test pulse inputs is necessary. Inputs are capacitively coupled, 200fF into
each channel.

TST_O   Test pulse input to ASDBLR odd channels.
                     Connects to TP_ODD on DSM_DTMROC.
                     Connects to ODD_OUT on DMILL DTMROC.

TST_E   Test pulse input to ASDBLR even channels.
                     Connects to TP_EVEN on DSM_DTMROC.
                     Connects to EVEN_OUT on DMILL DTMROC.

Analog Monitoring -   A differential monitor output is available on channel 1 and
channel 8.   Each output has an internal pull up resistor of 250 ohms to the positive supply.
Either the shaper or BLR output is available. Outputs are at about 200mV below the positive
supply.

PEN_SH   Pulled high to enable monitoring shaper output. . A resistor may
                     be used in series to reduce currentoutput. Internal resistance of ~ 5K.

PEN_BL   Pulled high to enable monitoring Baseline Restorer on channel 1
                     and 8. A resistor may be used in series to reduce current.
                     Internal resistance to –3V ~5K.

MON_A1   Channel 1 analog monitor positive going differential output.
MON_B1   Channel 1 analog monitor negative going differential output.
MON_A8   Channel 8 analog monitor positive going differential output.
MON_B8   Channel 8 analog monitor negative going differential output.

ASDBLR ASIC   Pad Frame