DMILL ASDBLR ASIC

Basic Design Goals - The ASDBLR is an eight channels ASIC designed to provide the analog interface to the ATLAS Transition Radiation Tracker. The tracker will consist of $4x10^5$, 4mm diameter straw tubes varying in length from about 40 to 80cm. Straw tubes are filled with a largely inert gas mixture that discourages the recombination of ion pairs created by charged particles passing through the straw. The signal is collected on a thin wire (anode) strung axially along the center of the tube, maintained at a positive potential (by the ASDBLR preamp input) with respect to the conductive walls of the straw (cathode). Electrons liberated in the gas by charged particles drift towards the wire at a relatively constant speed. The anode to cathode potential is set high enough that an avalanche occurs as the ionized electrons approach the wire. The avalanche electrons attach to the wire while the heavier positive ions are pulled slowly towards the cathode. The resulting signal current appears as a combination of an impulse of current as the avalanche electrons attach to the wire and a long decaying current induced on the wire as the positive ions move away. The ASDBLR has been designed to detect the avalanche signal induced by 2 to 3 primary ions. A signal shaping network differentiates the leading edge of the input signal and produces an overshoot that exactly matches (cancels) the ion induced current, shortening the signal from many hundreds of nanoseconds to 15-20ns at the base. This enables the circuit to process signals at rates approaching 20MHz. Since the primary ions travel at a nearly constant rate, the time difference between when a track traverses the straw and of arrival of the avalanche signal at the wire can be used to determine the closest point of approach of the track to the wire. To achieve a 150μm position resolution, one nanosecond time resolution is required.

The output of the ASDBLR is a 3 level (ternary) differential current used to indicate an input signal amplitude with two levels of threshold. A low level threshold is set to detect the arrival of the first ions from a track traversing the straw and a high level threshold is used to detect the absorption of transition radiation photons caused by energetic electrons traversing layers of plastic film placed between the straws. Since a very low level of theshold is required to achieve the detection efficiency and position resolution goals, a low noise approach has been used in the design of the ASDBLR. Our present objective is to operate at a signal to noise ratio of about 5:1. This will result in a noise induced trigger rate of between 10 and 50Khz. Since a common threshold is used for all channels it is important to maintain a small threshold dispersion among channels on the chip. Differences of 10% channel to channel at a 2fC threshold would be ideal, but this does not appear to be feasible. A more realistic goal is approximately 20%. The effects of 10 years of radiation displacement damage will lower the gain of the circuits and increase the threshold dispersion. We expect that some channels may have noise induced triggers at rates up to 500KHz.

The functional design goals of the ASDBLR are listed on the table on the next page.

Table 1 ASDBLR Performance Design Goals

Range of typical Signals	2fC – 200fC
Input Impedance	250 – 280 Ω
Shaper Peaking time	7.5ns ±1ns
Width of Shaped Signal at base	20ns
Maximum Overshoot Area	20%
Low Threshold Range	Noise floor – 10fC
Maximum Trigger Rate	20 MHz
Leading edge time resolution	1ns RMS
Min. Detectable Signal, Low Threshold	2fC (12,500e) in 7.5ns
Low Level Threshold Uniformity	All channels singles rates << 1MHz Ch to Ch deviation < .4fC
Minimum Output Width	5ns
Maximum Discriminator Dead time	5ns
Maximum recovery from 1pC signal	500ns
Peaking time for High Threshold Signal	10ns ± 1.5ns
High Threshold Range	10fC – 120fC
Typical singles trigger rate (Noise)	10 – 50kHz
High Level Threshold Uniformity	< 4fC
Channel to Channel Crosstalk	< 0.5 %
Radiation Hardness (10 year total dose)	1.5Mrad and 1x 10^{14} n/cm^2
Power	< 40mW/ch (< 320mW per chip)

Experience with the DMILL process

Initial Prototyping - we participated in two MPW's before designing the first ASDBLR prototype. In 1997 we submitted an Amplifier shaper with programmable shaping time taking advantage of FET's. Then in 1998 we produced a six channel early prototype of the ASDBLR with 3 channels of shaping optimized for a Xenon dominated gas and three channels dedicated to a standard Argon based proportional drift tube gas. These two designs were quite successful and very useful in the subsequent implemetation of our designs.
In February 99 we submitted a series of test structures that included multi-stripe NPN transistors, trial input protection devices and basic structures to study parasitics. This run gave us basic device information that has enabled us to provide significant input protection and helped qualify the multi-striped input transistor that we use for the preamp input.

ASDBLR Designs

ASDBLR99 - In the fall of 1999 we submitted the first full prototype of the ASDBLR, ASDBLR99. Initial tests on the ASIC indicated that it's performance was excellent and that the device met all basic performance goals of the TRT. The functional yield was reasonable at about 80%, but the threshold deviations were much larger than we expected. After applying parametric cuts to the Track threshold data our initial yield was less than 30%. We utilized standard NPN transistors (180μm emitter total) for input protection and found their energy handling capacity was well below our expectations of ~1mJ.

ASDBLR00 - Some potential improvements to reduce channel to channel threshold variation were identified and implemented. These included utilization of cross quad differential pairs at the comparator inputs and the elimination of a DC current flow in the differential attenuator network at the low level comparator input. Several other layout level improvements were implemented as well.

An input protection structure prototyped in the MPW run that appeared to be quite robust was implemented as part of a new input protection network. Input protection was also added to the BLR Bias control line after learning that two chips had failed due to shorts after proton irradiation in the CERN test beam.

This design was submitted in January 2001. The fabricated ASICS were fully functional and had a lower threshold spread, but exhibited excessive noise. The new input protection structure, expanded from the version prototyped in the MPW run was implicated. Destructive tests of the maximum protection offered indicated significant improvement over ASDBLR99 but it still was well below the target of 1mJ. The input capacitance was found to be ~18pF, much larger than the 7-8pF indicated by our extracted layout and other calculations. In retrospect we probably could have been more accurate in the initial calculation. The high input capacitance along with an increase in noise slope over ASDBLR99 (~110e/Pf) due to series resistance in the input protection network caused the noise to be about 1000e higher than ASDBLR99.

ASDBLR01 - ATMEL offered us the chance to submit metal only revisions of the ASDBLR00 design in August 2001. The Input protection was rewired to implement two basic input protection configurations (emitter NPN input or collector NPN input). Four variations of each basic configuration were used to give a total of eight variations on the eight inputs. The value of input capacitance was reduced by approximately half for all channels. Fabricated parts were returned in October 2001 and measurements indicate a significant reduction in the intrinsic noise to levels near that of ASDBLR99. The input protection goal of 1mJ has been dropped in favor of 0.5 mJ which appears to be a realistic goal.

ASDBLR02 - The experience to date has shown that our design is basically robust. None of the deficiencies except input protection has led to a major circuit revision. Within the channel, only one connection in the signal path has been

rewired. In that case a reference to ground was removed. A preamp supply R-C filter was added on each channel in response to a suggestion at the design review. A (final) version of the circuit is nearly completed. Changes from ASDBLR00 include:

1) A final version of the input protection that is much smaller than ASDBLR00 resulting in a reduction of the size of the ASIC from 3.6X3.6mm to 3.6X3.3mm.
2) Increased current in the input transistor (540μA → 710μA). This will make the beta loss due to displacement damage smaller by increasing the current density to 7μA/μm of emitter length and provide a lower intrinsic noise given our higher than anticipated input capacitance.

Our experience with the DMILL process directly relevant to the ASDBLR is summarized on the table below:

Table 2 ASDBLR related fabrications in DMILL

Lot	Date	Wafers	Packaged parts	Description
Z29159	10/99		100 die total 4 QFP's 4 die each	multi-stripe NPN's Input protection
Z31123	12/99	8	1180 TQFP, ~ 100 COB	ASDBLR 99
Z39694	6/01	5	20 CQFP	ASDBR00
Z40313	7/01	8	1393 TQFP	ASDBLR00
Z41258	10/01	7	1099 TQFP 244 FBGA	ASDBLR01

Design Level Tests - Extensive bench testing and studies with charged particle beams have been performed with single ASICs mounted on boards. The ASDBLR has been found to meet the basic design goals as reported above. A high density endcap wheel prototype with 192 channels has been used in the test beam and exposed to a high rate gamma source with a satisfactory outcome. A position resolution of 130μm has been observed at an operational rate of 16MHz.

Production Test Equipment - We have used our IMS automated tester to perform tests on more than 3000 ASDBLR ASICS (and several other versions of ASD's). Data is collected on supply current, output current of the ternary receivers and pulse response. A complete set of tests is attempted on each chip and the data is maintained in a database so that the best devices can be selected for mounting on the detector. For production acceptance testing we would envision setting aside ~50 chips as a "standards" to verify the stability of our test system. These would be maintained for the duration of our production test period. A separate report on ASDBLR production contains more specific information on the production test plan.

Yield - About 80% of the chips tested, independent of generation have all channels functional. As mentioned in the beginning, the most challenging goal

to meet is the threshold uniformity. To maintain an acceptable maximum singles (noise) rate for any channel in the ASDBLR without compromising performance by raising the threshold, we will need to employ a Low threshold cut of about 0.35fC on the deviation of any channel from the chipwide average value. Looking at IMS test data collected from more than 1000 ASDBLR01 ASICS we expect a yield of 53% when this cut is applied and a final yield of 50% when a less stringent threshold uniformity cut of 4fC (maximum deviation from chip average) is applied to High threshold data. This data of course does not tell us what to expect from lot to lot variations.

Radiation Testing –

A significant amount of radiation testing has been performed on ASDBLR circuits. Most has been performed with the ASDBLR99 although recently the ASDBLR01 design has been shown to be quite robust after being exposed to $3.5X10^{14}$ n/cm^2 at Prospero. We have seen three chip level failures on control lines with no input protection. In all three cases an internal short to the negative supply was the cause. The only component common to all three cases is the "polycap" capacitor. It would be useful to know if there has been a radiation hardness study done on it. The Cadence based library part generates a row of contacts just above a trench. We revised this cap for the 16pF of capacitance in the baseline restorer, but have not implemented the revised part anywhere else. Input protection has been added to both lines that failed (BLRBias and VCDS)

Table 3 Summary of Radiation measurements with ASDBLR ASICS

ASDBTR Type	# chips	Power on	Date	Type Dose**	Comments
99	3		4/00	$5X10^{13}$ n	6 loose ASICS exposed without power at Prospero
	3		4/00	$1X10^{14}$ n	Test structures also exposed, NPN beta → 84 and 52
	6	x	10/00	$1X10^{14}$ p	Cern Test Beam 2 ASICS fail due to BLR Bias short
	8		'01	$1X10^{14}$ n	ASICS mounted on endcap boards exposed at Prospero.
	8		'01	$1X10^{14}$ n	No failing channels very little performance change.
	24	x	'01	3Mrad γ	ASICS mounted on endcap boards exposed at CEA Saclay. Very little change. No dead channels.
	6	x	5/01	5Mrad γ	6 ASICs mounted on 3 TB3 boards, one ASIC (5Mrad) fails due to control voltage short. CEA
	4	x	5/01	10Mrad γ	4 ASICs mounted on 2 TB3 boards, all channels remain functional. CEA
01	9		10/01	$3.5\ X10^{14}$ n	9 loose ASICs exposed at Prospero No failing channels, beta → 22 Gain reduced by ~2

** n and p dose is in units of particles/cm^2

Changes in gain associated with displacement damage will result in increased threshold spread that will increase the number of noisy channels. (See separate report on yield.)

Conclusion - We believe that the optimization of the ASDBLR design is complete. Tests have been satisfactory and diverse enough to lead us to believe that there will be no surprises with the design and that our expected yield will be approximately 50% for a well considered set of cuts. Our next step will be to complete the ASDBLR02 design and submit it for a pre-production run.