ASDBLR01

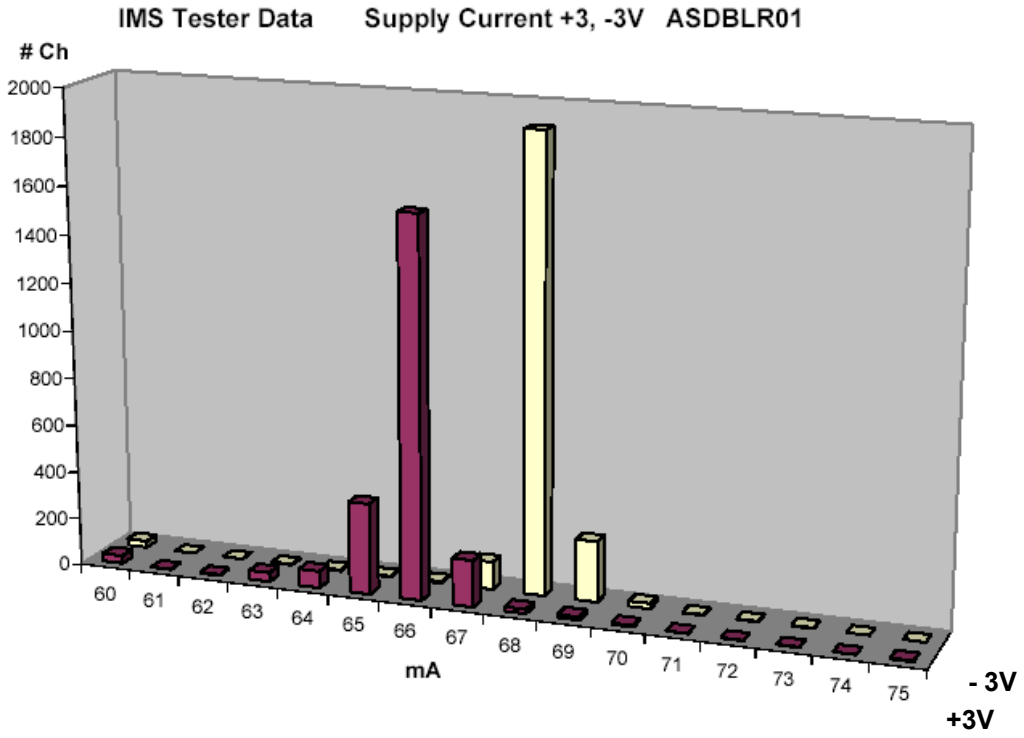
Tests, YIELD AND DETECTOR PERFORMANCE

Test DATA for the ASDBLR

The IMS tester at Penn has been used to test all generations of ASDBLR chips. At present, a complete set of measurements is attempted on each chip so that the data from all chips with functional channels may be used to sort out the best devices for mounting on the detector. Production testing may present other priorities, but the relatively short test time of ~25 seconds does not cause concern.

Supply Current

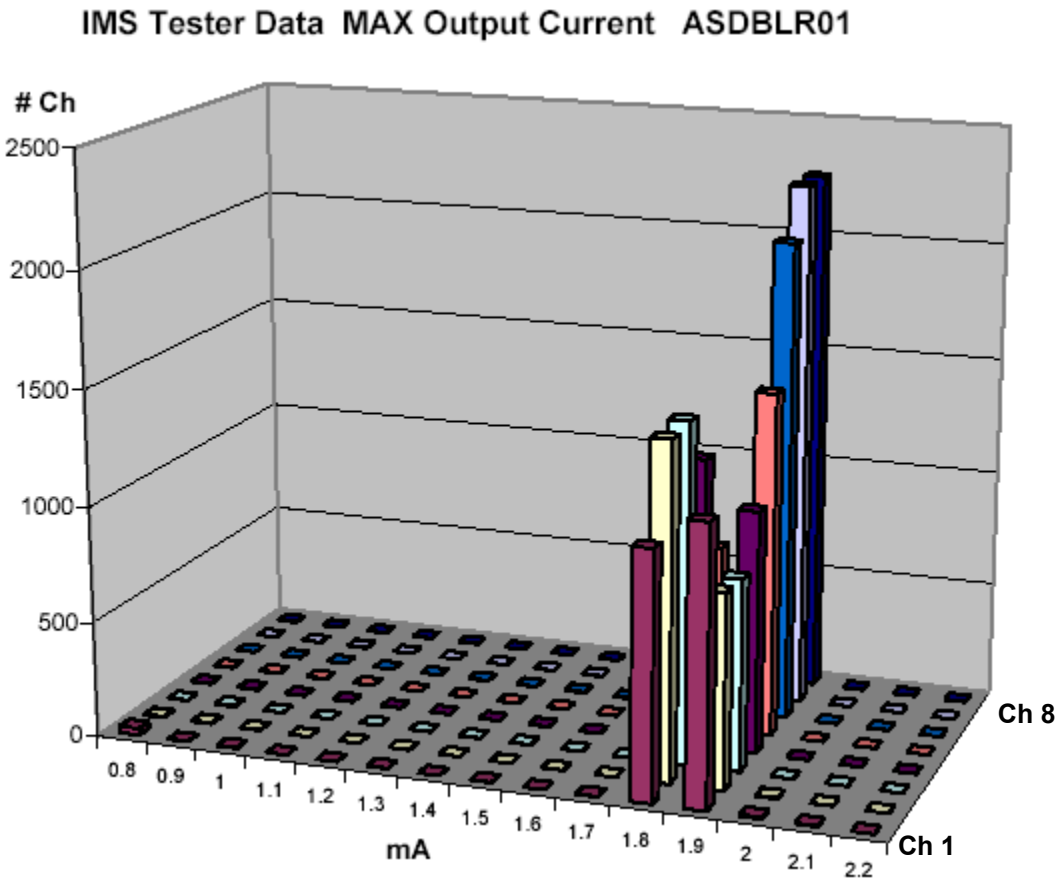
The supply current is the only chip level measurement made at the moment. (We are considering the addition of Threshold currents to allow monitoring of NPN beta.)
A distribution of the data from all ASDBLR01 chips tested to date is shown below.
It should be noted that the tester programs the ternary outputs for maximum output current which increases the draw on the power supplies. These numbers do not reflect the final power consumption (36-38mW/channel) that the ASDBLR will require when implemented in the TRT.



Ternary Driver Output Current –

The output current for all 16 ternary outputs is recorded twice: first with the Track and Transition Radiation thresholds set to their minimum value and then set to their maximum value. This data can be used to establish the uniformity of the threshold

current output and to verify the DC functionality of the individual comparators. A plot of the maximum ternary output current is shown below for each channel of the ASDBLR01 data.



Trigger Threshold –

A variable amplitude pulser connected to each ASDBLR channel is used to determine the effective threshold for the Track and TR comparators on each channel of the chip being tested. Three pulser settings are used to calibrate the Track comparator (2fC, 3fC and 5fC) and two settings (30fC and 50fC) for TR comparator. At each pulser setting the relevant threshold is varied to find the 50% triggering efficiency point. The threshold search starts at a target value and is decremented or incremented in 5mV steps. A total range of 150steps in each direction is allowed by the tester program.

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Data from these tests are stored in a database and may be sorted to establish yield versus a variety of criteria. Although the test algorithm and method of storing data has evolved somewhat, the tests described above have been used on all generations of ASDBLR.

Functional Yield -

While not part of a final test strategy it is useful to establish a *functional yield*.
To do this we put wide, but somewhat arbitrary limits on the data.
Supply current is constrained to be between 60 and 70mA, and the output drive current is expected to be within 0.5mA and 5mA.

About 6% of the tested ASDBLR01 chips fail these cuts, a final refinement may be useful but is not likely to impact yield significantly. Input to output channel functionality is established by looking at the 3fC and 30fC pulser data. Track and TR threshold data are required to be between 200mV and 500mV to qualify a working channel. This limit is intended to be well outside the range of values that we expect to select working chips from.

Table 1 Functional Yield Loss by cut of the ASDBLR01 (2300 ASIC sample)

	Cut	Yield Loss by cut
Supply Current	65±5mA both supplies	3.3%
Max Tern Output Current	.5mA to 5mA	2.3%
Channel Response	200mV < Thr** < 500mV	15.2%
Cumulative Yield Loss		20.8%

** 3fC Threshold for Track discriminator and 30fC Threshold for TR discriminator

Using this definition the functional yield loss of the ASDBLR99, ASDBLR00 and ASDBLR01 fabricated designs has been relatively constant at about 20%.

Parametric cuts on Threshold Deviations –
Since the Transition Radiation and Track threshold are chipwide control lines that are individually set by the DTMROC, it is important to understand the variation in effective threshold among the channels within each chip. The deviation from a chip wide average is used as an important parametric acceptance parameter for yield. Yield loss due to a physics driven cut on the transition radiation threshold is considered first and finally the effects on the total yield of Track deviations threshold are examined.

To establish yield estimates for production we have looked extensively at the IMS data for 1107 ASDBLR01 chips, the total sample available in February ’02. Functionality tests as described above are performed on the data before applying the tighter threshold cuts mentioned examined below.

TR Threshold Deviations –

The TR threshold is used to detect the conversion of a probable TR photon within the straw tube. This energetic conversion results in the deposition of about 6KeV of energy and is relatively easy to detect. A physics goal of ±500eV has been established that looks like it will have minor impact on yield. The table below shows the yield loss for several values of TR threshold deviation both in terms of additional loss to functional yield and cumulative yield loss to the 1107 chip sample.

Table 2 Effects of cuts on threshold deviation for ASDBLR01 TR threshold data.

Equivalent Energy Loss	Equivalent Input Charge	Additional Yield Loss	Cumulative Yield Loss
750eV	6.82fC	1.3%	22.3%
500eV	4.55fC	5.2%	26.2%
400eV	3.64fC	8.8%	29.9%
300eV	2.73fC	21.3%	42.4%

Track Threshold Deviations –

Given the relatively low value of gain that the TRT straw tubes will operate at, the setting of the Track threshold will require a careful optimization of singles rate, detection efficiency and track resolution. The effect of the Track Threshold maximum deviation cut on the 1107 chip sample of the ASDBLR01 data after all other cuts are taken is shown below.

Table 3 FINAL Yield after parametric selection of Track threshold with a ±500eV cut on TR threshold data.

Equivalent Energy Loss	Equivalent Input Charge	Final Yield
175eV	1.6fC	73.8%
26eV	0.236fC	30%
32.5eV	0.295fC	40%
40eV	0.364fC	50%
52eV	0.473fC	60%

Removing the TR cut of ±500eV adds 3% to the final yield of the 40eV cut in the table above rather than the 6.5% that one would expect by looking at Table 2. This is due to the fact that many of the failures are in the analog signal processing sections common to both comparators.

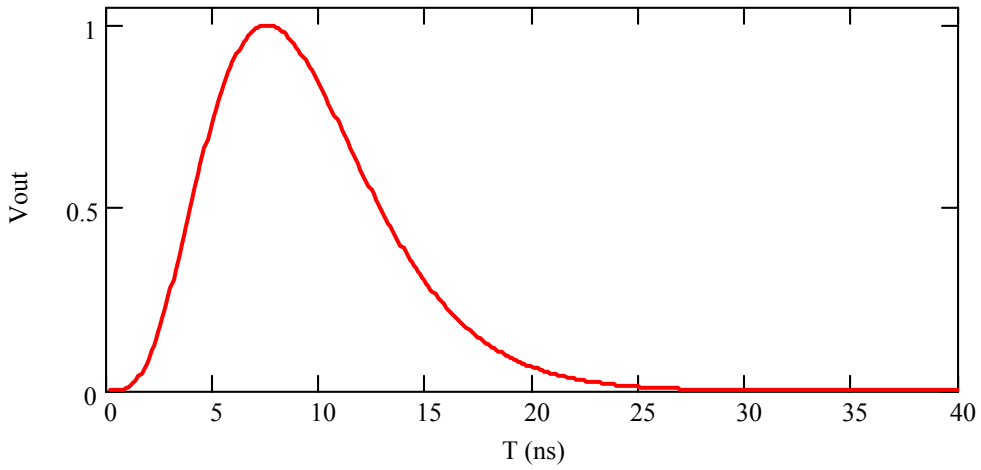
Calculated singles triggering rate due to intrinsic noise.

A calculation of the noise is useful to cross check SPICE results and to examine the effects of parameter changes quickly. Using Mathcad a calculation has been

implemented consider basic circuit and operational conditions. In the preamps: temperature, transistor beta, resistance, input capacitance, series input protection elements are considered. The noise of the two preamps is added in quadrature with consideration of the individual loading. The shaper is considered to add a constant noise of 1100e also added in quadrature. Due to the extended arrival time of the xenon pulse only 85 percent of the total charge arriving in the first 7.5 ns is considered to be available.

Shaping function assumes four equivalent 1.875ns poles. The calculation gives noise in electrons and then the noise is used with an input threshold to calculate the total rate of threshold crossings, considering the maximum trigger rate to be 50MHz.

Multi-Pole Waveform Used for Calculations of Series and Parallel noise weighting functions



The threshold of 2.1fC (~250eV) in the table below is chosen to allow operation at a typical noise rate of 10KHz.

Table 2 The trigger rate for various noise parameters is considered assuming a fixed 2 .1fC threshold.

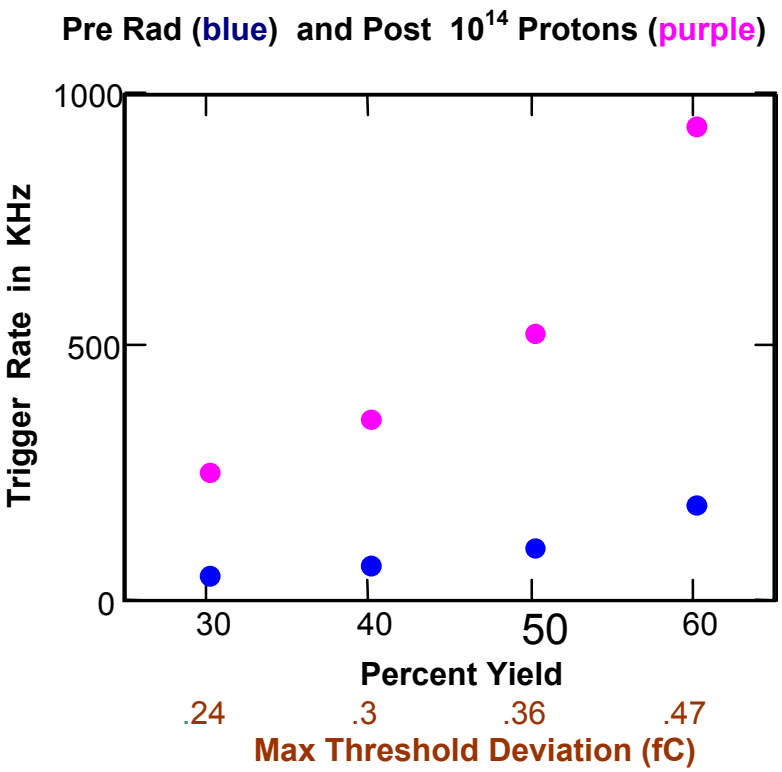
ENC e	ENC/pF	Ic Q1(μA)	Beta	Temp °K	Trigger Rate
2470	96	540	220	330	13KHz
2441	92	710	220	330	10KHz
2770	92	710	65	330	54KHz
3240	92	710	30	330	250KHz
3130	86	710	30	300	180KHz

** Other parameters used in calculations include: 16pF on the active input, 7pF on the dummy side, rb = 31.5Ω Peaking time 7.5ns.

Implications of threshold spread on singles rate

For optimal timing resolution the track discriminator must be operated at the lowest feasible threshold so ultimately the threshold level will be chosen based on the highest allowable singles rates. Since the DTMROC provides a single threshold Track and Transition Radiation setting for all channels on each ASDBLR threshold variations within the ASDBLR chip can not be compensated on a channel by channel basis. To avoid a large number of noisy channels or a lower detection efficiency, the threshold spread must be tightly controlled. Radiation effects lead to a reduced gain and an effective increase in threshold spread. This must be considered at the time of chip selection. The plot below shows the effects of threshold selection on trigger rate, considering the conditions above where the nominal threshold is set to 2.1fC and assumes that after exposure to 10^{14} protons/cm^{2} ** the gain at the input to the Track comparator is reduced by 25% and the beta of the NPN transistors is 65. Test data from 1107 ASDBLR01 Asics was used to determine the threshold cut to achieve the given yield. The singles rate grows significantly for yield cuts above 50% which corresponds to ± 0.36fC .

RATE IMPLICATION OF WORST CASE TRACK THRESHOLD DEVIATION CUTS



** The total dose in the TRT is expected to be 7X10^{13}n/cm^{2} for neutrons and 1.5mRad of ionizing radiation.