# ASDBLR Production Plan - *Draft* version 1.0

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Draft plan for the production flow for the ASDBLR chip for the ATLAS TRT detector.

# 1.0 Introduction

The ATLAS TRT has nearly 425,000 straws to read out and will require slightly over 53,000 working ASDBLR chips to instrument it fully. Adding in production and lifetime spares, we need to produce about 65,000 working, certified, tested, ASDBLR chips. At the present estimated yield of 50%, that implies producing, packaging, and handling about 130,000 chips. This is a large enough problem that it needs to be carefully thought out before production actually begins. This document is a first attempt to outline a detailed production plan. In this version we assume the following:

- The present (ASDBLR01) electrical design is final and that the minor layout changes to save space on the input protection circuitry will result in a chip that is 3.6 x 3.3 mm.
- All production will be done by ATMEL using the DMILL process at their Nantes foundry.
- All die will be packaged before test, but that some wafers may require screening tests to validate lots prior to packaging.
- That some die will be packaged in TQFP packages and some in FBGA packages this is only to generate the most conservative plan - the actual expectation is that the FBGA package will prove successful and all die will be packaged in FBGA's by Signetics Korea.

# 2.0 Requirements

## 2.1 Accountability

DMILL is a limited access radiation hard process and we are required to maintain logs of the location and use of all DMILL objects. This implies that our production plan must incorporate accounting and accountability at each step for all material delivered to Penn by ATMEL and then follow the flow of that material throughout the life of the TRT project.

### 2.2 Traceability

Because the performance of the detector depends upon the analog parameters of the ASDBLR (specifically the channel to channel threshold matching), it is necessary to keep an individual record of each chips measured performance. This implies the need to serial number the chips.

### 2.3 Maintainability

Because the ATLAS detector is expected to have a greater than 10 year lifetime and because the semiconductor process used for the ASDBLR is very unlikely to be available near the end of that time, it is necessary to maintain a stock of spare ASDBLR chips in usable condition for at least 15 years after the end of production. This implies the need for good long term storage facilities for the devices.

## 3.0 The Database

All information for the required traceability is maintained in a single central database on the Penn server. This database shall be SQL compliant, regularly backed up, and nonerasable. Appropriate viewers and entry tools for the database will be provided by the Penn ATLAS group. A copy of the tables from this database may be transferred to CERN or BNL or any other ATLAS institute as required with a simple set of queries to the database. This database will be modeled upon the present prototype ASDBLR test database, but will require additional features and tools.

## 4.0 Entities Involved

The following institutional and commercial entities are involved with this production flow. Contact names will be provided for each entity in the next version.

## 4.1 University of Pennsylvania (PENN)

The Penn ATLAS group has provided the design and most of the testing and verification of the ASDBLR to date. The Penn group is responsible, via MOU, for the production of the ASDBLR for ATLAS. The Penn group is, in addition, responsible for producing some fraction of the End Cap ASDBLR boards and so is also a consumer of the devices.

# 4.2 U.S. ATLAS

The U.S. ATLAS management, based at BNL, is responsible for overseeing the cost and schedule for items supplied by the various U.S. groups to ATLAS, including the University of Pennsylvania contribution of the ASDBLR. U.S. ATLAS is also the intermediary between the U.S. Department of Energy, which ultimately provides funding, and the Penn ATLAS group.

# 4.3 CERN

The "Frame" contract with ATMEL has been negotiated by CERN for all LHC groups and purchase orders to ATMEL and delivered wafers from ATMEL flow through CERN to satisfy the terms of this contract. CERN also is responsible for fabricating some of the End Cap boards using the ASDBLR packaged devices and so is also a consumer of the devices.

## 4.4 Lund

Lund University is responsible for assembly of the Barrel stamp board(s) and so is a consumer of some of the ASDBLR devices.

## 4.5 ATMEL

The DMILL foundry is owned by ATMEL Inc. and design files and purchase orders are directed to ATMEL. ATMEL manufactures the wafers, does screening tests to verify compliance with test structure parameters, and then ships the wafers to CERN. ATMEL also guarantees a minimum yield for each group of delivered wafers - the details of this guarantee are to worked out at the ASDBLR PRR in March 25/26, 2002.

## 4.6 The Packager

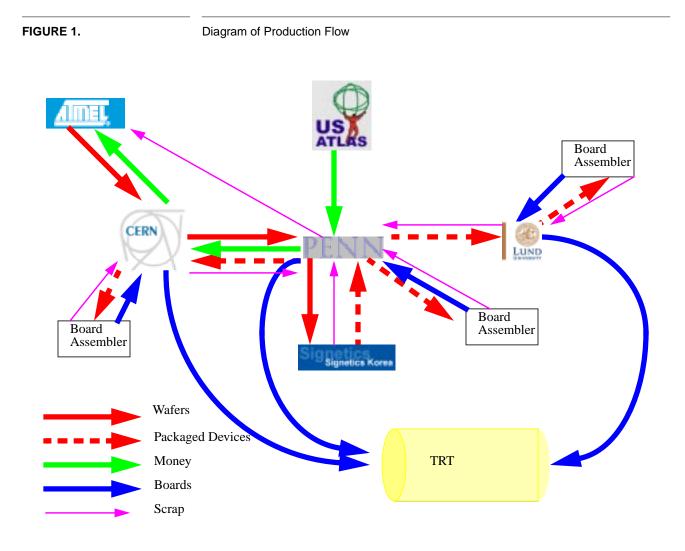
All production wafers are to be sent to a commercial house for packaging in either TQFP or FBGA packages. Any packaging house must be approved by ATMEL in order to have temporary possession of the wafers and must return all scrap material to Penn and or CERN. The particular identity of the selected house depends upon both the package type(s) chosen and a competitive bidding process.

# 4.7 The Board Assembler(s)

As the boards for the Barrel and End Cap are being paid for by several different ATLAS groups (at least CERN, Lund, and Penn) and each institute might choose to have more than one assembler, it is necessary to be prepared to deal with multiple Assemblers in terms of QA/QC, shipping, and inventory control. Each of the board assembly houses must be certified by ATMEL to carry out assembly using DMILL devices and must carefully control all scrap devices which must be returned to Penn.

# 5.0 Production Flow

In this section we outline the production steps from the end of all wafer testing at ATMEL to the point at which tested, good, devices are shipped to a board assembler. Production steps at ATMEL and at the board assembler are not covered in this document.



## 5.1 First Shipment

Wafers are shipped to CERN from ATMEL. The only step at CERN is to record the number of wafers shipped (and all accompanying test data). CERN then ships the same wafers (in the same or upgraded packaging) to The Packager (as an option one could imagine shipping wafers to Penn and then to The Packager, but that seems inefficient and would only be done if there were some significant legal or cost impediment to direct shipment). Shipping method(s), customs brokerage issues, etc. remain to be determined.

## 5.2 Packaging

The Packager thins, dices, and packages the devices as described in the packaging specifications. All packages are placed in standard JEDEC trays for shipping. All packages are marked with:

- Device Name ASDBLR
- Design Institute UPENN
- Lot number or date code (TBD) e.g. Lot N or 5102

All devices plus all scrap are then sent to Penn.

## 5.3 Receiving

Packaged parts are received at Penn, count is verified, marking(s) are verified and recorded, and the scrap is accumulated to return to ATMEL or dispose of as directed. All non-scrap parts are then stored in a dry Nitrogen atmosphere until the next step.

## 5.4 Serialization

All devices are serial numbered using a 2-D coded label. The information on the label is yet to be finalized, but is, at a minimum, a serial number and a unique identifier to differentiate an ASDBLR device from any other 2-D coded device in the TRT - e.g. "ASD" or, at least "A". The ASDBLR serial numbering scheme must run to numbers larger than 200,000 to cover the possible range (allowing for some yield variation). At this point the devices enter the Database with the information that devices Axxxxx to Ayyyyy are from wafer lot N which was composed of wafers Wuuuuuu to Wvvvvv delivered to CERN on xx/xx/xx, etc. Serialized devices are returned to dry Nitrogen storage.

We expect to be able to use the automatic chip handler during some first shift time to apply the labels. The labels will, probably, be commercially printed, but this is still to be determined.

# 5.5 Testing

All testing is to be done on the Penn IMS tester using a "standard" test fixture. The standardized production test sequence as described in ATL-IT-ER-0014 v.1 is likely to be modified somewhat before actual production, but the basic tests will remain. For the rest of this document "test" will mean this sequence of IMS based electrical tests unless otherwise indicated. All test results are recorded in the Database. Tests instances are marked with date/time of day so that multiple tests of the same device may be tracked independently.

## 5.5.1 Sample Test

As soon as possible after Serialization a small number of devices will be selected from the new shipment for immediate testing. Devices should be selected so that all trays of that shipment contribute at least one device to the test lot and the test lot should be of a statistically significant size - for this draft we suggest a test lot of greater than or equal to 20 devices. If the tested yield is within two sigma of the running average yield, the sample test is passed and the devices are returned to storage. If the tested yield is more than two sigma away from either the running average or ATMEL target yield on the low side then more devices should be tested (at least 100, again spread across all the trays) and the results of that second test will indicate whether or not there is a possible problem and whether or not ATMEL should be contacted immediately.

#### 5.5.2 Production Test

Production testing is done as a  $2^{nd}$  -  $3^{rd}$  shift activity by loading the handler with trays of untested parts. Parts are returned to the same tray after testing and sorting is handled later during the Triage or Shipment phase. The four tray handler then allows four trays of devices to be tested overnight - that is either 4 x 160 or 4 x 210 parts per night depending upon whether they are in TQFP or FBGA packages. Since the test time is between 25 and 50 seconds per device (unoptimized), all four trays would easily be complete by the next morning. At 640 devices per day, 3200 devices per week, it would take slightly more than 40 weeks to complete all the testing for the entire TRT. If this poses a possible schedule problem that rate can be significantly improved by have an evening operator switch trays once and, of course, by using some first shift time.

As each device is removed from the source tray, the 2-D code is read by the handler CCD camera and that serial number is entered into the database with the test results and test time. Location of the device after testing is also entered into the database.

All devices are returned to dry Nitrogen storage at the end of the test

#### 5.5.3 Retest

At appropriate times during the testing process some of the previously tested devices are to be retested to validate the DUT board, database, and device stability and reproducibility. The frequency of this retest and the number of devices to be retested is still to be determined.

#### 5.6 Data Analysis

At the end of each testing week (or more often if possible), all the recent data will be analyzed to give functional yields and distributions of parametric yields (i.e. threshold matching). Any anomalies in the yields or distributions need to be addressed immediately to determine if they are testing or process related. All such summaries shall be posted on the Penn ATLAS web page.

#### 5.7 Triage

Before devices are shipped to a board assembler it is necessary to go through a selection process. Based upon the test (and retest) data it is possible to divide devices into several categories:

- 1. Non-functional
- **2.** Partially functional (e.g. 6 working channels)
- 3. Fully functional but not satisfying the parametric cuts
- 4. Fully functional and satisfying all the parametric cuts

The non-functional devices clearly just go into the controlled scrap pile and the partially functional devices are only useful for bench tests or other non-critical uses, but the fully functional devices are all possible candidates for use on the detector (even devices outside the parametric cuts could plausibly be needed some years in the future to replace broken devices once our good spares are used up) and must be inventoried and stored until used on boards or until ATLAS TRT is decommissioned (2053??).

Since the actual implementation of parametric cuts will require at least a moderately large data sample, it may be necessary to ship the initial batches of chips to the board assembly house(s) as a sub-set of the final parametric cut. Thus the Triage step is envisioned as being a data only exercise until just before shipment.

#### 5.8 Shipment for Board Assembly

Boards using the ASDBLR devices will be assembled in multiple places as there are two or three variants of End Cap boards and then a Barrel stamp board funded by multiple funding entities. Requests for devices will be received from, at least, CERN, Lund, and Penn and devices must be sorted and shipped as soon as possible after a request. All shipments will require selection of devices from the database and verification that the requested serial numbers were packaged for shipment. Records of each shipment including addressee, date, shipping method and airbill number, packager name, and serial numbers of shipped parts will be recorded in the database. Board assembly houses will be required to return unused devices and damaged devices to Penn. Unused devices will be returned to TRT stock, damaged devices will be put into the DMILL scrap storage location for eventual disposal.

#### 5.9 Long Term Storage

After assembly of all the front end boards required for the TRT and operating spares, remaining ASDBLR devices must be stored for possible repair and rework during some future maintenance period. Remaining good devices (those listed in categories 3 and 4 from Section 5.7 on page 6) will be stored under dry Nitrogen until required or until the ATLAS TRT defines them as obsolete. Category 1 devices (the controlled scrap pile) will either be returned to ATMEL or disposed of according to their instructions. Category 2 devices will be treated as Category 3 & 4 devices unless the ATLAS TRT group decides differently at some future point.

# 6.0 Summary

This document is a draft of a plan to handle the front end integrated circuit production testing and material flow for the ATLAS TRT ASDBLR chips. Some 65,000 known good ASDBLR packaged devices will be fabricated at ATMEL, packaged at one or more packaging houses, tested at the University of Pennsylvania, and delivered to various board assembly houses for inclusion on ATLAS TRT specific printed circuit boards. All good and scrap devices will be tracked in a database available to all ATLAS collaborators and all remaining material will be stored at the University of Pennsylvania for the life of the ATLAS TRT project.

This document is incomplete at present and significant additional material is required before this process can proceed. The primary missing details are:

- Detailed implementation of a 2-D bar code scheme printing, applying, and recognizing.
- Detailed implementation of a final or near final database and the query tools for utilizing the database.
- Material moving during the production testing specifically what automated handling will be provided and how it will be controlled.