ASDBLR 99 Yield Studies

Low Threshold Parametric Study
1030 chip sample
830 chips functional
100eV ≅ 100mV

Max Dev. from
Chip Average

Thr + (mV)	Thr - (mV)	Yielded Chips	Effective Yield	Total Yield
300	300	830	100.00%	80.30%
35	35	299	36.00%	29.00%
50	50	528	63.60%	51.00%
55	55	577	69.50%	55.80%
50	75	584	70.40%	56.50%
50	100	598	72.00%	57.90%

Noisy Channels require Higher Thresholds.

Functional Cuts requirement:
Less than 30% deviation on power
All channels respond to Low and High Thr input.
Transition Radiation threshold required ≤ 55mV
No check of test pulse input.

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Analysis of Threshold offset Origin:

A significant part of the unexpected channel to channel mismatch observed in the tracking discriminator threshold can be explained as arising from a random DC offset at the inputs to the first stage of the discriminator.

No leakage was detected in the capacitors AC couple the BLR to the shaping stages. One source of offset is found to be due to the combination of the DC operating point of the BLR and ~1% (1 sigma) resistor mismatch in the input attenuator network. The expected value using the DMILL Design document was 1.44% 3 sigma.

Summary of measurements pointing to Resistor mismatch:

Data was taken with five chips, two with low offsets and three with a BLRBIAS dependent offset in channel 1. This is an enriched sample of ASDBLR's intended to help investigate the cause of sensitivity to the BLRBIAS setting. Most measurements were taken with chip #164 channels 1,2,3.

1) Tracking Discriminator zero point offset. Disc powered, Shaper/BLR off.

*RMS channel to channel variation of for all five chips → 18mV.

* Increasing or decreasing the Discriminator +/- power supplies while keeping the difference voltage the same produced only small threshold shifts that could easily be early voltage effects.

2) Tracking Discriminator zero point offset with Shaper and BLR powered.

*RMS channel to channel variation →38mV.

Subtracting the 18mV discriminator only RMS variation from 1) in quadrature gives a 33mV RMS offset contribution due to turning on the BLR network.

3) Measurement of the DC output of the BLR monitor in channel 1.
From the schematic we can deduce that the DC output of the BLR monitor should reflect 83% of the DC offset of the BLR stage.
None of the chips shows a significant offset at the BLR monitor point.
The variation of the BLR monitor DC offset with BLRBIAS**
The BLR Offset variation ~1mV for all chips measured for -2V<BLRBIAS<2V.
(BLRBIAS determines the DC operating point of the BLR outputs)

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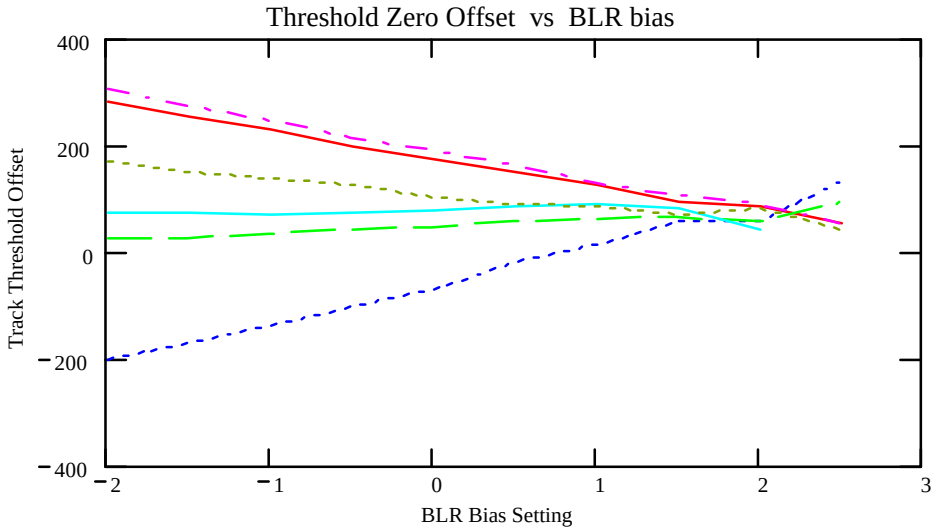
4) Threshold offsets DO vary with BLRBIAS setting. The variation appears to be reasonably linear with a wide range of positive and negative BLRBIAS dependant slopes (Thresh Zero/BLRBIAS). A n offset as large as 15mV at the input to the comparator is indicated in the parts measured when the BLRBIAS is set to it's extreme value.

Plotting the Threshold offset vs BLRBIAS data from three channels shows a common intersection at about 1.8v of BLR bias with thresholds ranging between 30 and 70mV, similar to the shaper off thresholds measured in 1). Some threshold offsets change from positive to negative as a function of BLRBIAS.



5) Holding the Discriminator Power fixed at +/-3V and varying the Shaper power supplies with respect to 0V and allowing BLRBIAS to track with of all slopes at some point. The sign of the slope is consistent with the slope found in 4) considering the change in the DC operating point with BLR BIAS.

Conclusions:

1) There is NO significant DC offset in the bridge.
2) The intersection point of the slopes noted above occurs when the DC output of the BLR equals the 0V reference (GNDD) of the discriminator input stage attenuator network and no quiescent current flows through the resistor attenuator network between the BLR and input to the comparator.

1-2mV offsets at the input of the tracking discriminator are indicated under normal operating conditions when the BLR output operates at ~500mV and the resistors vary in opposite directions by order .5% . This accounts for a threshold offset of ~40mV. These variations are consistent with the values for expected for NPN transistor variation.

Elimination of this Offset Contribution:

The attenuator network does not need to reference ground on the comparator side. This was done to ensure a wide range of setpoints for the BLR current for the prototype. It allows both the DC and AC component of the BLR output to be

attenuated. Our tests have shown no need to vary the BLR current, the shape is relatively insensitive to the setting of the BLRBIAS. Elimination of the ground reference for the differential attenuator network is a trivial change that to first order will eliminate the DC current in the network that causes the offset. See the schematic of the input stage of the comparator that follows

NPN matching. Measurements by TEMIC indicate that the 3 sigma Base – Emitter voltage matching of NPN devices specified in RDER 2401 of 1.85mV for a 1.2 μm X.8μm is exceeded by a factor of 2 to 3. Scaling to the input of the comparator where we used 4μm X .8μm NPN's, the expected 20mV threshold offset due to NPN ΔVbe mismatch of 20mV will be more than doubled.

Adding in quadrature the RMS threshold variation expected due to the comparator attenuator network and the offset due to mismatch of Vbe in the NPN comparator input stage we can estimate an additional threshold offset contribution of $2^{1/2} * 40mV = 56mV$ due to these effects alone. Gain and shaping variations set a minimum variation channel to channel within a chip originally expected to bey ~25mV.

Rev 00 Version of the ASDBLR to reduce threshold offsets –

The following changes have been implemented in the REV 00 version of the ASDBLR to reduce the threshold offset.

1) Elimination Ground Reference at the input to the Tracking Comparator.
2) Increase of 4X in the emitter length of the comparator differential input stage and implementation of a cross quad layout.
3)
4) Increase of 2X in the emitter length of the emitter followers at the BLR output.

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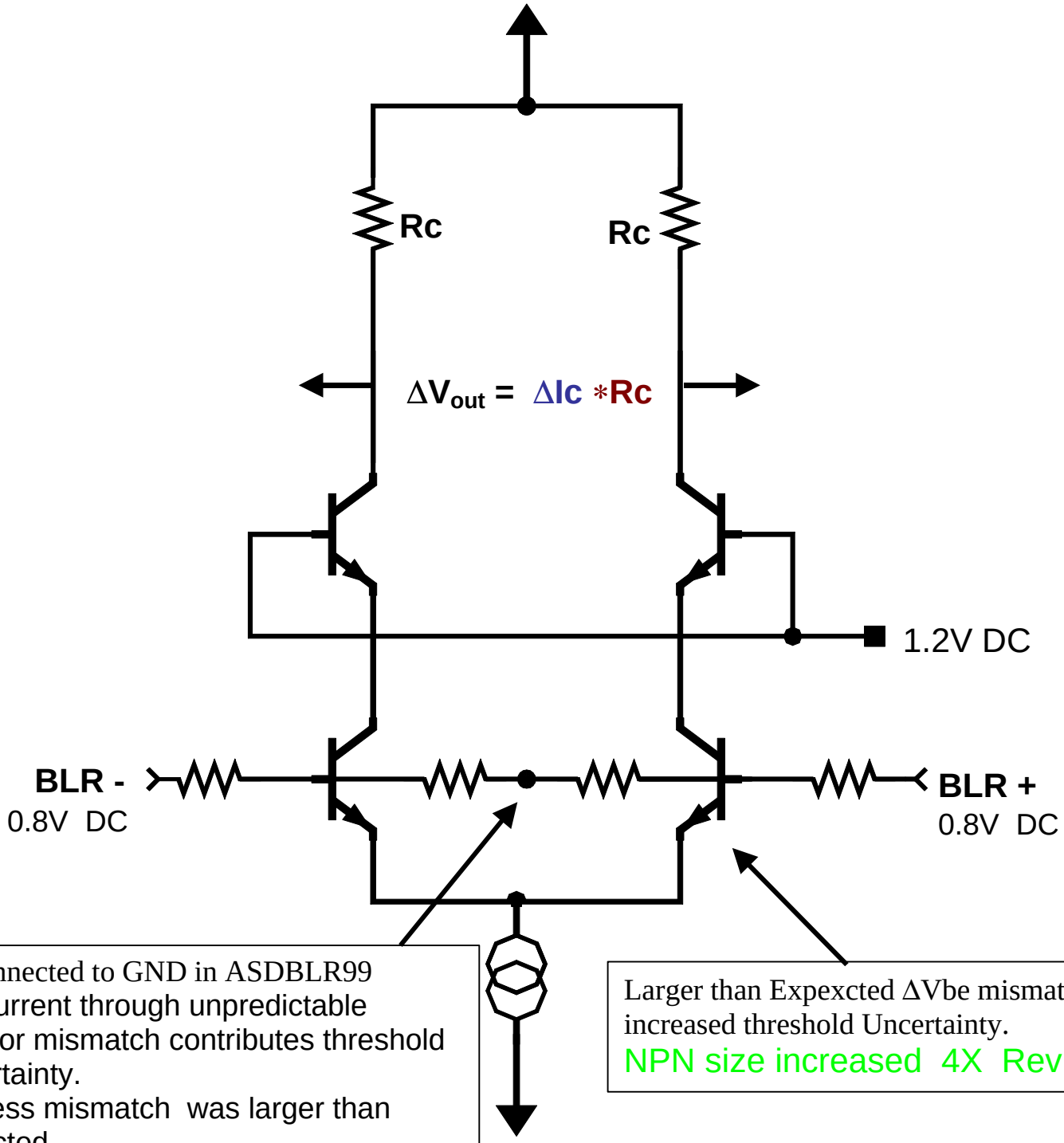
Threshold Offset Contributions

Input Stage to Track Discriminator



Connected to GND in ASDBLR99
DC current through unpredictable resistor mismatch contributes threshold uncertainty.
Process mismatch was larger than expected .
Removed GND reference in Rev 00.

Larger than Expexcted ΔVbe mismatch increased threshold Uncertainty.
NPN size increased 4X Rev 00

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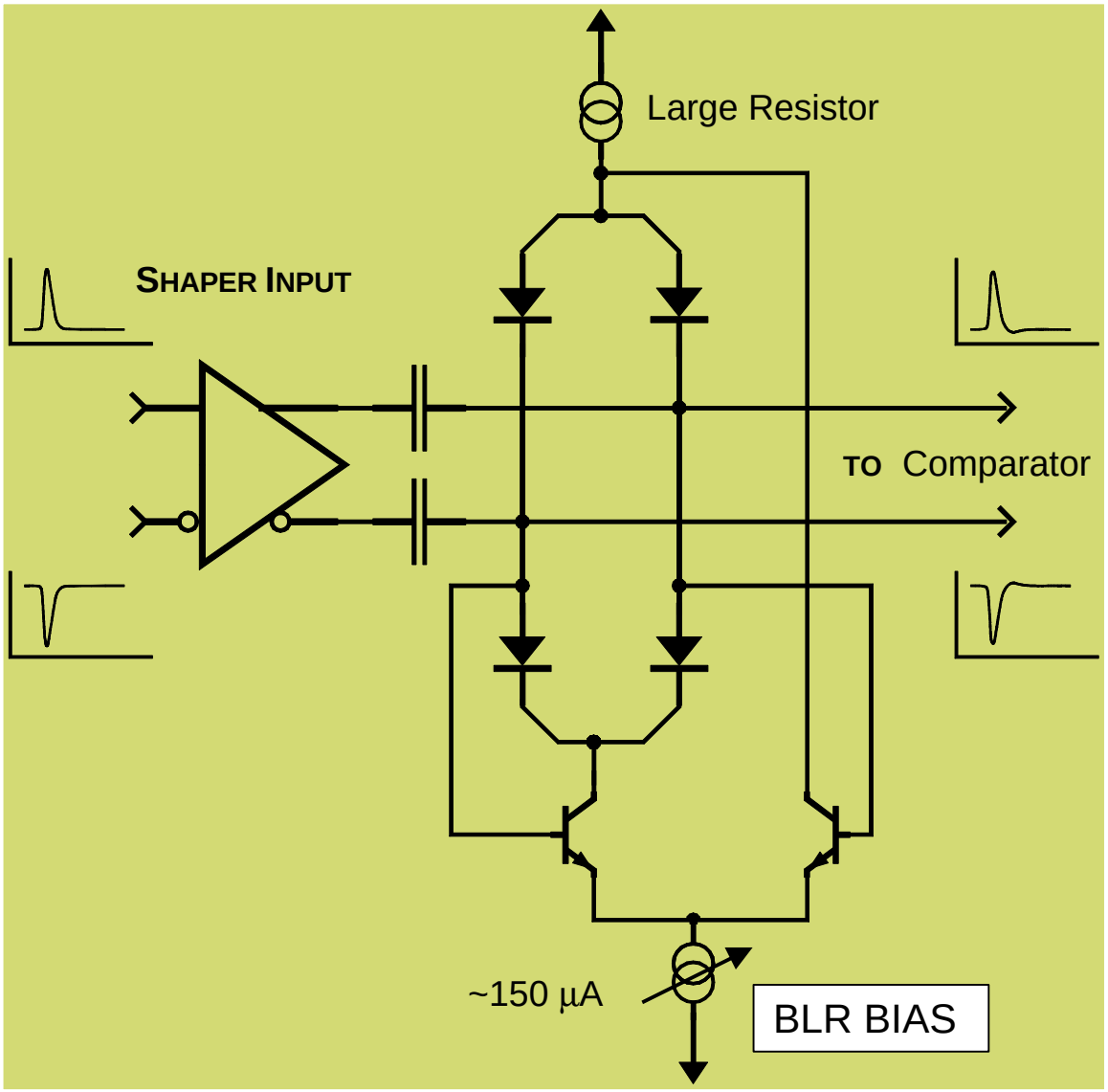
BRIDGE BLR with CURRENT STEERING



Adjusting the bias current in the BLR changes the DC operating point Of the BLR output. The output of this stage connects to the Comparator input shown in the previous slide.

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