

Project Specification

Project Name: **DTMROC**

Version: **DSM**

Author	Date	Changes
Ph. Farthouat	17 Jul. 97	First draft
Ph. Farthouat	21 Jul. 97	Electrical characteristics
Ph. Farthouat	23 Jul. 97	Paul Keener's corrections
Ph. Farthouat	29 Jul. 97	Peter Lichard's corrections
Ph. Farthouat	13 Aug. 97	Rick Vanberg's corrections
Ph. Farthouat	19 Sept. 97	16-channel version
Ph. Farthouat	22 Oct. 97	Indiana workshop modifications
Ph. Farthouat	03 Nov. 97	Indiana workshop modifications
Ph. Farthouat	13 Nov. 97	Command decoder modifications, test pulse & list of blocks
F. Anghinolfi	27 Mar. 98	Second draft for review on 6/7 April 98
M Söderberg	16 Jun. 98	Updates from the design review in Penn
Ph. Farthouat	24 Jul. 98	Dead-time requirements updated
P.T. Keener	04 Aug. 98	Command decoder modifications
M Söderberg	16 Aug. 98	By-pass and test points documentation
Ph. Farthouat	26 Aug. 98	A few mistakes correction
N. Dressnandt	4 May 2000	Update Spec to reflect real DTMROC
V.Ryjev	28 Mar.2001	DSM DTMROC additional features
R. Van Berg	03 Nov.2001	DSM DTMROC update text and introductions
M. Newcomer	7 Jan 2003	Update, added sections on Analog I/O, Pad list, Pad Frame etc.

Table of Contents

Table of Contents.....	1
1.1 ATLAS TRT Readout Architecture	3
2 Technical aspects.....	5
2.1 Requirements.....	5
2.1.1 Robustness and Testability	6
2.2 Input Decoding, Time Registration, Data flow, and Readout.....	8
2.2.1 Input Level Translators: Ternary Receivers (See also section 3.1).....	8
2.2.2 Input Latch.....	9
2.2.3 Time digitiser.....	10
2.2.4 Test and mask register	11
2.2.5 Pipeline	11
2.2.6 L1A and BC identifiers: L1ID and BCID.....	12
2.2.7 Derandomizer.....	12

2.2.8	Readout	13
2.3	Command Decoder	14
2.3.1	Error handling	14
	Unrecognised field 1	14
	Unrecognised field 2	15
	Field 3 < 12	15
	Mismatched chip address or unrecognised field 5	15
	Table 2.2 Control and communication command field descriptions	15
2.3.2	Configuration Register	16
2.4	Miscellaneous	19
2.4.1	DTMROC Reset list	19
2.4.2	Threshold DACs	20
2.4.3	JTAG Logic Implementation and Access	21
3	I/O	23
3.1	Inputs	23
3.1.1	Power -	23
3.1.2	Ternary Inputs	23
3.1.3	LVDS Inputs : Clock, Hard Reset, Command In –	24
3.1.4	Address inputs (0-5) -	24
3.2	Outputs	25
3.2.1	Data Output Drivers - (Data out and CMD out)	25
3.2.2	Test Pulse Outputs –	25
3.3	Temperature and Voltage Sensing -	26
3.3.1	Vdd Monitoring - Bit 24 of CSR - $V_{dd} \approx (.014 * DAC - .1)V$	27
3.3.2	Temp Monitoring – Bit 23 of CSR $Temp \approx (-2.85 * DAC + 400)C$	27
3.3.3	Spare Input -- Bit 26 of CSR	27
3.3.4	AsdblPowerSense (input) Bit 25 of CSR	27
4	Pin List, Die and Packaging info	27
4.1	Functionality List	28
4.1.1	Inputs	28
4.1.2	Outputs	28
4.1.3	Power – from board ($V_{dd} = 2.5 \pm 0.25V @ \approx 120mA$, Gnd = 0V)	29
4.1.4	Test Signals	29
4.2	Pad Frame Drawing Die Size: 5mm X 5.2mm	30
4.3	FBGA package Size: 11mm x 13mm	31

Scope

The aim of the project is to design the digital read-out chip for the ATLAS TRT. The main constraints are:

- The inputs are connected to the ternary outputs of the ASDBLR.
- The timing and control interface is done according to the SCT protocol.
- This version is designed in the IBM 0.25 micron process.

This document covers the DSM DTMROC used with the ASDBLR00 or 01. There are a few relevant documents which should be read:

- ABC specifications. <ftp://ftp.te.rl.ac.uk/atlas/specification.pdf>
- ASDBLR specifications. see ASDBLR under <http://www.hep.upenn.edu/atlas/asdbl>
- Technical specification of the ATLAS TRT DTMROC.

4. Other DTMROC related links:

- <http://chall.ifj.edu.pl/~szczzygie/dtmroc/>
- <http://ryzhov.home.cern.ch/ryzhov/DTMROC/>
- A description of each analog I/O block can be found at: <http://www.hep.upenn.edu/atlas/dtmroc> under Custom DSM Analog Blocks

1.1 ATLAS TRT Readout Architecture

The ATLAS TRT front-end readout architecture is based on a bipolar amplifier/shaper/base line restorer (ASDBLR) and a CMOS digital chip (DTMROC).

To achieve the tracking and TR performances desired, the readout electronics has to perform the following functions:

1. Amplify the incoming straw signal.
2. Shape the amplified signal and remove the tail arising from the ion drift in order to keep the retrigger time short so as to achieve the desired efficiency at full luminosity (order 60% at 20 MHz hit rate).
3. Apply two thresholds, one for tracking functionality (low threshold to detect minimum ionising particles) and one for transition-radiation functionality (high threshold to detect transition-radiation X rays).
4. Obtain timing information in 3ns bins for the low-threshold signal in order to achieve the desired < 160um position resolution.
5. Store information about every bunch crossing in a Pipeline as to whether or not the input signal exceeded the high-threshold values during the full level-1 trigger latency. The Pipeline should contain at least 128 positions (3200ns latency). Note that in this implementation data is stored in the PIPELINE for 256 clock cycles (256 positions), however, because the Command Decoder requires 4 clock cycles to decode an L1A trigger command, the effective delay is only 252 cycles (6300ns latency).
6. For each level-1 trigger signal Accept (L1A), extract from the Pipeline the information corresponding to the bunch crossing, which gave rise to the L1A and to the two following bunch crossings.
7. Gather in a Readout Driver (ROD) the data from *many* channels (typically 104 DTMROCs are read out by one ROD – so 1664 channels per ROD), compress them, format them and send them to the Readout Buffer.
8. Timing and control of the DTMROC is governed by a timing and control board, the TRT-TTC which implements that ATLAS standard TTC protocols for the TRT chip set.

Tasks 1 to 6 are performed by the *front-end electronics*, which is located on the detector, while tasks 7 and 8 are performed by the *back-end electronics*, which is located off the detector in USA15. An overview of the system is presented in Figure 1.0.1.

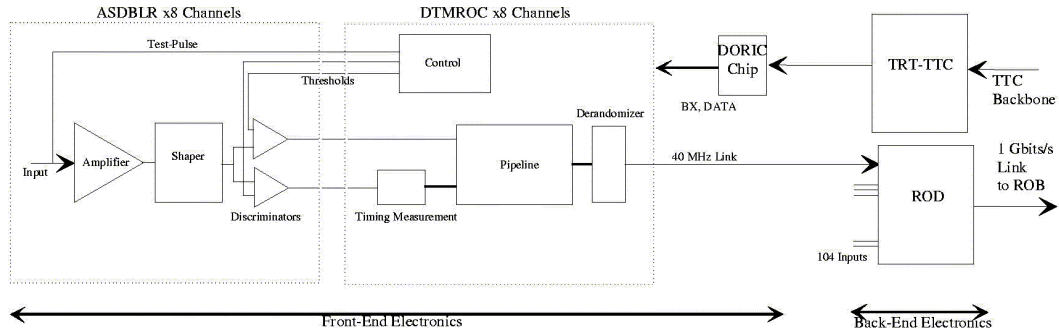


Figure 1.0.1 Schematic diagram of the TRT electronics

2 Technical aspects

2.1 Requirements

1. The DTMROC chip (or “chip”) will be designed to accept the 16 differential signals from the two ASDBLR chips and decode the ternary current levels to produce the high threshold and low threshold signals. The high threshold signal has to be glitch sensitive: as soon as a signal longer than 5ns is detected it should be extended until the next clock (see paragraph 2.2.3 of this document). Measurements show that the initial versions of the chip exceeded the required performance by detecting pulses as short as 4ns.
2. The low threshold signal must be sampled for its presence or absence each 3.125 ns during the 25 ns clock cycle. An 8-bit word should be formed with these 8 samples.
3. At the start of each clock cycle (rising edge of the clock) the chip samples:
 - 1 bit high threshold signal \times 16 channels
 - 8 bit word described above \times 16 channels
 - 3 bit Bunch Crossing counter value
 - 1 bit DLL “dynamic” error flag indicating the quality of external and DLL clock signals and stores these values, a 149-bit word, into a Pipeline of 256 positions until a decision can be made whether to keep the data.
4. Upon receipt of a Level1 Accept signal (L1A) the data from the Pipeline SRAM location, determined by the actual address pointer and the programmable latency offset, as well as the data of the two following bunch crossings are copied into another buffer called the Derandomizer. There is no restriction on the L1A command rate – consecutive triggers (each 3 bunch crossings) are accepted. This allows the storage of successive data slices into the Derandomizer followed by readout into the backend system.
5. The data written into the Derandomizer is transmitted to the ROD through a 40 Mbits/s copper link. The LVDS/Penn standard is used on this link and the chip follows the defined protocol to transmit the data (see paragraphs 2.2.8, 0 of this document).
6. The chip provides two test-pulses to stimulate all odd or all even ASDBLR channels. The amplitude and delay of the test-pulses are programmable. See paragraphs 2.3.2.1.2, 2.3.2.1.3.
7. The chip provides two 8-bit threshold voltages to the tracking and transition-radiation comparators of each ASDBL chip. See paragraph 0.
8. The chip should provide, along with the data, the following status information in a header:
 - A single mode bit indicating whether the chip is in test-mode or data-taking mode.
 - A 3-bit L1A trigger-counter (L1ID) indicating the number of triggers since the last reset.
 - A 4-bit bunch-crossing counter (BCID) indicating the number of bunch-crossings since the last reset.
 - A 1-bit flag representing the status of some error indicators in DTMROC (see 2.2.8).
9. The chip will incorporate features that will enable it to be tested at the wafer level and in situ. Tests include but are not restricted to:
 - Transmission of programmable pattern through the Pipeline and readout circuitry.
 - Transmission of the chip ID (set by on-board jumpers).
 - The functionality of the LVDS/Penn receiver and driver blocks can be tested using a spy-point mode. These components may also be bypassed entirely to test the digital core independently. Special non-production bonding is required.
 - The Functionality of channel zero ternary receiver. Special non-production attachment to the test bonding pads is required.
10. It is a system requirement that the fraction of data that is lost due to the finite Derandomizer storage on the chip is less than 1% with an average L1A rate of 75 kHz. The fraction of data lost when the

L1A rate is 100 kHz must be less than 3%. This requirement is met with 12-event storage. The chip provides storage for 42 events. See paragraph 2.2.7.

The main functional blocks and data flows of the DTMROC are presented below.

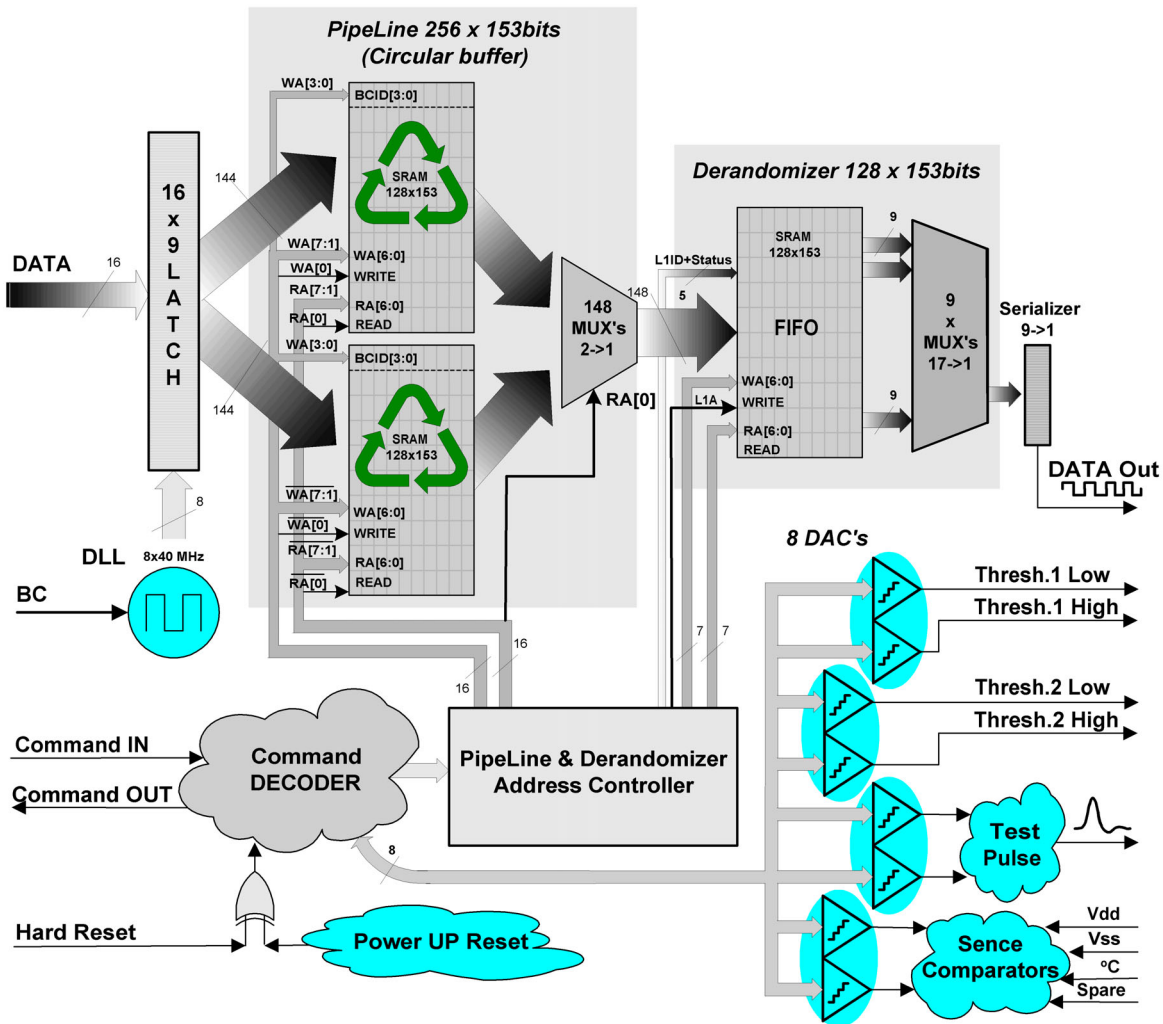


Figure 2.1 DSM DTMROC block diagram

2.1.1 Robustness and Testability

2.1.1.1 Single event upsets (SEU).

The DTMROC is intended to be used in a highly radioactive environment. Hence, it will be exposed to destructive effects (Single Event Upsets), due to the energy deposited in silicon by ionising particles. These events represent potential problems for the circuit functionality, since they cause unpredictable changes in the combinatorial and register logic cells. To combat this, a special methodology was used to implement the vital registers and sections of the DTMROC to monitor and prevent malfunctioning or

even complete loss of control of the chip caused by undesirable changes in internal storage elements, as well as possible transmission errors during the circuit configuration.

All internal registers are equipped with SEU detecting parity check logic. The most critical parts (Fast Command Decoder, Configuration and Threshold registers, event length counters, etc.) are built of the SEU resistant and self-recovering elements based on triple logic with majority vote. The schematic implementation of one register unit is presented below.

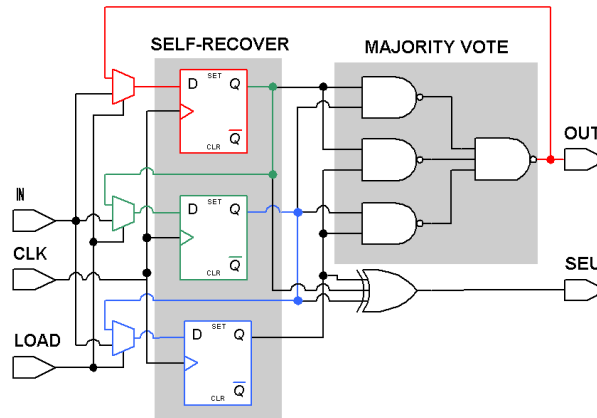


Figure 2.2 SEU resistant, self-recovering unit

2.1.1.2 Boundary and internal logic scan

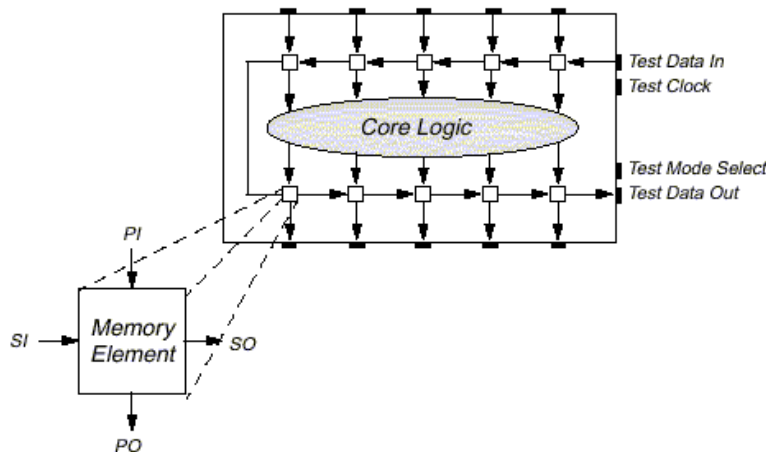
Two special facilities ensuring the full testability of the DTMROC were introduced into the design.

- JTAG Boundary-Scan concept (IEEE Std 1149.1) is implemented as a serial shift register that is wrapped around the boundary of the device. The sketch of its architecture is presented in the below.

The fundamental component of the boundary-scan architecture is the boundary-scan cell. It can shift data through the device core logic or around the core logic, depending upon the test mode selected. At the device level, the boundary-scan elements contribute nothing to the functionality of the core logic and the boundary-scan path is independent of the function of the device. The value of the scan path is at the board level, because it allows testing many devices at once. Boundary scan's primary purpose is to test for assembly defects such as missing or damaged devices, open and short circuits, misaligned devices, etc.

Three JTAG mandatory instructions (EXTEST, BYPASS, SAMPLE/RELOAD) are implemented, as well as four optional (INTEST, IDCODE, RUNBIST, USER SCAN PATH TEST). For more details see IEEE Std 1149.1 and miscellaneous in 2.4.3.

- Anc
spe
can



ernal logic. In this
 shift register, and one
 it.

Figure 2.3 Boundary-Scan concept

2.1.1.3 Memory self-test

All memories (Pipeline and Derandomizer) are equipped with Build-In-Self-Test (BIST) controlled via both, the Configuration (see 2.3.2) and JTAG register (see 2.4.3). The individual BIST results - progress and status, can be observed from the General Status and JTAG registers (see 2.3.2.1.4).

2.1.1.4 DLL control logic

Two special circuits were implemented to control the quality of the external and the DLL clocks. A “watch dog” continuously compares rates of the external and internal DLL clocks, and a “dynamic” tester examines the positions of 8 DLL outputs relative to the external clock, see figure below.

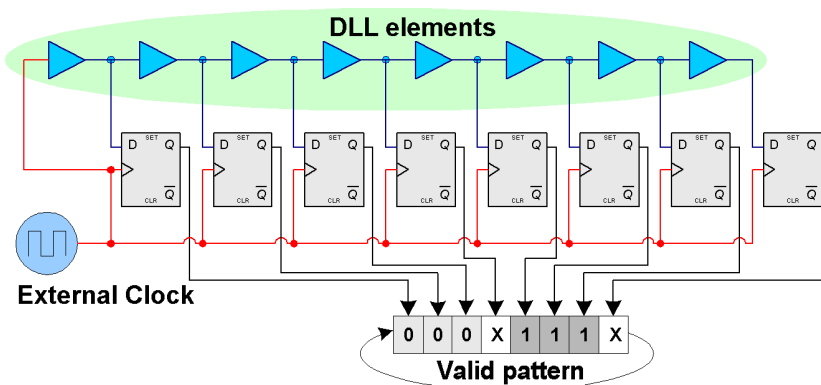


Figure 2.4 DLL "dynamic" status

2.1.1.5 Status register

A general-purpose Status Register was introduced to indicate the status of the most important components of the DTMROC. See its bit assignment in Section 2.3.2.1.4.

2.2 Input Decoding, Time Registration, Data flow, and Readout.

2.2.1 Input Level Translators: Ternary Receivers (See also section 3.1)

The communication between the ASDBLR and the DTMROC is implemented with a ternary encoded differential current. Table 2.1 gives the encoding function of the current in units “U” of current that are sourced by the by the DTMROC inputs. Typically $U = 200\mu\text{A}$.

Table 2.1 Ternary input current

Amplified Signal in the ASDBLR	True Signal	Complementary Signal
No signal above thresholds	2U	0
Signal between low and high thresholds	1U	1U
Signal above both thresholds	0	2U

The DTMROC receives ternary encoded data from the ASDBLR consisting of 0uA, 200uA, or 400uA of current leaving the TRUE or COMP inputs. The ternary receivers convert these currents back into two separate digital waveforms. The ASDBLR “A” ternary output should be connected to the DTMROC TRUE input. Under quiescent conditions (no pulse) there is 400uA leaving a TRUE port of the DTMROC. A pulse will be viewed as a rising voltage on the TRUE input. One DTMROC services two ASDBLR chips.

The Ternary Receiver circuit is capable of receiving 4ns wide (at base), tri-level differential current pulses. The circuit permits high-density communication between high gain front-end amplifiers (ASDBLR chips) and the digital DTMROC chips without driving up pin-counts and without causing self-oscillations via stray capacitive couplings back to amplifier inputs.

2.2.1.1 Testing and Bypassing Ternary Receiver Channel Zero

Unlike the DMILL version there is no special provision for testing or bypassing any of the Ternary Receivers.

2.2.2 Input Latch

The asynchronous data input from the ASDBLR has a total duration in the range from 5 ns to a few clock cycles. These signals are not synchronous with respect to the clock and in order to detect short transitions on the signal a latching mechanism has to be introduced on the Hthr output signal from the ternary receiver according to the following specification:

1. Any logical high level (active) on the Hthr signal longer than 5 ns shall be registered as a high level in the Pipeline in the following time slice. (Next leading edge of the BC clock.)
2. Measurements indicate latching on signals longer than 4ns. Still need measurement of set-up and hold times for latch function with respect to BC clock. What happens for hold times less than 1ns?

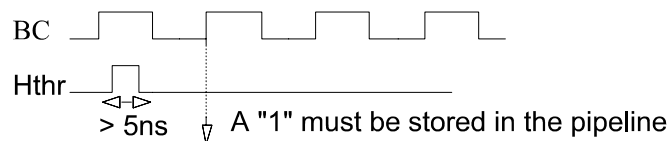


Figure 2.5 Input latch

3. Special ‘accumulation’ mode of the High Threshold signals is implemented. Bit 06 logic one of the Configuration register enables this ‘accumulation’ mode. In this case, the level one registered by the relevant latch remains high until being cleared by writing logic zero to bit 06 of the Configuration register (see 2.3.2).
4. A “wire or” logic was implemented in the ternary receivers, that allows selected DTMROC channels to contribute to the DTMROC fast trigger.

2.2.3 Time digitiser

The Lthr signal is time digitised: the level of the signal is stored each 3.125ns (25/8) leading to an 8 bit word showing the history of the signal during a clock cycle. This 8-bit word is loaded in the Pipeline.

The following specifications are required:

1. The time between 2 consecutive sampling should be 25/8 ns +/- 0.5 ns. Correct synchronisation to the Pipeline sampling time should be insured so that time intervals are attributed to the correct clock period, see 2.2.3.1
2. Special care should be taken to avoid any ambiguity during the loading in the Pipeline (see Figure 2.6) as one could easily introduce a 25 ns error if the phase between the BC8 signal and the Pipeline load is not properly adjusted. We should not have any events for which a 25 ns error is introduced, see 2.2.3.1
3. Status bits indicating the DLL operating conditions are provided, see 2.2.3.2
4. It is possible to reset (to put it in proper working conditions) the DLL with a software reset (DLL_reset) from the command decoder. The power-up circuit or an external hardware reset (hard_reset) signal will also reset the DLL
5. A 50% duty cycle clock is generated from the DLL and can be selected for operating the chip. Special circuitry with a watchdog returns the chip clock to external clock if the DLL clocks are missing, see 2.2.3.3

2.2.3.1 Time digitiser synchronisation

The 8 samples taken during one clock period (25ns) are latched by the rising edge of the BC5¹ clock, together with the Hthr bit. The 9 bits word at the output of this 9-bit latch register is sampled at the Pipeline input by the rising edge of the BC1 clock.

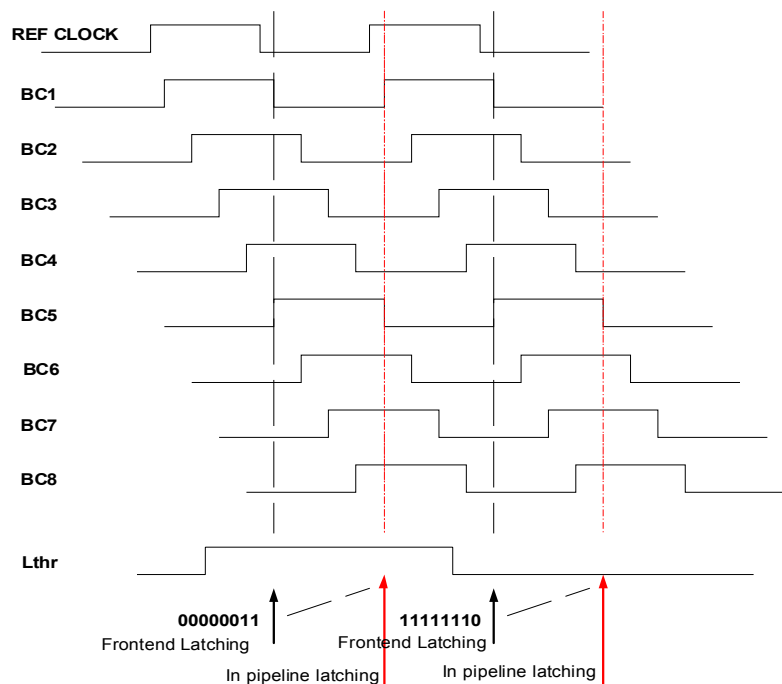


Figure 2.6 DLL clock synchronisation

¹ To be confirmed

2.2.3.2 DLL Status bits

Two status bits are provided by the DLL block :

1. DLL_STATUS bit (Bit 12 of the Status Bit register, see 2.3.2.1.4)
2. DLL_DYNAMIC_ERROR bit attached to the data stored in the Pipeline.

The DLL_STATUS bit is generated by a startup function used to force the DLL delay elements to approach the target value. The bit is set as soon as the time interval between BC1 and BC9 is less than 5ns (BC to BC delay of 2.50ns instead of 3.125ns nominal). Once set, the DLL_STATUS can only be cleared by subsequent Power_up or Hard-reset or DLL_Reset signals. The DLL_STATUS bit does not detect a DLL function failure after it has been set.

A typical value for setting up DLL_STATUS after a reset condition is 5us.

The DLL_DYNAMIC_ERROR bit is produced by a detection circuit, which samples at each external clock edge the 8 values of the BC clocks. If the sample is different from the pattern 000x111x, then the bit is set. It resumes to zero when the sample satisfies the pattern 000x111x. The DLL_DYNAMIC_ERROR bit is stored in the Pipeline together with the data of the same 25ns time period. After a positive L1, it is transferred with data to the readout buffer. When reading the bit is Ored to the ERROR Bit (see Data Format 2.2.8.1). The DLL_DYNAMIC_ERROR bit can be disconnected from the ERROR bit by the bit 8 of the Configuration Register (see Table 2.3).

2.2.3.3 DLL Clock for chip operation

The DLL provides clock edges spaced by 3.12ns with jitter less than 500ps. These edges can be used to generate an internal 25ns clock DLLCLOCK with precise 50% duty cycle. The selection of a clock with controlled duty cycle is desirable because of the clocking scheme used in the RAM blocks for the Pipeline and readout buffer.

The DLLCLOCK rising edge is synchronised to BC1, the falling edge to BC5.

A control bit CLOCKSELECT (Bit 9 of the Configuration Register, see Table 2.3) is used to select the internal clock of the chip (either external clock or DLLCLOCK). If CLOCKSELECT is zero (default value after power-up, HardReset), the external clock is used for the chip clocking. If, by writing in the Configuration Register, CLOCKSELECT is set to one, the clock issued from the DLL (DLLCLOCK) is used for the chip clocking.

To keep the control on the chip if DLLCLOCK disappears because of a DLL failure, a watchdog circuitry is implemented. After 7 to 16 missing DLLCLOCKS (compared to external clocks) the chip clock is switched back to the external clock. The status bit DLLCLOCKENABLE (Bit 13 of the Status Bit register, see Table 2.6) indicates what is the status of the clock selection.

2.2.4 Test and mask register

A 144-bit register is used either to mask the channels or to insert test data in the Pipeline. This register is serially loaded and read-out via the command decoder. The T/M bit (see 2.3.2) is used to select the mode of operation: if equal to 1 the register content is used as test input of the Pipeline; if equal to 0 it is used as a mask. After Hard or Power-on reset T/M is set to 0 (Mask mode) and no locations are masked.

2.2.5 Pipeline

The Pipeline is a synchronous dual-port static RAM memory of total storage capacity of 256x153-bit words. The whole memory space is built of 34 parallel banks of 128x9-bit words. In case of data acquisition this memory is operated as permanently running simple circular buffer. On each clock rising

edge 4 bits of the actual value of the BC ID counter and 9 (High threshold value + 8 bit time sample) data bits per channel are stored, (1+4+144) bits in total. In case of L1A recognition, the relevant read address (calculated from the actual Pipeline write address reference and the programmable L1A trigger latency offset) is generated and the data are available for the following copy operation into the Derandomizer.

The PIPELINE stores data for 256 clock cycles (25ns per cycle). The COMMAND DECODER requires 4 clock cycles to decode a L1A trigger. The effective storage time is therefore 6.3 μ s ((256-4) \times 25ns). Each data set contains 149 bits. (1-bit DLL “dynamic” error flag, 4-bits of BC ID and 16 channels \times 9-bits per channel)

If the chip is in test mode (T/M =1) the input of the Pipeline is provided by the Test and Mask register (see 2.2.4).

The parallel write access to all memory banks may cause large power consumption fluctuations with the serious consequences for the stability of the analog part of the DTMROC. To avoid this problem, every odd RAM bank has been connected to a *True* address bus and every even bank is driven by an *Inverted* address bus.

This memory is equipped with Build-In-Self-Test (BIST) controlled via the Configuration (see 2.3.2) and/or JTAG register (see 2.4.3). The BIST result can be read out from the General Status and JTAG register (see 2.3.2.1.4)

2.2.6 L1A and BC identifiers: L1ID and BCID

Two counters keep track of the number of L1A triggers and the number of Bunch Crossing clock cycles since the last reset: L1ID and BCID.

L1ID is implemented using a 3 bit counter incremented by the L1A signal decoded by the timing and control interface and reset by the Soft Reset signal or the external Hard_reset signal. It is initialised to “111” so that the first BC is numbered zero.

BCID is implemented using a 4-bit counter incremented by the BC clock rising edge and reset by the BCR signal or the Soft Reset signal from the Command Decoder or the Hard_reset signal. It is initialised to zero so the first BC is numbered one.

The output of the L1ID register is stored into the Derandomizer, unlike the BCID value which is stored into the Pipeline. Both of these ID's are used to provide the header of the data readout stream (see 2.2.8)

2.2.7 Derandomizer

The Derandomizer is an additional buffer acting as a FIFO. It is build of the same synchronous dual-port static RAM memory as the Pipeline, but half the number of banks, that gives 17 \times (128 \times 9)=128 \times 153-bit words storage capacity. Upon receipt of a L1A (as decoded by the control interface) the current Pipeline output and the following two consecutive ones are stored in the Derandomizer for readout In addition to these data, the SENDID status bit, the L1ID and the Common Error status bit are stored. This gives 441 bits¹ to be stored per event.

¹. 16 channels time 3 time slices time 9 bits, plus 9 bits for status bits

The Derandomizer can store 42 events (3 slices \times 42 events $<$ 128 locations). In case of memory overflow the control logic provides a “full” flag and skips complete events (that avoids the synchronisation troubles) until memory disposes 3 vacant locations to store subsequent event.

The Derandomizer SRAM is equipped with Build-In-Self-Test (BIST) controlled via the Configuration (see 2.3.2) and/or JTAG register (see 2.4.3). The BIST result can be read out from the General Status and JTAG register (see 2.3.2.1.4)

2.2.8 Readout

As soon as the Derandomizer is not empty the readout is placed serially on the DATA_OUT line at a 40MHz rate. The LVDS/Penn standard is used. As the event size is constant a simple protocol is used: a 3 bit preamble “101” is sent at the beginning of an event.

In case of the Read out start up or resumption, the first preamble bit is sent out 7 clock cycles after the last bit of the L1A command, otherwise the events are separated by one blank “0” bit. When idle, the data output signal is “0”.

2.2.8.1 Data format

The data format should be:

```
PREAMBLE [3 bits] “101”  
SENDID [1-bit], L1ID [3-bits], BCID [4-bits], ERROR [1-bit]  
STRAW1 BC1 [9-bits]  
STRAW1 BC2 [9-bits]  
STRAW1 BC3 [9-bits]  
...  
...  
STRAW16 BC1 [9-bits]  
STRAW16 BC2 [9-bits]  
STRAW16 BC3 [9-bits]
```

The ERROR bit represents the logical OR of some error indicators in the DTMROC listed below:

- DLL static *status* “Low”
- DLL dynamic *error* “High”, if enabled by the Configuration Register
- Internal DLL clock was selected but not allowed by “Watch Dog” circuit
- Derandomizer SRAM was full once, indicates loss of some preceding entire events
- Configuration Register parity error
- ASDBLR1 Threshold Register parity error
- ASDBLR2 Threshold Register parity error

If the chip is placed in the Send_ID mode (see 2.3.2), all the STRAW BC [9 bits] words are replaced by a 9 bits word made of the 6 bit chip address (CHIP_ID) and three zeroes. This word is repeated 48 times to comply with the normal data stream length.

The Send_ID mode format should be:

```
PREAMBLE [3 bits] “101”  
SENDID, L1ID, BCID, ERROR [9 bits]  
CHIP_ID 000 (1)  
CHIP_ID 000  
...  
...
```

CHIP_ID 000
CHIP_ID 000
CHIP_ID 000 (48)

2.2.8.2 Readout modes

Depending on the F/R bit (see 2.3.2) the full data set is transmitted (F/R=1) or the last 4 bits of the third time slice time digitiser is skipped (F/R=0). The same function applies if the chip is in Send_ID mode: the last 4 bits of every third CHIP_ID word is skipped if F/R = 0.

If placed in Time-adjustment mode (see 2.3.2) a succession of 101010... is sent. It does not depend on F/R or SENDID bits.

2.3 Command Decoder

The command decoder block receives the BC and a DATA signal from the ROD. Both signals are LVDS/Penn standard. It decodes the DATA stream and issues all the necessary timing signals (L1A,...), internal registers read/write strobes and data.

The implemented decoding algorithm is very simple. It is build of the command shift-in register, a look-up table with valid command codes and comparator logic. This architecture, in our case, is favourable over the resources consuming and heavy FSM solution. In order to insure the circuit SEU robustness some supplementary logic was incorporated. The most crucial during the data taking operation, the “fast” command (L1A, SoftReset and BunchCrossingReset) decoder was triplicated for error correction, as well as, a command length counter. A “surveillance” counter was implemented to guarantee the RTL state coverage and to release any access enduring longer then 171 clock cycles, see Table 2.2 Fields 1–6.

Upon a read request, 3 clock cycles after the last bit of the command, the command decoder serially transmits the contents of the selected register on the differential cmd_out line. This line uses the LVDS/Penn standard and is common to several chips. Therefore it has a “tri-state” capability. A 3-bit preamble is introduced [“101”] and the idle state of this line is “HiZ”.

The Table 2-4 gives the commands that must be decoded. “aaaaaa” is the chip address. If “aaaaaa” equals “111111” then all the chips are addressed (broadcast). The chip address is defined by setting external pins.

All the bits are received on the DATA input starting with the most significant one except for the testpulse delay.

2.3.1 Error handling

The protocol is based on the ABCD chip specification, which lacks any advanced protection against transmission errors. The bit patterns are however chosen such that a single bit error should not cause an acceptance of a wrong command.

The chip must take the following actions if it receives commands that it does not recognise:

Unrecognised field 1

The command decoder must flush the unrecognised field 1 and start looking at the following bit for a new command.

Unrecognised field 2

If field1 = 101 but field2 does not match a valid pattern, the command decoder must flush all 7 bits from the unrecognised field 1 and 2 and start looking at the next bit for a new command.

Field 3 < 12

If field1 = 101, field2 = 0111 but field3 is some number less than 12, the command decoder must flush 15 bits from the unrecognised fields 1,2 and 3 plus however many bits field3 designates and starts looking at the next bit for a new command.

Mismatched chip address or unrecognised field 5

If the chip address (field4) does not match the chip address established on external pins or the field5 does not match a valid pattern, the remaining bits in the input stream indicated by field3 are flushed and the command decoder starts looking at the next bit for a new command.

Table 2.2 Control and communication command field descriptions

Field 1	Field 2	Field 3	Field 4	Field 5	Field 6	Function
110						L1A (on the BC following the last bit)
101	0100					Soft Reset (on the BC following the last bit)
101	0010					BC Reset (on the BC following the last bit)
101	0111	0010 0100	Aaaaaa	000000	24 data bits	Write Configuration Register, default hex. value "00001"
101	0111	0001 1100	Aaaaaa	001010	16 data bits	Thresholds Register ASDBLR1, default hex. value "FFFF"
101	0111	0001 1100	Aaaaaa	001100	16 data bits	Thresholds Register ASDBLR2, default hex. value "FFFF"
101	0111	0001 1100	Aaaaaa	010010	16 data bits	Test Pulse Configuration, default "0000"
101	0111	0001 0100	Aaaaaa	010100	8 blank bits	DII Reset, 200ns wide, active low pulse
101	0111	0001 0010	Aaaaaa	000110	6 data bits	Test pulse delay, default hex. value "00"
101	0111	0001 0100	Aaaaaa	011000	8 blank bits	Test Pulse trigger, 200ns wide, active high.
101	0111	1001 1100	Aaaaaa	011110	144 data bits	Test/Mask register
101	0111	0001 1100	Aaaaaa	010001	16 data bits	Temperature (8msb) and Voltage (8lsb) DAC's register, default hex. value "FFFF".
101	0111	0000 1100	Aaaaaa	100011	32 data bits	Common Status Register, read only.
101	0111	0000 1100	Aaaaaa	1rrrrr		Read Registers. "rrrrr" being the register address as defined above

2.3.2 Configuration Register

The Configuration register contains **24 control bits** with the initial value at start-up is “000001”. The bit assignment is presented below, the most significant bit (MSB) <23> gets sent first.

Table 2.3 Configuration register Bit Assignment

Bits	Read/Write Significance
23:16	L1A Latency offset value. It defines the address (actual Pipeline ReadAddress – Offset) of Pipeline location to be read-out
15	SPARE External monitor (Status Register bit#26) output enable. If set, then this flag is included into the General Status bit representing the logical OR of all enabled error indicators in the DTMROC.
14	ASDBLR power supply monitor (Status Register bit#25) output enable. If set, then this flag is included into the General Status bit representing the logical OR of all enabled error indicators in the DTMROC.
13	DTMROC power supply monitor (Status Register bit#24) output enable. If set, then this flag is included into the General Status bit representing the logical OR of all enabled error indicators in the DTMROC.
12	Temperature monitor (Status Register bit#2 3) output enable. If set, then this flag is included into the General Status bit representing the logical OR of all enabled error indicators in the DTMROC.
11	Fast OR select bit. If set, Ternary Receiver Low Threshold output contributes to the Fast Or trigger. Logic zero indicates that High Threshold output is selected.
10	Fast OR enable bit. If set, a “Wire Or” of the input channels, contributing to the DTMROC fast trigger, is activated.
9	DLL clock select bit. When set, the internal on-chip 40MHz clock (if valid) is used as the system clock to run the circuit.
8	DLL “dynamic” error flag enable. If set, then flag is included into the General Status bit representing the logical OR of all enabled error indicators in the DTMROC.
7	High Threshold signals ‘accumulation’ mode enable bit. When set, the level one, once registered by the relevant latch, remains high until cleared by writing logic zero to this position.
6	Enable Pipeline and Derandomizer BIST’s. When set, the controller starts the SRAM’s self test, which lasts ~2k clock cycles. The Status and the End of Test flags are available from the Common Status Register. Must be logic zero to enable normal operation.
5	SPARE bit.
4	ASDBLR shaper select bit.
3	Test Mode bit. If set, the chip is in test mode and the Pipeline is filled with the test pattern register content. If clear, the chip is in data taking mode.
2	Time adjustment mode. If it is set, the chip transmits “010101...” on the readout data line to the ROD
1	Send-ID bit. If it is set, the chip ID (address) is sent upon a L1A reception (see 2.2.8).
0	Full/Reduced read-out bit. If it is set, the 3 BC data sets are transmitted (444 bits per event), otherwise only the first half of the last BC data is sent (380 bits per event).

2.3.2.1 Thresholds Registers 1 and 2

There are two 16 bits threshold registers. One controls the threshold setting for ASDBLR1, and the other one controls the threshold setting for ASDBLR2 (see Table 2.2). Each register sets two 8-bit voltage DAC values: One for the low and one for the high thresholds for one ASDBLR.

The data format for each of the two registers is (Bit <15> is first in serial order, the initial value at start-up is “FFFF”):

Table 2.4 ASDBLR threshold registers bit assignment

Bit <15:8>	Bit <7:0>
8 bits High Threshold; Bit<15>MSB; Bit<8>LSB	8 bits Low Threshold; Bit<7>MSB; Bit<0>LSB

2.3.2.1.1 Test Pulse Configuration

One 16 bit register controls (see Table 2.2) the Test Pulse amplitude using two 6-bit internal DAC’s: one for odd and one for even channels. The two remaining bits are used for enabling/disabling the odd/even Test Pulse generators.

The data format is (Bit <15> is first in serial order):

Table 2.5 Test pulse configuration register

Bit <15>	Bit <14>	Bit <13:8>	Bit <7>	Bit <6>	Bit <5:0>
Not used	Odd Enable Bit 1 = Enable 0= Disable	6 bits Odd channels test pulse amplitude; Bit<13> MSB ; Bit<8> LSB	Not used	Even Enable Bit 1 = Enable 0= Disable	6 bits Even channels test pulse amplitude; Bit<5> MSB ; Bit<0> LSB

2.3.2.1.2 Test Pulse Delay

The Test Pulse signal generated by the command decoder (see Table 2.2) can be delayed with a minimum delay spread of 25ns in 32 steps. The delay is controlled by 5 bits out of the 6-bit Test Pulse Delay register. The delay set by this register is not absolutely calibrated, but it guarantees that the test pulse delay spreads over more than one clock cycle for all conditions of operations and process. The typical time step for delay adjustment is 1.5ns.

Table 2.5 Test pulse delay register

Bit <5 >	Bit <4 :0>
Unused	Bit<4> = MSB Bit<0> = LSB

2.3.2.1.3 Test pulse Shape

The two test-pulses (odd and even) are generated from a voltage step whose amplitude is fixed by the Test pulse Configuration register (see 2.3.2.1.1) and timing is fixed by the Test pulse delay register (see 2.3.2.1.2).

The test-pulses’ DAC’s provide the voltage step amplitude for odd and/or even channels and the Test pulse delay circuit provides the time with a typical 1.5ns step resolution at which the pulse(s) is (are) applied.

When connected to the ASDBLR inputs, TST_E and TST_O, the DTMROC outputs, tp_odd and tp_even will produce currents at the odd and even channel inputs to the ASDBLR preamp that closely mimic the

current pulse produced by the TRT straw filled with an Xe/Ar/CO₂ gas. The anticipated stray capacitance of the interconnect between the DTMROC and ASDBLR is 7pF.

2.3.2.1.4 Common Status Register

A general-purpose **32-bit** register representing specific information concerning the DTMROC operating conditions or error flags has been implemented.

Table 2.6 Common Status register Bit Assignment

Bits	Read Significance
31 : 27	SEU statistics. It represents the number of detected (and, hopefully, recovered!) SEU's. These SEU's are coming from: FastCommand Decoder, Configuration Register, Threshold1&2 Registers, EventLength Counter, L1_ID and BC_ID circuitries. Total number of FF's = ???.
26	SPARE External sense comparator output, set if the input is larger than the DAC set point.
25	ASDBLR power supply sense comparator output, set if the input is larger than the DAC set point.
24	DTMROC power supply sense comparator output, set if the input is larger than the DAC set point.
23	Temperature sense comparator output, set if the input is larger than the DAC set point.
22	Voltage and Temperature sense DAC's register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by SoftReset.
21	Test Mask register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by SoftReset.
20	Test Pulse Delay register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by SoftReset.
19	Test Pulse Configuration register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by Soft Reset.
18	Threshold-2 register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by SoftReset.
17	Threshold-1 register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by Soft Reset.
16	Configuration register SEU flag. It indicates, when set, that the parity logic has detected SEU in this circuit. Remains set until being cleared by Soft Reset.
15	Serializer error flag. If set then output data might be corrupted (the event length is OK).
14	Derandomizer full flag, indicates data loss (complete event, no synchronisation troubles)
13	DLL clock enable bit. Set if internal on-chip 40MHz DLL clock is selected (bit<09> in Configuration register) and considered as "Valid" to run the circuit.
12	DLL static status, set when DLL has been locked.
11	Derandomizer BIST result flag. If self-test is disabled must be logic one. When test is enabled and ended (bit#10), logic one indicates a failure.
10	Derandomizer BIST progress flag. When set, Derandomizer self test is ended and the test result flag (bit#11) is valid.
9	Pipeline BIST result flag. If self-test is disabled must be logic one. When test is enabled and ended (bit#8), logic one indicates a failure.
8	Pipeline BIST progress flag. When set, Pipeline self test is ended and the test result flag (bit#9) is valid.
7	Slow command unrecognised field
6	Fast (L1A, SoftReset, BCReset, StartSlowCommand) command unrecognised field
5 : 0	Chip 'geographic' address

2.4 Miscellaneous

2.4.1 DTMROC Reset list

Table 2.7 Various reset actions

Reset Name	Action on the relevant circuit									
	Command Decoder	Pipeline and Derandomizer Controller & FULL flag	Serializer readout & Error flag	D L L	L1 ID	BC ID	Config Threshold Mask registers	Unrecognized command flags	SEU Parity Error flags	SEU statistic counter
Power UP	R	R	R	R	R	R	P	R	R	R
Hard Reset	R	R	R	R	R	R	P	R	R	R
Soft Reset	-	R	R	-	R	R	-	R	R	R
BC Reset	-	-	-	-	-	R	-	-	-	-
DLL Reset	-	-	-	R	-	-	-	-	-	-

R - indicates reset to "0"

P - indicates preset to the initial value, see the Table 2.2.

2.4.1.1 Power-up Reset

A trigger circuit comprised of three PMOS and three NMOS transistors monitors the difference between Vdd and a diode referenced input. The output, **power_up_resetb** is set initially high and goes low when Vdd > 1.6V. After power-up the chip should be in a known state and work without external intervention. The chip should be in the same state as after a HardResetB.

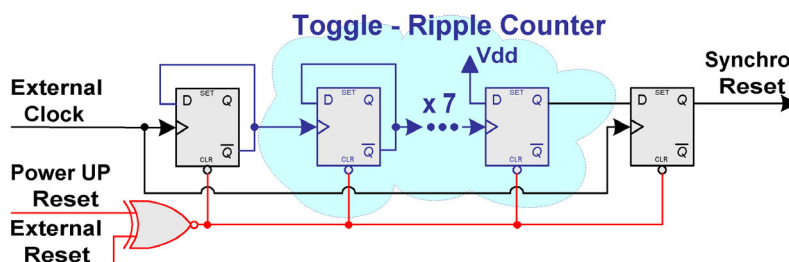
See writeup under <http://www.hep.upenn.edu/atlas/dtmroc> Custom Analog Blocks

2.4.1.2 Hard reset

A hard reset input is provided. It must be LVDS compliant. An active low signal on the hard reset input lasting longer than 3 clock cycles, is accepted as a valid hard reset, otherwise it is rejected. After a hard reset the DLL should be locked, the masks should be off, the chip should be in normal data taking mode and the Pipeline and Derandomizer pointers are reset. The DAC threshold values will be reset.

Some logic was implemented to mix the PowerUp and HardReset signals and to insure the clean start up and initialisation conditions. An active reset input, the only one at the same time, is extended by 129 external clock cycles and the supplied output is synchronous with the negative edge of this clock. The schematics of this circuit is presented below, all inputs/outputs are active low.

Figure 2.7 Power-Up and Hard Reset stretcher/synchronizer



2.4.1.3 Soft reset

A Soft Reset command is provided through the serial DATA input of the chip and the Command Decoder (see Table 2.2). The “SoftResetB” signal provided by the command decoder is the logical sum of PowerUpB and HardResetB signals and Soft Reset command. The SoftResetB does not change internal register values. It resets the command decoder, the Pipeline and Derandomizer controller and the event readout sequencer.

2.4.1.4 DLL reset

A DLL Reset command is provided through the serial DATA input of the chip and the Command Decoder to reset only the DLL.

2.4.1.5 Bunch Crossing Reset (BCR)

A Bunch Crossing Reset command is provided through the serial DATA input of the chip and the Command Decoder (see Table 2.2). The “BCresetB” signal provided by the command decoder is the logical sum of PowerUpB and HardResetB signals as well as Soft Reset and BC Reset commands (see 2.2.6).

2.4.2 Threshold DACs.

(see also <http://www.hep.upenn.edu/atlas/dtmroc> > Custom DSM Analog Blocks > *Dual 8 bit D/A Block.*)

2.4.2.1 The DSM_DTMROC has 4 8 bit DACs intended to control the Tracking and Transistion Radiation discriminators on the two ASDBLR ASICS it is paired with. The voltage output is produced by passing a current through an internal resistance of 5K. Ideally a threshold register setting of 255 (see 2.3.2.1) should produce an output of 1.25V. An internal band gap provides an absolute reference. Steps are linear in increments of ~5mV starting at 0V.

2.4.2.2

2.4.3 JTAG Logic Implementation and Access.

Three mandatory and four optional instructions defined by the IEEE Std 1149.1 are supported. The “Hard_Reset” input is reserved as an optional asynchronous TAB controller reset, active low.

Instruction Register:

- *BYPASS* - 11111
- *EXTEST* - 00000
- *SAMPLE* - 00010
- *INTEST* - 00100
- *IDCODE* - 00001
- *RUNBIST* - 10000
- *SCAN_PATH_TEST* - 01000

Test data registers:

- *Bypass* - mandatory, length 1
- *Boundary* - mandatory, length 48
- *DEVICE ID* - optional, length 32
- *SCAN_PATH_REG* - optional, length 689
- *JTAG_BIST_REG* - optional, length 8/3076

IDCODE capture value:

- Manufacturer ID - 24
- Part Number - 4535
- Version Number - 3

Table 2.8 Boundary Scan Register implementation

INDEX	PORT	PACKAGE PIN	FUNCTION	CELL
47	address0	P1	input	BC_2
46	address1	P2	input	BC_2
45	address2	P3	input	BC_2
44	address3	P4	input	BC_2
43	address4	P5	input	BC_2
42	address5	P6	input	BC_2
41	tern00_comp	P7	input	BC_2
40	tern00_true	P8	input	BC_2
39	tern01_comp	P9	input	BC_2
38	tern01_true	P10	input	BC_2
37	tern02_comp	P11	input	BC_2
36	tern02_true	P12	input	BC_2
35	tern03_comp	P13	input	BC_2
34	tern03_true	P14	input	BC_2
33	tern04_comp	P15	input	BC_2
32	tern04_true	P16	input	BC_2
31	tern05_comp	P17	input	BC_2
30	tern05_true	P18	input	BC_2
29	tern06_comp	P19	input	BC_2
28	tern06_true	P20	input	BC_2
27	tern07_comp	P21	input	BC_2
26	tern07_true	P22	input	BC_2
25	tern08_comp	P23	input	BC_2
24	tern08_true	P24	input	BC_2
23	tern09_comp	P25	input	BC_2
22	tern09_true	P26	input	BC_2
21	tern10_comp	P27	input	BC_2
20	tern10_true	P28	input	BC_2
19	tern11_comp	P29	input	BC_2
18	tern11_true	P30	input	BC_2
17	tern12_comp	P31	input	BC_2
16	tern12_true	P32	input	BC_2
15	tern13_comp	P33	input	BC_2
14	tern13_true	P34	input	BC_2
13	tern14_comp	P35	input	BC_2
12	tern14_true	P36	input	BC_2
11	tern15_comp	P37	input	BC_2
10	tern15_true	P38	input	BC_2
9	ConfigSpare	P46	output	BC_1
8	ShaperSelect	P47	output	BC_1
7	EnableDecoup2	P52	input	BC_2
6	cmd_in	P54	input	BC_2
5	bc	P56	input	BC_2
4	hard_reset_B	P58	input	BC_2
3	*	-	control	BC_2
2	cmd_out	P62	output	BC_1
1	data_out	P64	output	BC_1
0	EnableDecoup1	P65	input	BC_2

3 I/O

Input Protection -- All inputs and outputs include input protection. Low level inputs and outputs, test pulse and reference lines use specially designed analog input protection pads. Tests of this input protection up to 8mA show that they act as ideal diodes in series with $\sim 50\Omega$.

The Maximum Voltage on any input is: $V_{dd} + 1$ diode drop, $0V - 1$ diode drop.

3.1 Inputs

3.1.1 Power -

V_{dd} Operating Range ≈ 2.1 to $2.7V$

Current Requirement – $\approx 120mA$ @ $2.5V$ See Figure 3.1 below.

** note that there is a $\sim 25\%$ reduction in power with the BC clock Off.

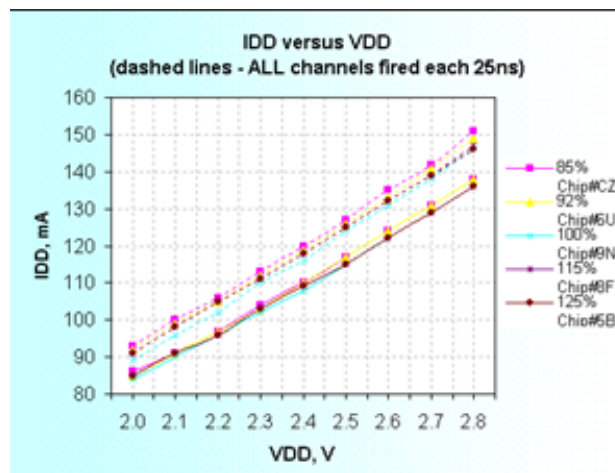


Figure 3.1 Measured DTMROC -S current requirement versus Vdd. Clock is ON.

There are 5 voltage domains on the ASIC that should be connected in common at the board level.

- Digital – power for all core digital logic.
- Analog - Power for Test Pulse and D/A's and Sense circuits
- Ternary Receivers – Power for 16 Ternary Receivers
- DLL – Power for DLL and clock drivers.
- Shield – fixes substrate potential between Analog and Digital domain

3.1.2 Ternary Inputs

(see also section 2.2.1 and <http://www.hep.upenn.edu/atlas/dtmroc> under Custom DSM Analog Blocks - Ternary Receiver)

The DTMROC has 16 ternary receivers used to decode timing and two levels of threshold status from eight channels each on two ASDBLR chips. The ternary encoding logic scheme is described in 2.2.1 From a system perspective it is important to note that this is a constant

current technique. As shown in Table 2.1 a constant current of 2 "U" drawn from each ternary receiver is split between its differential inputs in one of three ways. The ternary receiver provides two relatively low impedance inputs referenced internally to about 1 Volt to ensure that the ASDBLR (current source) outputs do not go into saturation. The terms "True" and "Comp" that accompany the ternary receiver input pin names are chosen to indicate the voltage excursion expected (using an oscilloscope probe) as an input goes from a quiescent to an active state where "True" indicates a positive going excursion and "Comp" indicates a negative (higher current) excursion. *The ASDBLR "A" ternary output should be connected to the DTMROC TRUE input.* Typically the ASDBLR will provide current units, "U" of -200µA (A total of -400µA per ternary receiver), however the absolute magnitude of the current unit may vary as follows:

Current Unit Magnitude	-200µA (-40µA, + 100µA)
Fractional Unit Switching	1 ± 0.1U
Minimum Switching Duration	4ns

Table 10 Input Impedance of the DSM Ternary Input

Input Current	Approximate Input Impedance
0 µA	470Ω (@ ~1V)
200µA (1 "U")	300Ω
400µA (2 "U")	180Ω

Power - each ternary receiver requires 2.5mW at Vdd= 2.5V

Input Protection – Input protection pads are used to allow normal handling of the inputs although static discharge should be avoided. The inputs are NOT intended for a voltage input.

3.1.3 LVDS Inputs : Clock, Hard Reset, Command In –

The LVDS receiver is a standard cell block from CERN (LVDS_RX) that should be able to decode differential input amplitudes as small as 50mV. It provides high impedance inputs and has input protection.

Power – 8.4mW

Input Specification:

xx_pos → rising edge true

xx_neg → falling edge true

Differential Swing -

$$100\text{mV} < \text{Swing} < 500\text{mV}$$

Common mode $V_{dd}/2 \pm 200\text{mV}$

3.1.4 Address inputs (0-5) -

Single ended static inputs with input protection.

Vdd = high Gnd = Low

3.2 Outputs

3.2.1 Data Output Drivers - (Data out and CMD out)

(see also <http://www.hep.upenn.edu/atlas/dtmroc> Custom DSM Analog Blocks - LVDS Driver and LVDS Driver for CMD Out)

3.2.1.1 CMD Out

Outputs - *CMD_out_pos*, *CMD_out_neg*

Electrical Specification - The data output driver is a high impedance matched differential current loop with a programmable current intended to drive twisted pair cable. Loop current is programmed by the *AdjCur_cmd* pad.

Hookup Requirements - outputs should be held to a common mode voltage of $V_{dd}/2 \pm 250mV$. The absolute value of the common mode voltage is set by the user. Impedance of line should limit switching transient to $< 500mV$.

3.2.1.1.1 CMD Out Operational Modes

Tristate – No output current.

Data - 3mA source/sink Max with *AdjCur_CMD* attached to Vdd. **Loop Current $\approx (1.6 * V_{dd} - 1.0)mA$**

Wire Or - Unmasked Ternary outputs are ‘OR’ed together.

In **quiescent mode** the output current is near zero so that several DTMROC chips may be connected in parallel without increasing the offset. When an unmasked ternary input is detected, the output will switch a current of $1/2$ of the CMD data mode current to the outputs, sourcing current from the “pos” output and sinking it to the “neg” input.

High or Low Ternary level inputs can be selected to trigger **Wire Or** outputs using **bit 11** of the **configuration register**.

(See Table 2.3 Configuration register Bit Assignment)

3.2.1.2 Data Out --

Outputs - *Data_out_pos*, *Data_out_neg*

Operational Mode Always enabled for Data Output. Same as Data mode outputs above except *AdjCur_data* input is used to program current (3mA current loop Max with *AdjCur_data* attached to Vdd @ $V_{dd}=2.5V$)

Hookup Requirements (Same as CMD Out Data) Set common mode voltage of $V_{dd}/2 \pm 250mV$. The absolute value of the common mode voltage is set by the user.

3.2.2 Test Pulse Outputs –

The DTMROC has two test pulse outputs, **tp_even** and **tp_odd**, intended to provide test input

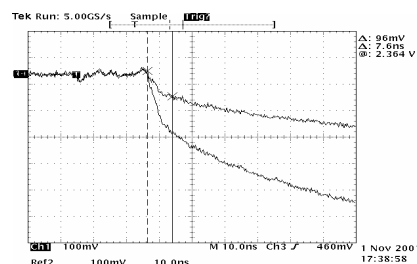


Figure 3.2 DSM Test Pulse output

to even and odd channels on both ASDBLR chips simultaneously. The signal shape generated is the integral of the expected point ionization signal in a TRT straw. A 200fF capacitor at the input to each channel of the ASDBLR differentiates this signal to inject a signal typical of that expected in the straw. The absolute calibration is not expected to be better than $\pm 20\%$. But it should serve to indicate the data path integrity and help decipher if the straw is connected to the input. The measured output from a test block fabricated in a multi-project run is shown in Figure 3.1. (See <http://www.hep.upenn.edu/atlas/dtmroc> >Custom DSM Analog Blocks > Xenon Test Pulse Output)

3.2.2.1 Amplitude -

Two 6 bit D/A's (see Table 2.1) set the test pulse output amplitude for values between 0 and 50fC of input charge. The external connection *tp_bias* can be used to adjust the output range. Nominally a 9K Ω resistor will be used between *tp_bias* and 0V.

3.2.2.2 Timing Delay -

The delay of both test pulse outputs relative to the BC clock is controlled by a single 5 bit register that gives a delay range of approximately 1ns per count.

3.2.2.3 Enable and Disable -

Bits 14 (odd) and 6 (even) provide individual enables for the test pulse outputs.

3.3 Temperature and Voltage Sensing -

A simple measuring scheme is used to monitor on chip temperature, Vdd voltage and two off chip sense input voltages.

A monitored voltage is compared to a programmed D/A value (See Table 3.11) using a low offset comparator. The comparator output voltage is stored in the Common Status Register (See Table 3.12).

Note that the MAX D/A value is 1.25V so resistor ratios are used to proportionally monitor higher voltages. Input 'Jmp' leads allow on chip ratios to be employed.

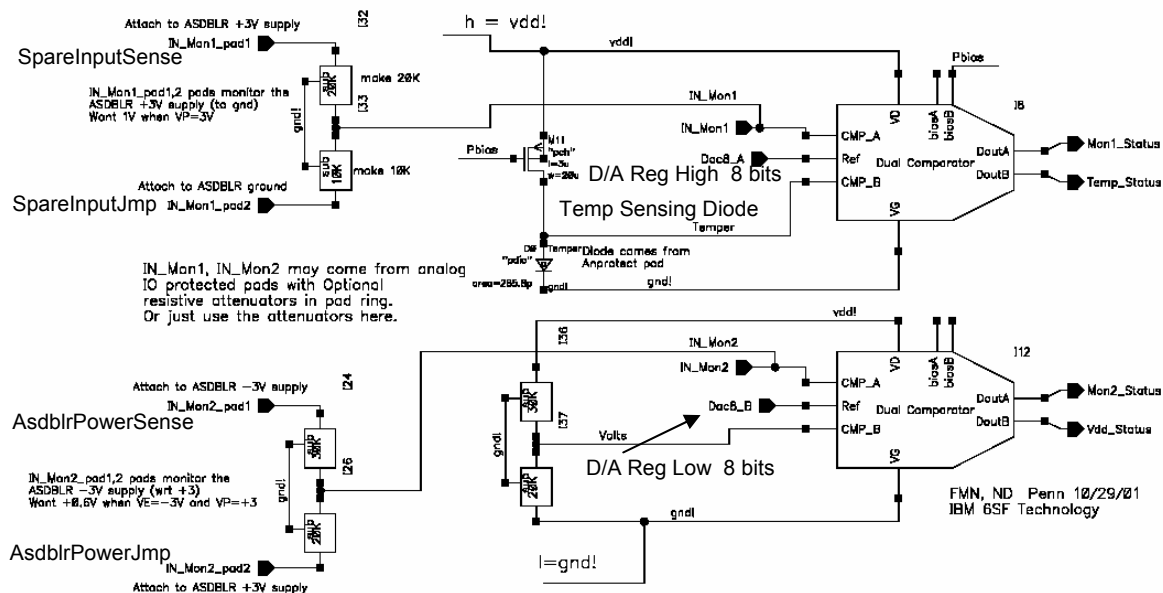


Figure 3.3 Block Schematic of Monitoring Circuit. Inputs for Vdd, temp, and two external voltages are provided.

(See <http://www.hep.upenn.edu/atlas/dtmroc> >Custom DSM Analog Blocks > Voltage and Temp Sense Block)

3.3.1 Vdd Monitoring - Bit 24 of CSR - $V_{dd} \approx (.014 * DAC - .1)V$

An internal ratio of 2/5 is employed monitoring Vdd with 30K Ω and 20K Ω connected in series. The common resistor node is monitored and compared with the low byte of the monitor D/A register. (See Table 3.13)

3.3.2 Temp Monitoring – Bit 23 of CSR $Temp \approx (-2.85 * DAC + 400)C$

A constant current of approximately 17 μ A is used to bias a diode similar to that used in the analog protection pad. Uses the high order byte of the monitor D/A register.

Maximum Voltage on any input is: Vdd + 1 diode drop, 0V – 1 diode drop.

3.3.3 Spare Input -- Bit 26 of CSR

Useful Monitoring range - 0V – 1.2V
High Byte of Monitor D/A reg.
Resolution 5mV per D/A count

Spare Input Jump

Attenuates the Spare input DC by 1/3. Internal $V = 2/3$ Spare input Voltage + reference level (usually GND) that *Spare input Jump* is referenced to.
Resistance between *Spare input* and *Spare input Jump* is 30K Ω .

This input was intended for use when monitoring the ASDBLR +3V supply, but since the protection diode will limit at Vdd + 1 diode drop an external resistor divider must be used for this function. In this case Spare Input Jump should **not** be used since it will attenuate on the chip as well.

3.3.4 AsdblPowerSense (input) Bit 25 of CSR

Useful Monitoring range - 0V – 1.2V
Low byte of D/A monitor register.
Resolution 5mV per D/A count.

AsdblPowerJump (input)

Attenuates the voltage on *AsdblPowerSense* by 3/5 when attached to a voltage reference, usually GND.
Resistance between *AsdblPowerSense* and *AsdblPowerJump* is 50k Ω .

4 Pin List, Die and Packaging info

The pins of the chip are listed here first by functionality type and I/O characteristics. The pad frame is shown in section 4.2 and bonding diagram for the FBGA version in Section. Note that the pin names are preliminary and need to be made consistent with ASDBLR and ROD/TTC names and with internal block names.

4.1 Functionality List

4.1.1 Inputs

Ternary Inputs from ASDBLR –

- Ternxx_true <xx=15..0>
- Ternxx_comp <xx=15..0>

LVDS Control Inputs – from TTC

- bc_pos -- Beam Crossing Clock
- bc_neg
- cmd_in_pos -- Commands to the DTMROC
- cmd_in_neg
- hard_reset_pos -- Hard Reset
- hard_reset_neg

CMOS Level Static Inputs - hard wired on the board or cable

- address<5..0>

Reference Inputs – hard wired resistor on board

- AdjCur_data – Bias to adjust LVDS current out for Data_Out (Vdd nominal)
- AdjCur_cmd – Bias to adjust LVDS current out for Command_Out (Vdd nominal)
- tp_bias – Test Pulse Bias (9K Res to 0V)

Voltage Sense Inputs (to on board comparators)

- SpareInputSense - Spare comparator input.
- SpareInputJump - Jumper to GND to invoke resistor attenuator.
- ASDBLRpowerSense - ASDBLR +3V power supply sense or other voltage input.
- ASDBLRpowerJump - Jumper to GND to invoke resistor attenuator.

Decoupling Capacitor Control – Allows internal capacitor filter banks to be enabled.

Vdd = enable on chip decoupling caps

- enable_decoupling_1 2 leads.

4.1.2 Outputs

LVDS Data Outputs – to ROD (Data) and TTC (Command) Current Loop Outputs 3mA @Vdd
= 2.5V must terminate into $\sim VDD/2$

Polarity : pos -->Positive going voltage transition for logic transitions

- data_out_pos
- data_out_neg
- cmd_out_pos
- cmd_out_neg

Control Outputs – full scle CMOS (0:2.5V)

- Shaper Select – select Xe or Ar shaping function on ASDBLR
- Spare 1 – not necessarily bonded out
- Analog Outputs – to ASDBLR (0-1.2V)
 - threshold0_low
 - threshold1_low
 - threshold0_high
 - threshold1_high
 - Test_Pulse_even
 - Test_Pulse_odd

4.1.3 Power – from board (Vdd = 2.5 ±0.25V @ ≈120mA, Gnd = 0V)

Power on the Die is separated into five regions:

Digital - all core logic functions

Shield - Shield between Analog and Digital substrate regions intended as stable reference for substrate.

Analog - D/A, Test Pulse

DLL - DLL block and Clock generation

Ternary - Ternary Receiver.

Off Chip Power and GND pads may be connected in common to their respective voltage levels.

- VDD_digital – common Digital/Analog at board level.
- VDD_ternary – Separate power for Ternary Inputs.
- VDD_shield – Vdd Shield implant Separates Analog and Digital regions.
- VDD_analog – Analog power for D/A and Test pulse.
- VDD_DLL – DLL and clock power.
- GND_digital – Core logic power return.
- GND_ternary – Ternary Rcvr power return.
- GND_shield – Substrate Gnd reference between analog and digital regions.
- GND_analog – Analog power return.
- GND_DLL – DLL and clock power return.

4.1.4 Test Signals

- JTAG – all CMOS levels (0:2.5V)
 - TDO JTAG data output
 - TMS JTAG mode select
 - TDI JTAG data input
 - TCK JTAG clock
 - TRST JTAG reset

4.2 Pad Frame Drawing Die Size: 5mm X 5.2mm

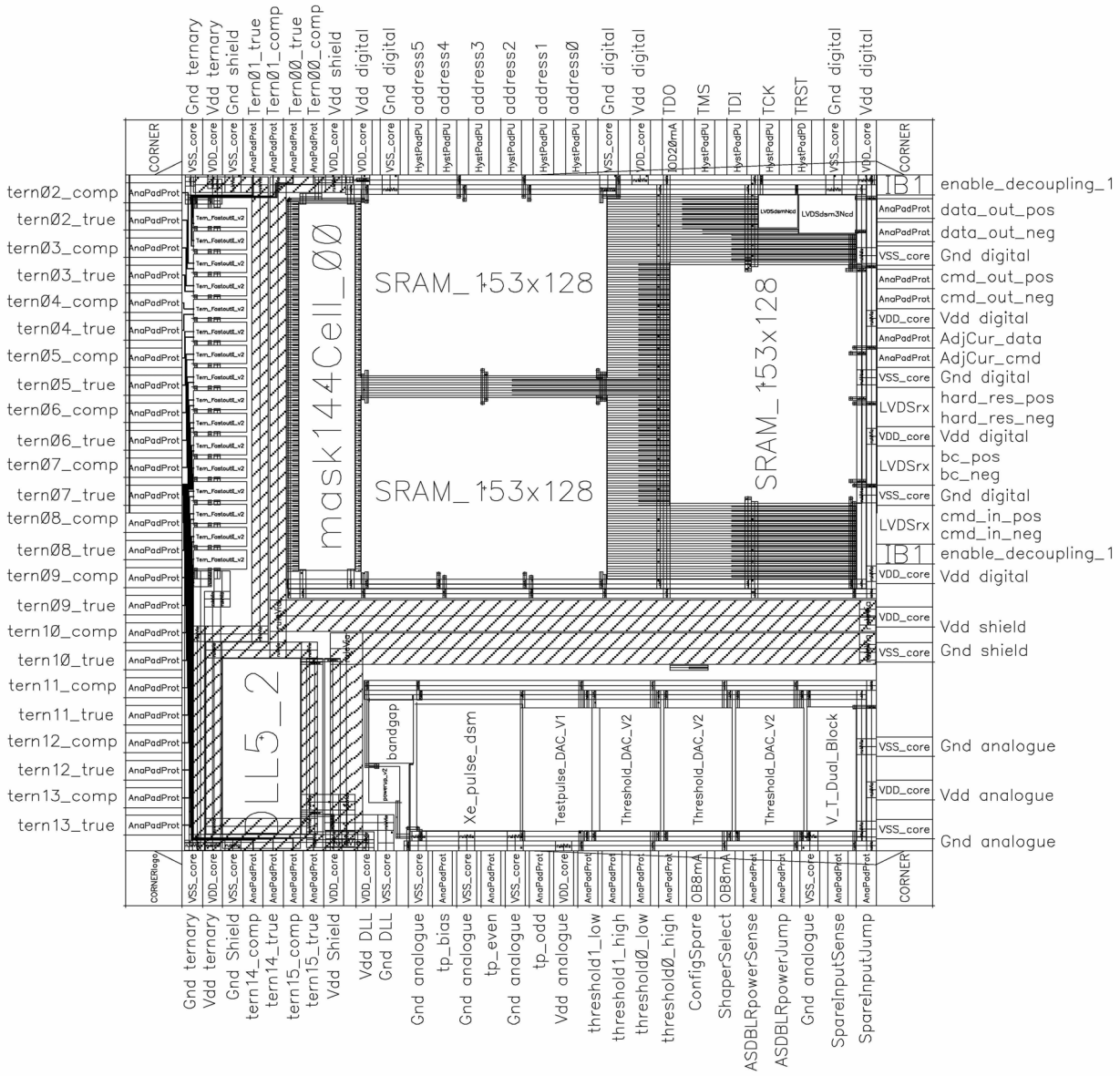


Figure 4.1 DSM DTMROC (DTMROC –S chip) pad frame

4.3 FBGA package Size: 11mm x 13mm

A custom 11mm x 13mm package has been design for the DTMROC – S chip. The bonding diagram with a ball mapping indication is shown in the figure below. The ball grid is a 10X10 array with 0.8mm spacing.

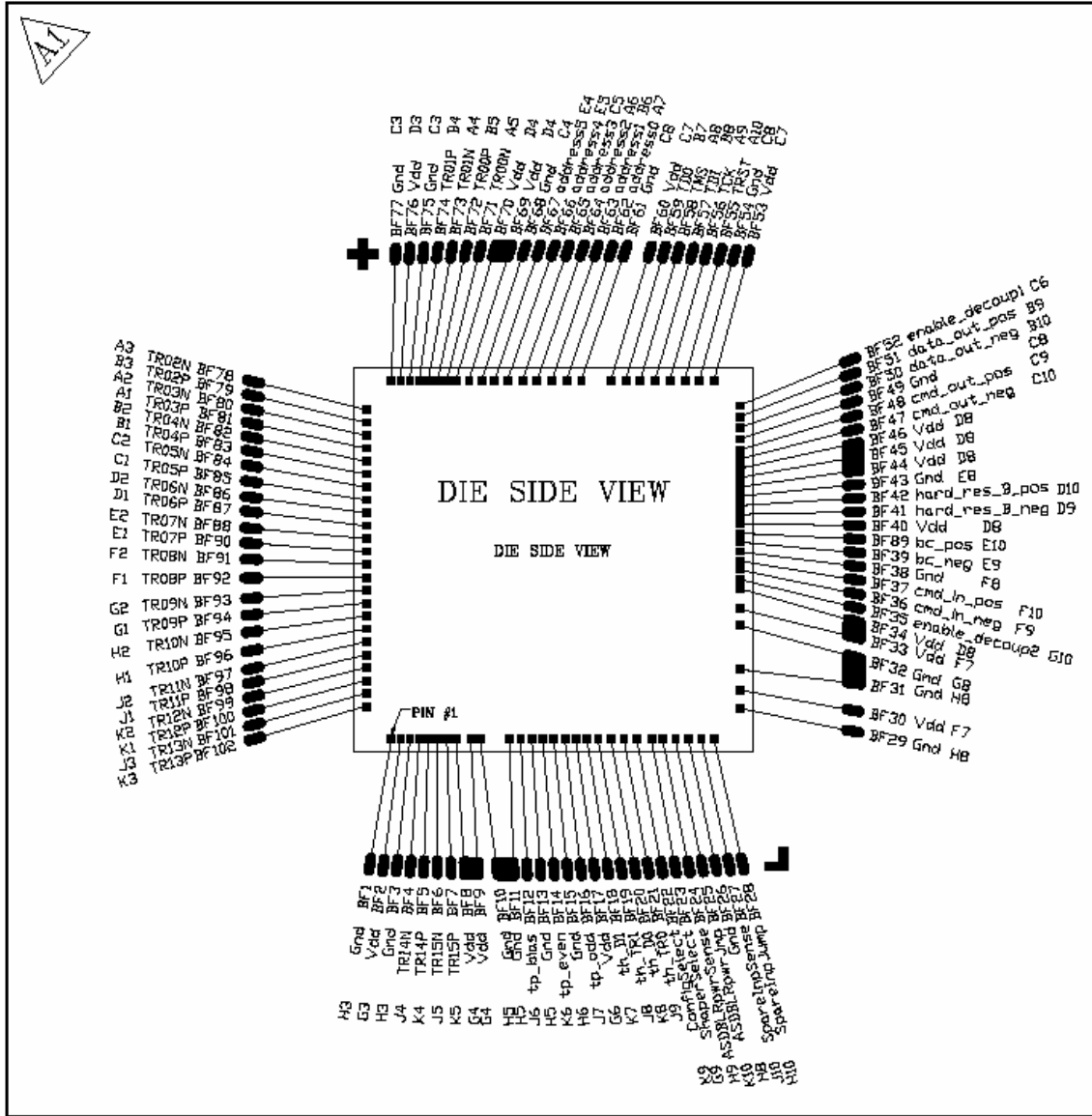


Figure 4.2 FBGA bonding Diagram