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Design and implementation of the ATLAS TRT front end electronics

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Abstract

The ATLAS TRT subsystem is comprised of 380,000 4 mm straw tube sensors ranging in length from 30 to 80 cm. Polypropelene plastic layers between straws and a xenon-based gas mixture in the straws allow the straws to be used for both tracking and transition radiation detection. Detector-mounted electronics with data sparsification was chosen to minimize the cable plant inside the superconducting solenoid of the ATLAS inner tracker. The "on detector" environment required a small footprint, low noise, low power and radiation-tolerant readout capable of triggering at rates up to 20 MHz with an analog signal dynamic range of >300 times the discriminator setting. For tracking, a position resolution better than 150 μm requires leading edge trigger timing with ~1 ns precision and for transition radiation detection, a charge collection time long enough to integrate the direct and reflected signal from the unterminated straw tube is needed for position-independent energy measurement. These goals have been achieved employing two custom Application-specific integrated circuits (ASICS) and board design techniques that successfully separate analog and digital functionality while providing an integral part of the straw tube shielding.

Keywords: ATLAS; TRT; ASDBLR; DTMROC

1. Introduction

The detector-mounted front end electronics for the ATLAS TRT [1] is currently being installed on the detector in the ATLAS surface building, SR-1 at CERN. It is the product of a decade-long development to meet the conflicting constraints of radiation tolerance, power and performance in the LHC environment. The TRT straw tubes will operate at a gain of 2×10^4 with a gas mixture of $70\%Xe+27\%CO_2+3\%O_2$ to allow prompt collection of the primary electrons and efficient conversion of the higher energy transition radiation (TR) photons. The cathode of the straw tubes will operate at negative high voltage and the anode wire will directly connect to the input of the readout electronics. Predicted radiation levels in the region of the detector for a 10 yr exposure are 3×10^{14} neutrons / cm^3 and 10 Mrad ionizing radiation, well beyond the capabilities of most present day commercial electronics. The high fluence of ionizing particles adds single event upset (SEU) as a potential problem as well as long term damage. Table 1 summarizes the front end electronics perfomance specifications that have evolved based on detector requirements and the limits of available technology. The high channel count and high density interconnect led us to develop application-specific integrated circuits (ASICS) that reduce component cost, cable plant and offer superior EMI immunity in the high-density detector environment. It was decided upon early to separate the functionality into an analog signal processing ASIC and a digital ASIC to digitize time, provide data readout sparsification, and control levels for the Analog ASIC.

The amplifier, shaper, discriminator and baseline restorer (ASDBLR) [2,3] provides the complete signal processing chain for eight channels of straw anode input. A three-level differential digital output for each channel signals the time over a tracking, "low" level, and TR, "high" level, programmable threshold.

The sixteen-channel digital time measurement and read out chip (DTMROC) [4,5] encodes time over the low threshold in 3.1 ns time bins, and the time over the high threshold in 25 ns bins, based on the 40 MHz beam crossing clock. The nine bits of digital time information per crossing for each channel is stored in a programmable-depth

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Table 1
ATLAS TRT front end electronics characteristics

Peaking time for track detection	7.5 ns
Peaking time for TR photon detection	10–12 ns
Double pulse resolution	25 ns
Maximum straw triggering rate	<20 MHz
Intrinsic electronics noise	<0.3 fC RMS
Operational track disc threshold	2 fC
Maximum threshold for TR photons	120 fC
Total on detector power	80 mW/Ch
10 year neutron exposure	3×10^{14}/cm^2
Total dose (10 yr) ionizing radiation	10 Mrad

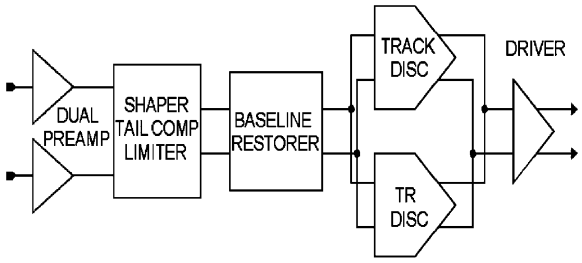

Fig. 1. Block diagram of a single ASDBLR channel.

pipeline awaiting a delayed Level 1 trigger decision. A derandomizing buffer provides data sparsification going from the 20 MHz individual straw triggering rates to the (maximum) 75 KHz ATLAS Level 1 readout rate.

The two basic straw arrangements around the beam, axial and radial, in the barrel and endcap TRT led to two different printed circuit board approaches to mount the electronics on the detector as discussed in Section 3.

2. The TRT ASICS

The following sections provide a short description of the two TRT ASICS. More complete descriptions can be found in Ref. [2–6].

2.1. The ASDBLR

The ASDBLR requires 36 mW per channel and provides the complete analog signal processing chain for eight straw tubes. Fig. 1 shows the block diagram for a single channel. The low-noise dual preamp provides a DC-balanced signal to the shaper stage with a gain 1.5 mV/fC and peaking time of 1.5 ns for an impulse input. Dual inputs provide common mode pick-up rejection both on and off chip.

The three-stage shaper and preamp together provide four equivalent 1.5 ns poles of shaping to produce a nearly symmetric response with ~5 ns peaking time for a straw point ionisation input. The first shaper stage converts the dual preamp output to a differential signal with a gain of two. The second stage provides ion tail cancellation for either xenon or more conventional argon-based gases, as selected externally. A full scale range of 600 fC allows the tail cancellation to be effective over the widest feasible range of charge depositions. The final shaping stage contains a pole–zero network that cancels the short tail added by preamp feedback components and limits the maximum output response of the shaper to 120 fC equivalent input, the largest expected threshold setting for the TR discriminator.

The differential signal from the shaper is AC-coupled through 8 pF capacitors from input to the output buffers of the baseline restorer (BLR). A bridge diode network with dynamic current control is used as a variable impedance between the differential outputs. Current in the bridge determines the differential impedance and is dependent on the polarity of the output. The impedance increases as signals of the desired polarity are passed on to the discriminator, and when the shaper output returns to baseline, any overshoot due to discharge of the coupling capacitors is quickly eliminated by an increase in current in the bridge, lowering it's impedance.

The track discriminator adds 2.5 ns to the peaking time in the first stage and can reliably be set to trigger on signals between 1 and 10 fC. The TR discriminator utilises the same basic configuration, but has a 10 : 1 attenuation at it's input and adds 5 ns to the shaping time to allow integration of the prompt and reflected straw signal for accurate detection of the TR photons.

The track and TR discriminators switch separate 200 μA currents between shared differential outputs to form a current sum of the combined discriminator outputs. This ternary encoding scheme is based on the assumption that the track discriminator output is always present when the TR discriminator is triggered due to it's lower threshold [3].

Our radiation tests have shown that the ASDBLR is capable of withstanding the predicted 3×10^{14} (1 MeV NIEL) neutrons/cm^2 and 5 Mrad ionizing radiation without substantial performance shifts, although it has also been shown that unexpectedly high levels of thermal neutrons in addition to the expected neutron dose would compromise the expected useful lifetime of the ASDBLR [6].

The ASDBLR was fabricated in a radiation tolerant BiCMOS technology that was under development for the space and military community.

2.2. The DTMROC

The main functional blocks of the DTMROC are shown in Fig. 2. A multi-institutional design team was utilized to meet the complex functional design requirements of this mixed analog and digital ASIC. Production ASICS have been fabricated by 0.25 μm minimum feature size commercial CMOS process, using edgeless transistors and library blocks that have been shown to be radiation tolerant well beyond the levels required by the TRT.

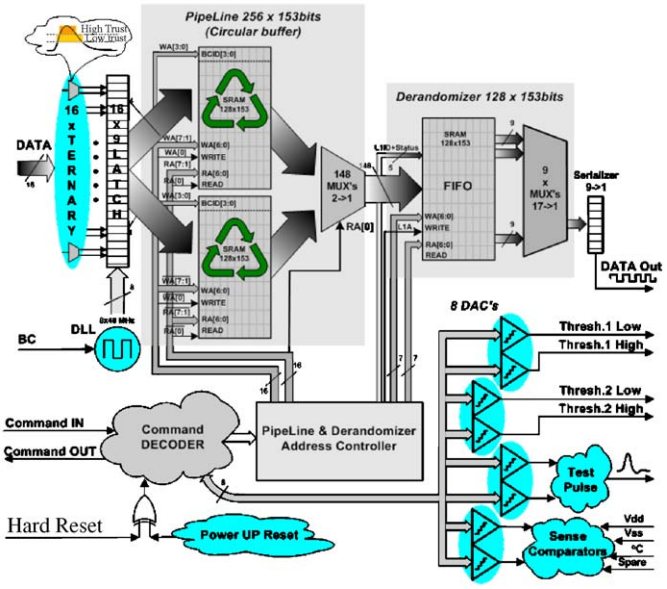

Fig. 2. DTMROC-S block diagram.

The DTMROC interfaces to two 8-channel ASDBLRs; time encodes their ternary outputs, stores the data in a pipeline and supplies Level 1 sparsified data to the read out driver (ROD) located off detector. It uses the ATLAS 40 MHz system clock (synchronous with the LHC beam crossings), supplied as an LVDS level signal and serves as a reference-time marker for the DELAY LOCKED LOOP (DLL) and as the system clock for the rest of the chip. The DLL divides the clock into eight equal offset phases (3.1 ns separated) to provide a time marker for the timing discriminators. Sixteen TERNARY RECEIVERS with low-impedance inputs interpret the current step outputs from the ASDBLR companion chips separating out the track and TR discriminator levels. Track discriminator level information is digitized in eight 3.1 ns time bins for each of three 25 ns beam crossings. This binning is sufficient to provide a 1 ns RMS time measurement as required for better than 150 μm track position resolution. A one bit indication of the state of the TR discriminator output is added to make a 9-bit word that is latched for each beam crossing and stored in the 144-bit wide programmable depth PIPELINE. The maximum depth of 256 locations allows more than 6 μs latency of the Level 1 trigger. On reception of a Level 1 trigger, data from three sequential 25 ns clock intervals are latched into the 42 event DERANDOMIZER. Data are serialized by the READOUT CONTROLLER and driven off chip by a LOW LEVEL DIFFERENTIAL DRIVER at the 40 MHz system clock rate to the off detector read out driver (ROD) board.

The COMMAND DECODER checks the bit stream for the presence of a Level 1 trigger command then looks for commands for various resets, test-pulse generation, and data to load into the DTMROC registers.

The DTMROC provides four 8-bit DACs for the remote programming of the two track and TR discriminator thresholds on the ASDBLR chips. Two shaped, test-pulse outputs are provided for calibrating the detector. The amplitude and delay of these test pulses are programmable. An on-board band gap voltage reference provides for the DAC reference currents. The power dissipation is 20 mW/channel when clocked at 40 MHz.[4]

3. The development of readout boards

The basic three ASIC readout units of two ASDBLRs and one DTMROC are common to both Endcap and Barrel Printed Circuit Boards (PCB).

3.1. TRT end cap wheel readout

The 278,000 straws in the end-cap wheels on either side of the barrel point radially outwards from the beam, and have the readout on the straw end at the largest distance from the beam [1]. There is sufficient room in the radial direction to allow use of separate analog and digital boards connected by miniature high-density connectors, see Fig. 3. In the final readout, triple sets of the 64-channel boards shown in the figure form a 192-channel board set that is read out by a single 16-pair control and data cable with five conductors carrying power.

3.2. TRT barrel readout

The 52,000 barrel straws are placed axially around the beam in three layers of 32 modules each. The quadralateral cross-section modules fit together to make three concentric rings inside a support structure with two triangular openings per module on either side [1]. The electronics is constrained to a 2 cm region sandwiched between the end-cap wheels and the end of the barrel. The barrel readout boards are sized to be in contact with and fit within the barrel support structure to complete the Faraday shield on the ends of the detector. The areal density of the readout is 30 mm^2/wire, about twice that of the end-cap wheel. This density was high enough to require the development of custom ball grid array (ASIC) packages to minimize the

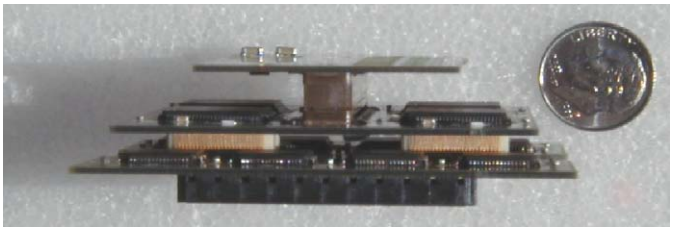

Fig. 3. The photograph above shows a 64-channel detector-mounted end-cap wheel readout board. The upper board is an unstuffed connector for power and data. The next lower board (center) houses four DTMROC ASICS and primarily handles digital I/O. The bottom board (4100 mm^2) has eight ASDBLR ASICS and connects directly to the end-cap wheel straw anode connectors. The final version of the readout has three interconnected pairs of DTMROC and ASDBLR boards with one data cable board.

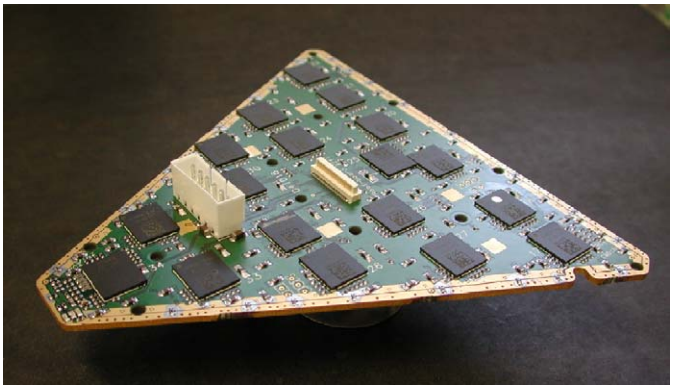

Fig. 4. One of the 12 TRT barrel board designs with digital ASICS in their custom ball grid array packages shown on top, and analog readout with similar packaging assembled on the bottom. The boards are sized to fit into and make contact with the barrel support structure to enclose the straws in a Faraday shield.

footprint of the packaging allowing the readout to fit within the allotted space.

After several prototypes, we converged on a single PCB design that houses both analog and digital ASICS. A production board is shown in Fig. 4. The 14-layer PCB board employs four kinds of "blind" vias to limit the number of layers that are interconnected and allow internal shielding of sensitive signals. An outer ring of edge plating is used to connect analog ground to spring contacts on the inside of the barrel support structure. In the final assembly, a liquid cooling plate is attached to the digital side of the board and the total height of the assembly including cooling plate and connectors is less than 1.5 cm [7].

4. Conclusion

The objectives of the detector-mounted TRT straw readout have been accomplished by an international team from Sweden, CERN and the US. This team has developed two complex ASICS that provide the complete readout chain, special ASIC packaging and unique approaches to the printed circuit board design separately tailored for the two TRT straw layouts. A sign of the degree of success of this effort is clock-syncronous pick up and other noise of the assembled readout on detector is typically less than 30% of the desired operational threshold of ~12,000 electrons equivalent input signal.

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