

The ASDBLR and DTMROC Detector Mounted Readout for the ATLAS TRT

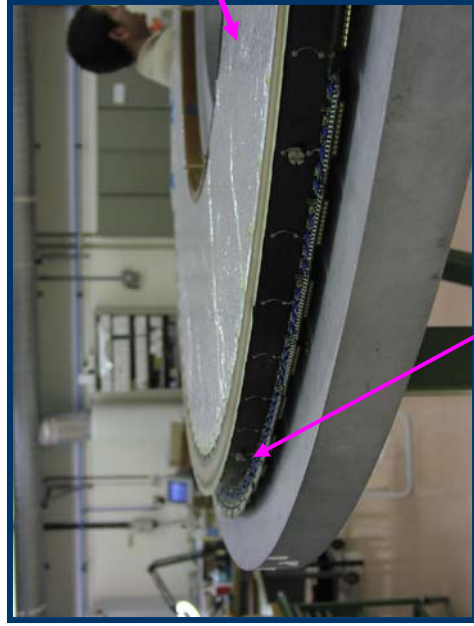
Mitch Newcomer for the ATLAS TRT Electronics Group

July 2, 2003

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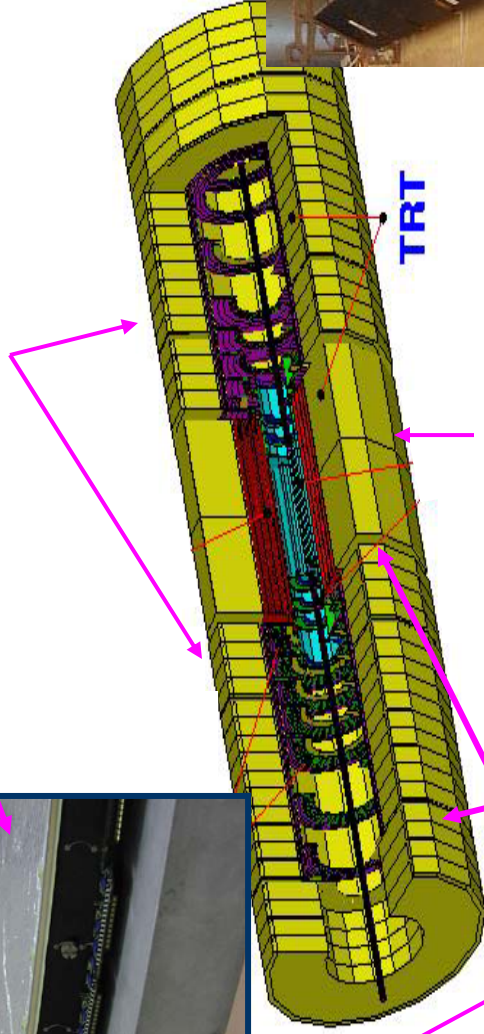
TRT

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TRT Wheels

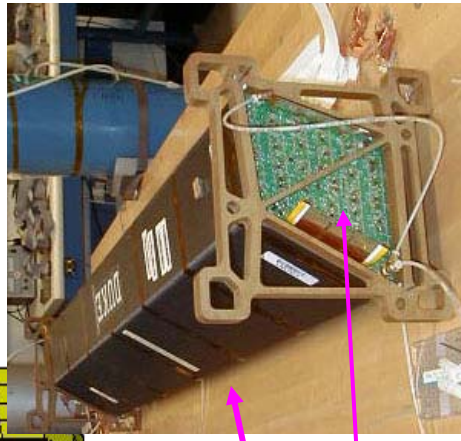
Radially Aligned Straws (320K channels)



Barrel Modules

Axially aligned 100K channels

TRT Front End
Electronics



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Detector Mounted Readout Objectives

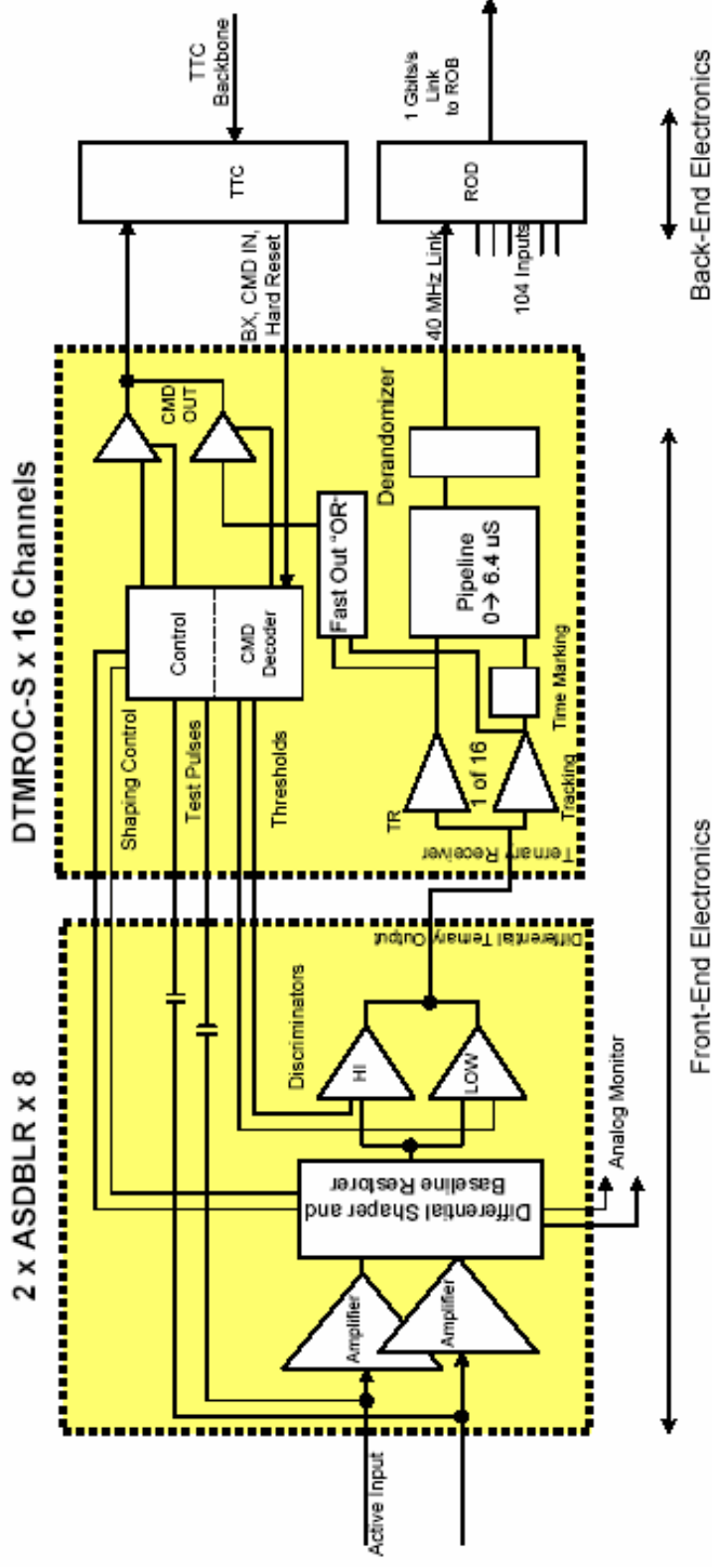
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- Low Noise/Low threshold operation → ~2000e ENC
 < 300KHz spontaneous straw tube trigger rate
- 1ns time resolution → ~130 μ m position resolution
- High Rate operation → 20MHz with stable threshold
 (100:1 Signal variation)
- Radiation Tolerance → 3.5X10¹⁴ n/cm 5MRad
- Reliable operation of high bandwidth Analog and Digital
 readout ASICs without interference
- ATLAS R_{ead} O_{ut} D_{river} Compatibility

Readout Electronics basic block

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16 channel custom ASIC triplet



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ASDBLR References

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Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL Technology

N. Dressnandt, N. Lam, F.M. Newcomer, R. Van Berg and H.H. Williams
IEEE (2000) Trans. On Nucl. Sci. V48 n4 p1239

An Amplifier-Shaper-Discriminator with Baseline Restoration for the ATLAS Transition Radiation Tracker

B. Bevensee, F.M. Newcomer, R. P. Van Berg and H.H. Williams
IEEE (1996) Trans. on Nuc. Sci. V 43 p1725

<http://www.hep.upenn.edu/atlas>

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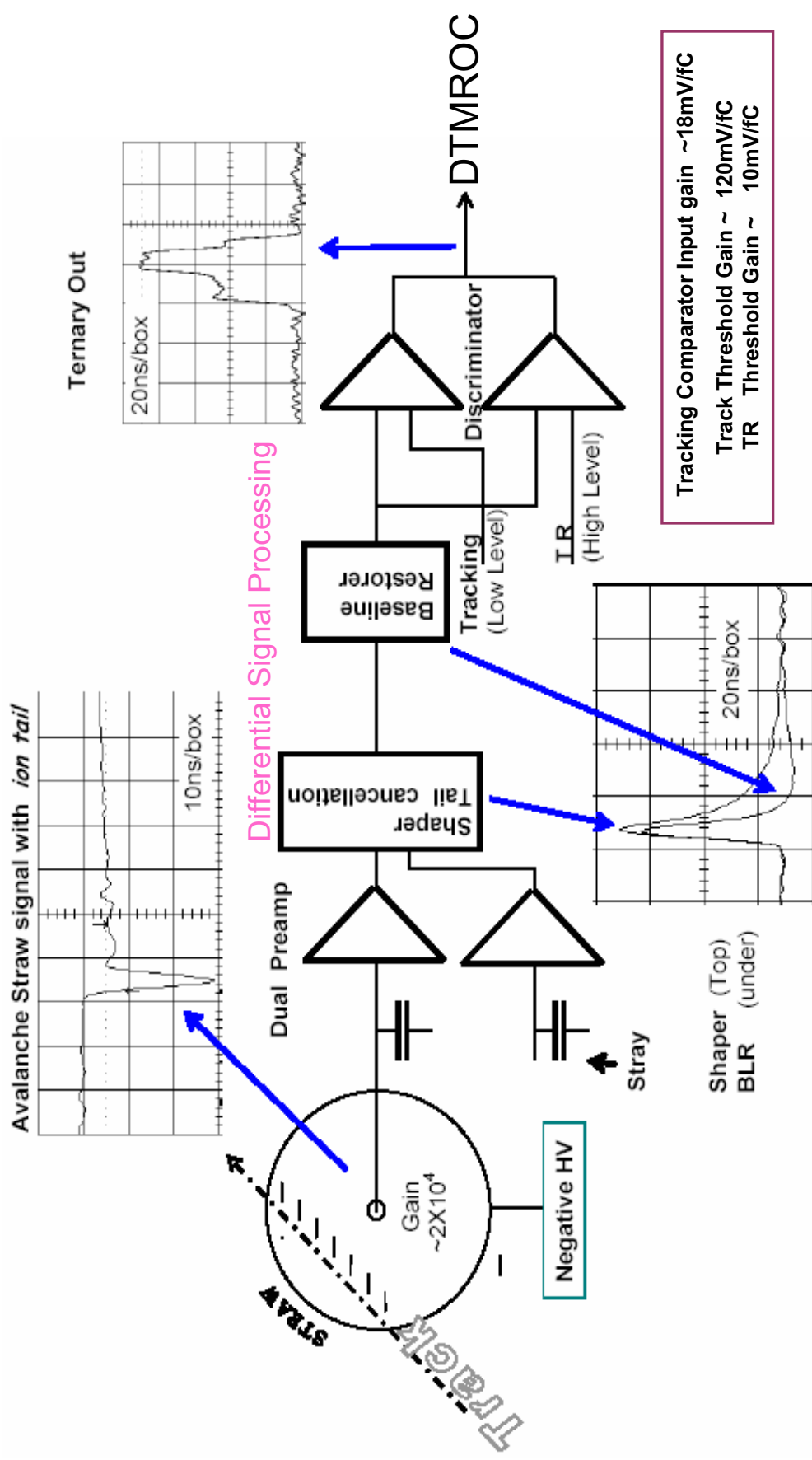
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ASDBLR

8 Ch Analog Front End

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ASDBLR Basic Design Spec

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- Power ~ 40mW/ch.
- Preamp Input protection ~ 2.8mJ.
- Analog Gain ~ 18mV/fC at Comparator input.
- Double Pulse Resolution ~ 25 - 50ns dependent on 1st pulse amplitude.
- Spontaneous Trigger Rate at 2fC threshold ~ 300KHz.
- High Threshold Maximum Range → 140fC.
- Ternary (comparator) output levels (nominal Design):

Signal	Tern Pos	Tern Neg
Quiescent	-400uA	0uA
Track only	-200uA	-200uA
Track & TR	0uA	-400uA

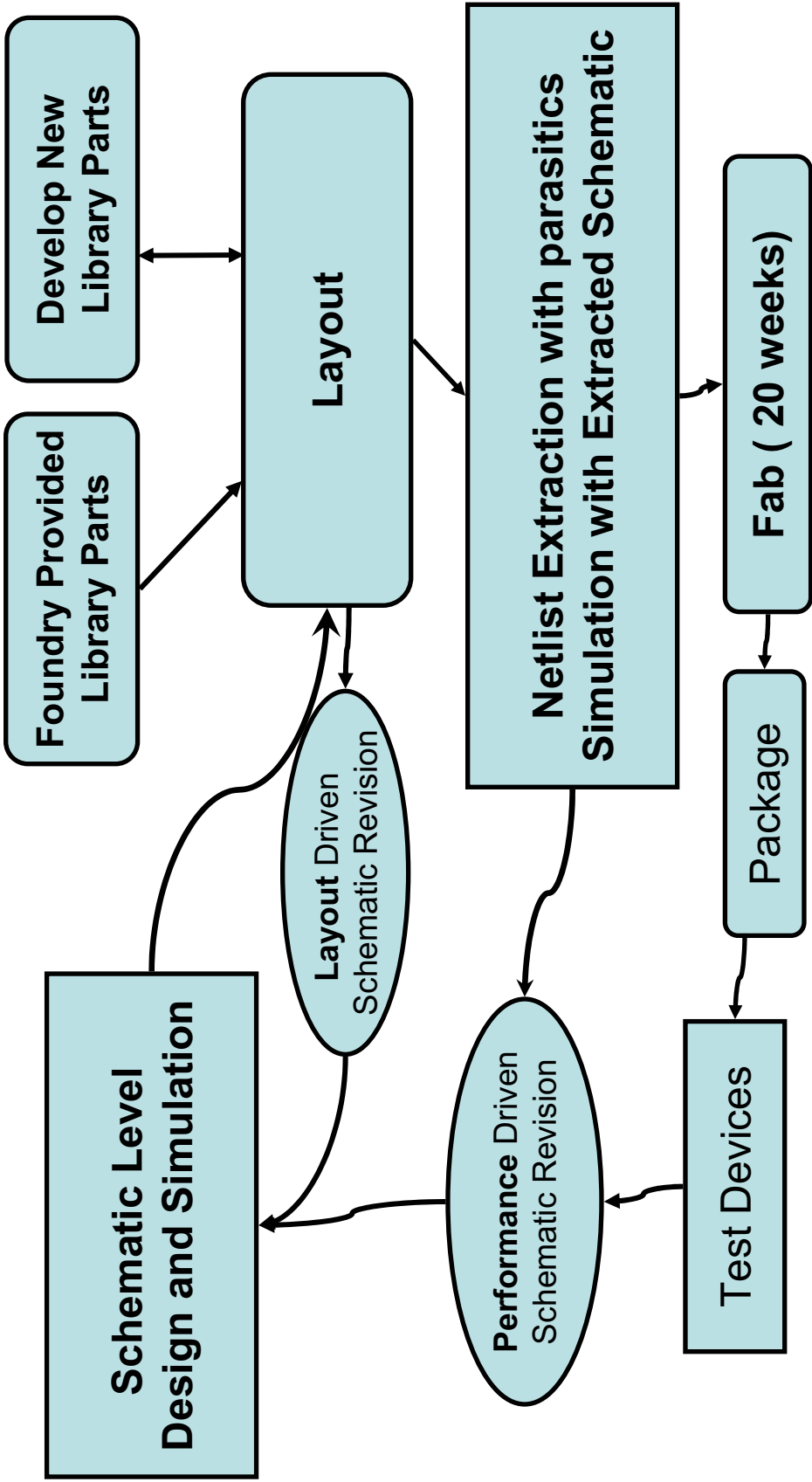
ASDBLR Implementation

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- Process - Rad Tolerant 0.8um BiCMOS Technology (DMILL)
- Designed at the discrete device level using SPICE for Simulation
- Channel Complexity 160 Bipolar Transistors / 10 CMOS Switches
160 Resistors / 105 Capacitors
- Channel based Layout ~
 - Avoided metal runs over transistors/resistors.
 - Double vias where possible.
 - Separated Analog and Comparator/Ternary Driver Power
 - Dedicated power bus distribution at the channel level.
 - Substrate Contact and Power buss isolation between ch.
 - Preamp Supply filter on each channel.
- Eight (nearly) identical Channels on 340um Pitch

ASDBLR design Cycle

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ASDBLR02 Final Design

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Final Design Improvements

- Reduce area of input protection network → Reduce Capacitance 11pf → 5pF.
- Increase Input transistor current to 7.5uA/m reduce beta loss.
- Increase analog gain by 50% to reduce sensitivity to device matching in comparator. (56mV/fC at BLR output)

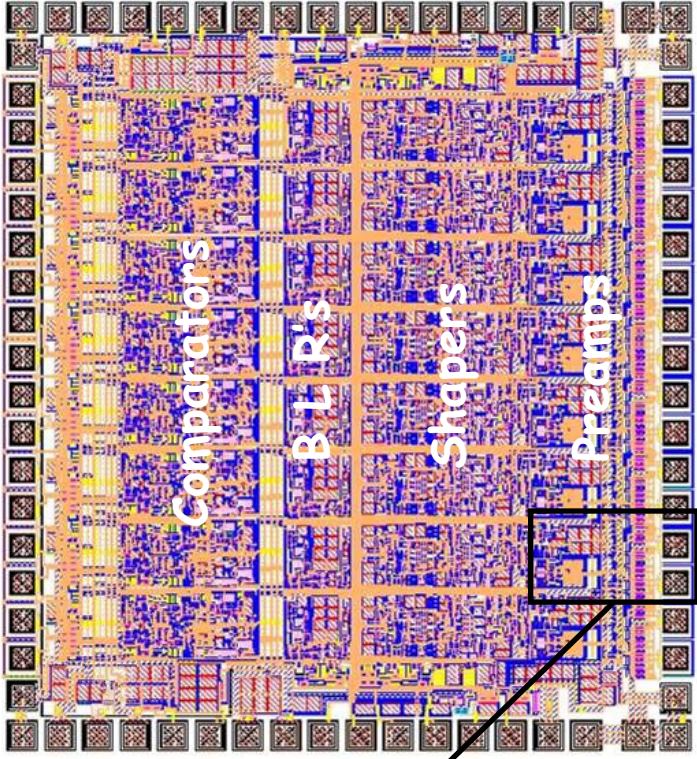
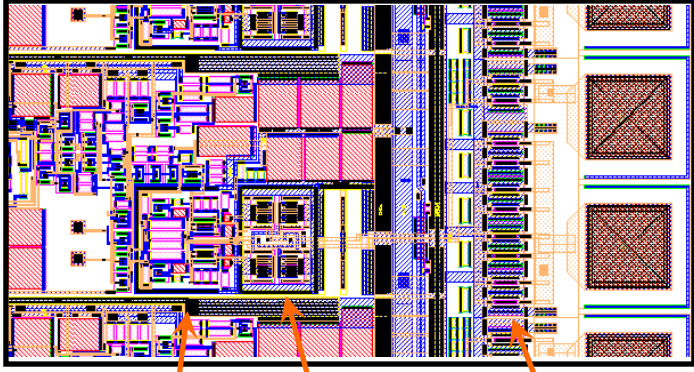
Measured Results

- Input referred threshold matching good, $RMS < .25fC$
- Noise ~ 2100e ENC on board with ~5pF capacitance (100e/pf).
- Power ~ 40mW/channel.
- High Rate operation ~ demonstrated to 20MHz (pulser tests)

Production ASDBLR

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3.3 X 3.6mm



Dual Preamps
intermingled
layout

Input
Transistors in
cross Quad
Configuration

Input protection NPN
Transistors
Expanded Geometry
Emitter Stripes 4 x 30 um

Comparators

B.L.R's

Shapers

Preamps

ASDBLR Radiation Testing

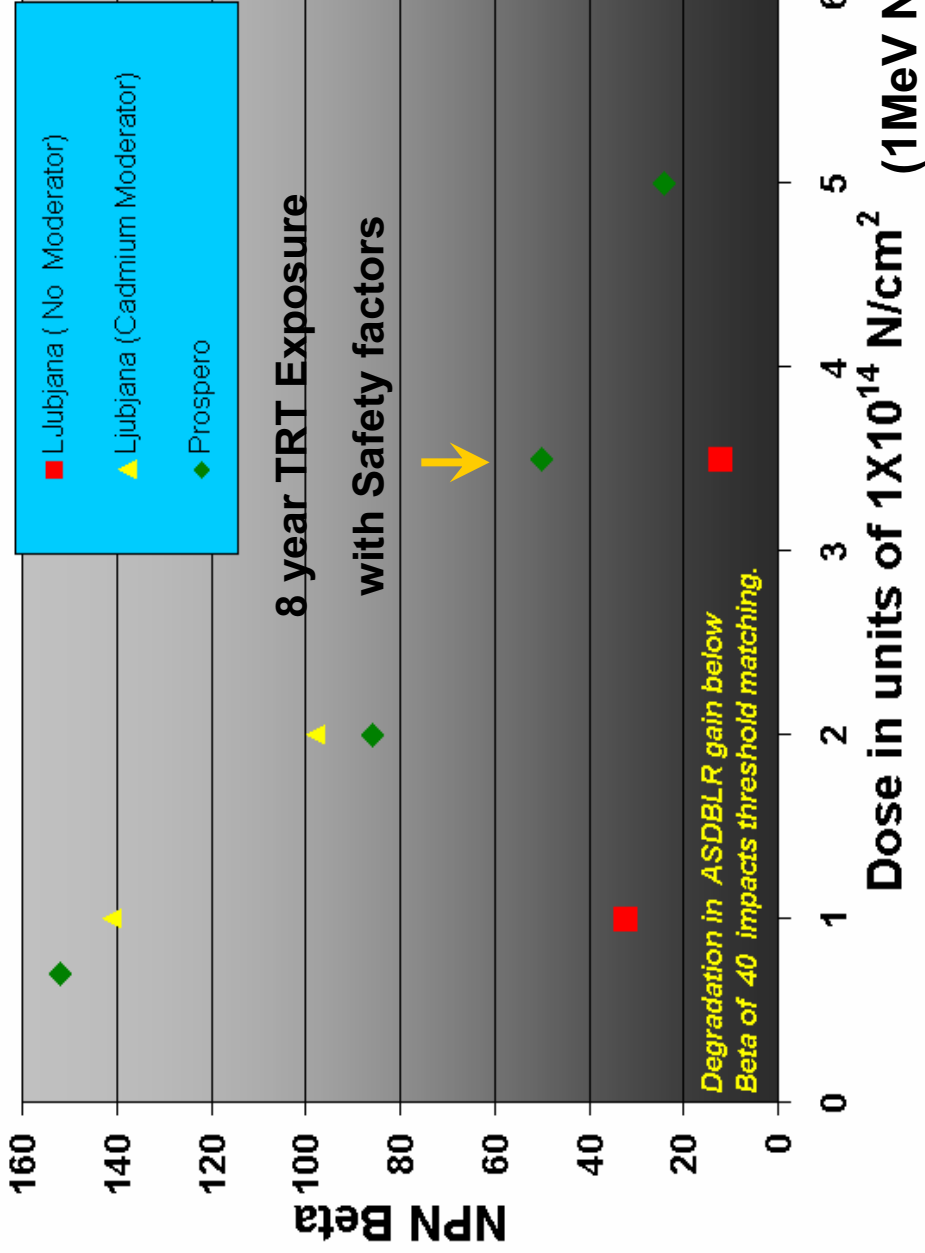
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- **Gamma Testing up to 7MRad with no significant performance degradation.**
- **1MeV NEIL Neutron Testing to 5×10^{14} (10 year with safety factor) shows a significant reduction in beta resulting in lower gain and increasing the channel to channel threshold offset. At Beta = 30 the gain is lowered by ~ 50%.**
- **DMILL NPN Beta is sensitive to Thermal Neutrons**
More study needed. Moderator re-evaluation?

Neutrons

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DMILL NPN Neutron Sensitivity



Thermal Neutrons present at the Ljubjana facility point out a possible weakness using the DMILL Process.

Careful comparison of these results with the expected exposure in the ATLAS ID need to be performed.

All devices annealed at 150° C for 48 hrs.

ASDBLR Radiation Testing ATLAS TRT report NSS 2002 FEE2003

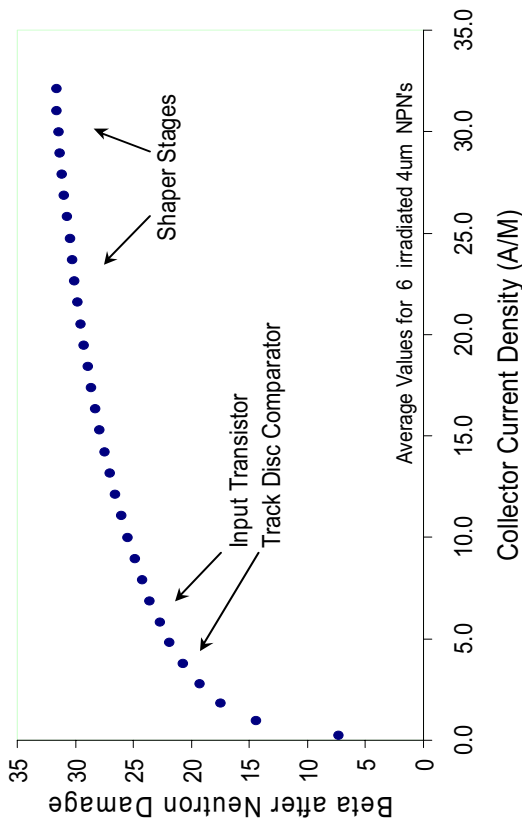
Summary of Device tests to 11 / 2002

ASDBLR	# chips	Power on	Date	Type Dose ¹	Change in Resistance	Post Rad NPN Beta
99	3		4/00	5X10 ¹³ n	NA	84
	3		4/00	1X10 ¹⁴ n	NA	52
00	6	x	5/01	5Mrad γ	5%	180
	9		10/01	3.5 X10 ¹⁴ n	1.5%	55 ³
01	6	x	6/02	1.5X10 ¹⁴ p	5%	70
01	16	x	7/02	7MRad γ	8%	130
01	10		5/02	3.5X10 ¹⁴ n	10.4%	11 ^{2,3}

¹ n and p dose is in units of particles/cm².

² Thermal neutron dose high $\sim 10^{14}$ n/cm².

³ After annealing 23hrs@150C



The measured current gain of DMILL NPN transistors after exposure to 3.5X10¹⁴n/cm² and prior to annealing. The arrows show the operating points chosen for various parts of the ASDBLR channel design. After annealing the beta increased by a factor of two.

From: Radiation Hardness: Design Approach and Measurements of the ASDBLR ASIC for the ATLAS TRT

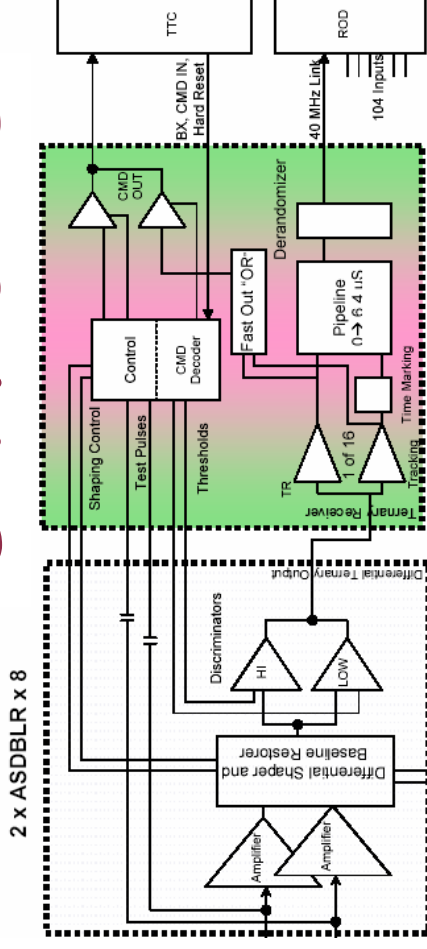
Nandor Dressnandt, Mitch Newcomer, member IEEE, Ole Rohne and Steven Passmore

See NSS 2002 Conference Record

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DTMROC-S



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N.Dressnandt, P.T.Keener, F.M.Newcomer, R.Van Berg,

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DTMROC References

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Implementation of the DTMROC-S ASIC for the ATLAS TRT Detector in a 0.25 μ m CMOS technology

***V.Ryjov, F.Anghinolfi, Ph.Farthouat, P.Lichard, R.Szczygieł, N.Dressnandt, P.T.Keener,
F.M.Newcomer, R.Van Berg, H.H.Williams, T.Akesson, P.Eerola***

NSS 2002 Conference Record

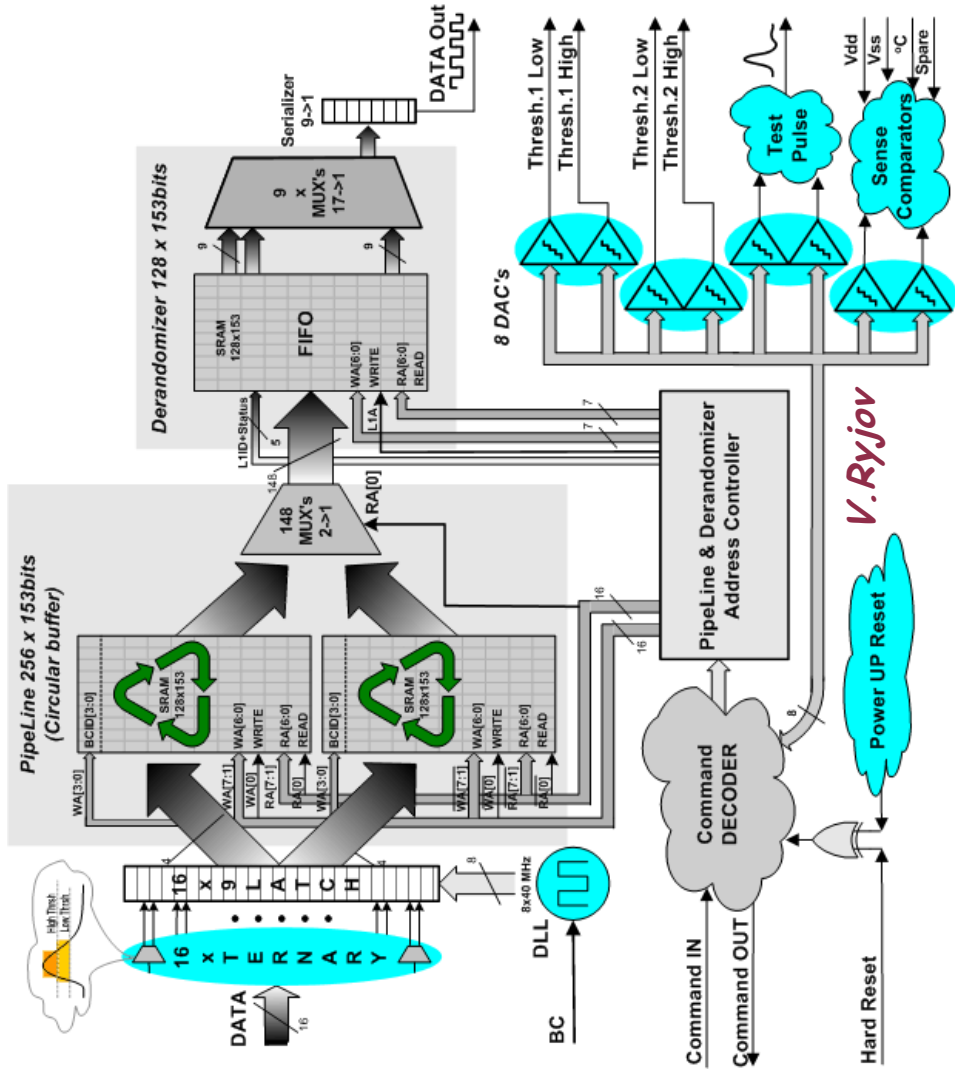
Progress in the Development of the DTMROC Time Measurement Chip for the ATLAS Transition Radiation Tracker (TRT)

***C. Alexander, F. Anghinolfi, N. Dressnandt,
T. Ekenberg, Ph. Farthouat, P. T. Keener, N. Lam, D. La Marra,
J. Mann, F. M. Newcomer, V. Ryjov, M. Soderberg, R. Szczygieł,
V. Tikhomiro, R. Van Berg, H.H. Williams***

IEEE (2000) Trans. On Nucl. Sci. V48 n3 p514

<http://hep.upenn.edu/atlas>

functional Blocks



V. Ryjov

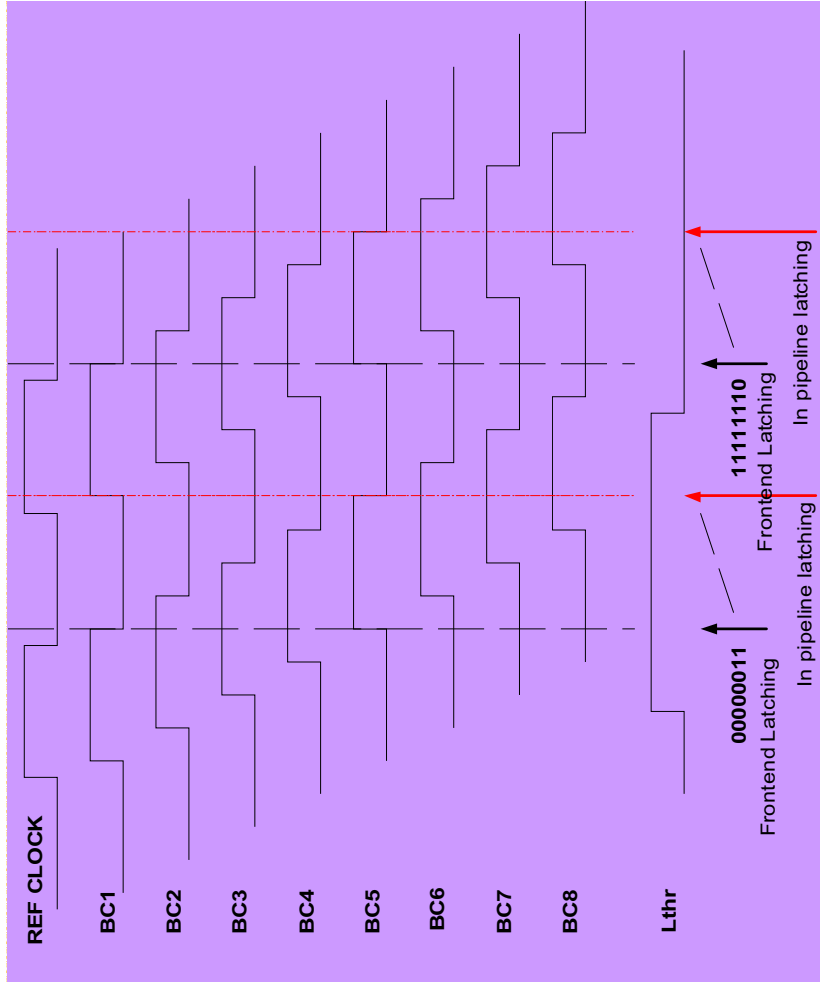
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Time Marking

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32 elements delay chain, phase detector, charge pump

- 40MHz Clock \rightarrow 3ns time bins
- 8 equally spaced clock outputs used to sample straw track pulses
- 50% duty cycle clock regenerated to run the chip core logic

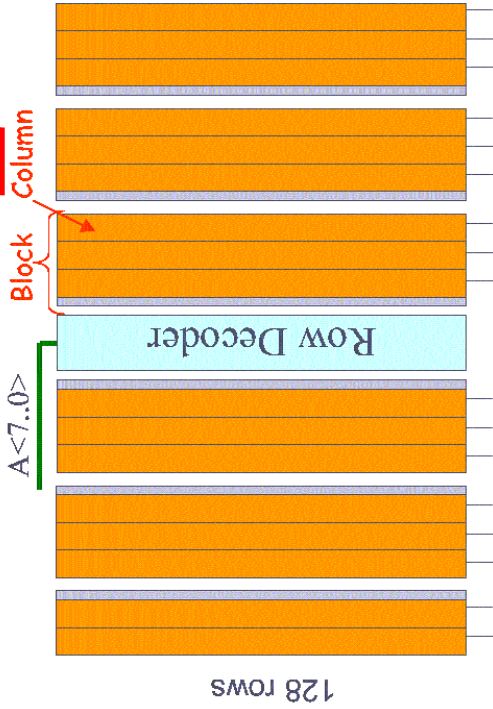
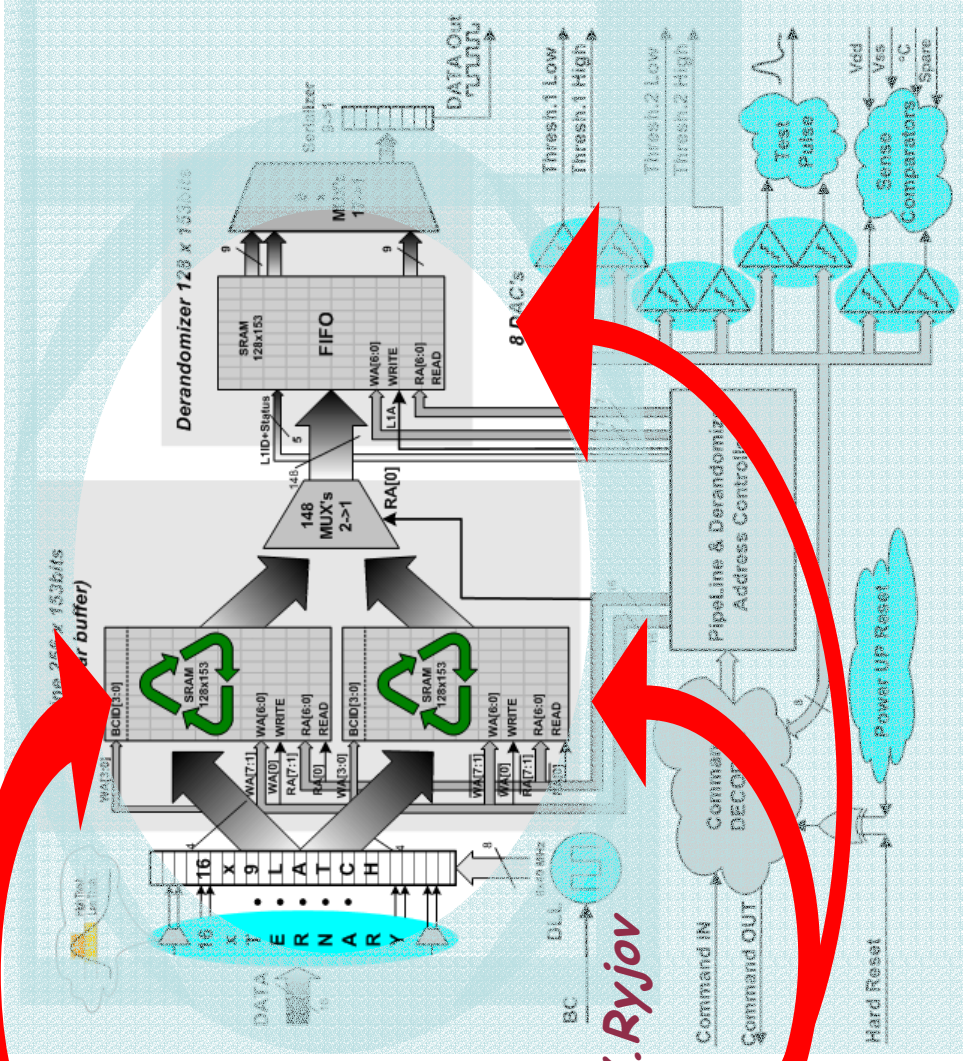


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Memory / Pipeline

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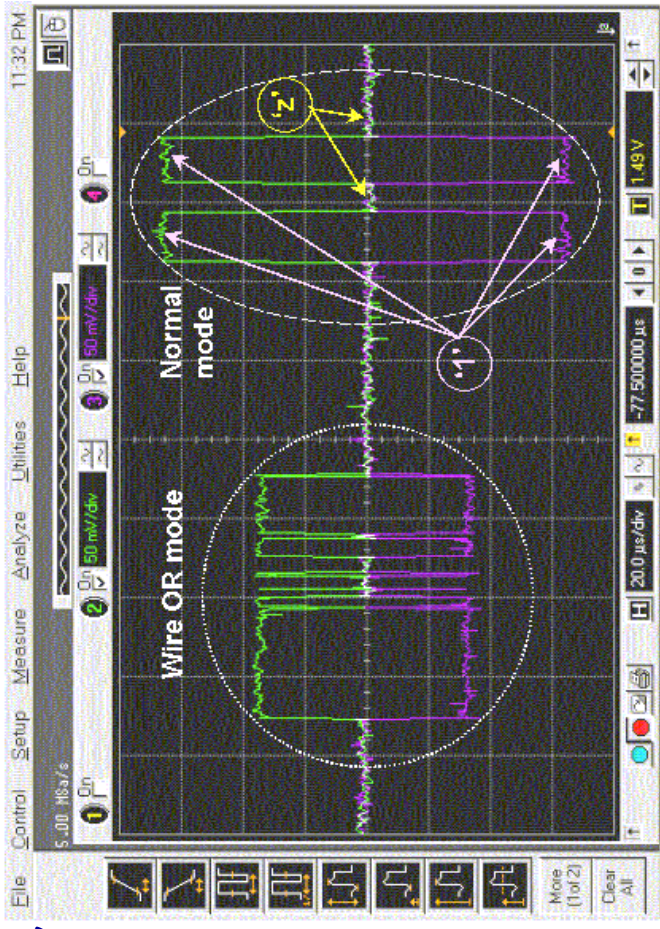
V. Ryjov

Dual-port 128x153-bit SRAM (2.39kB)

DTMROC-S I/O

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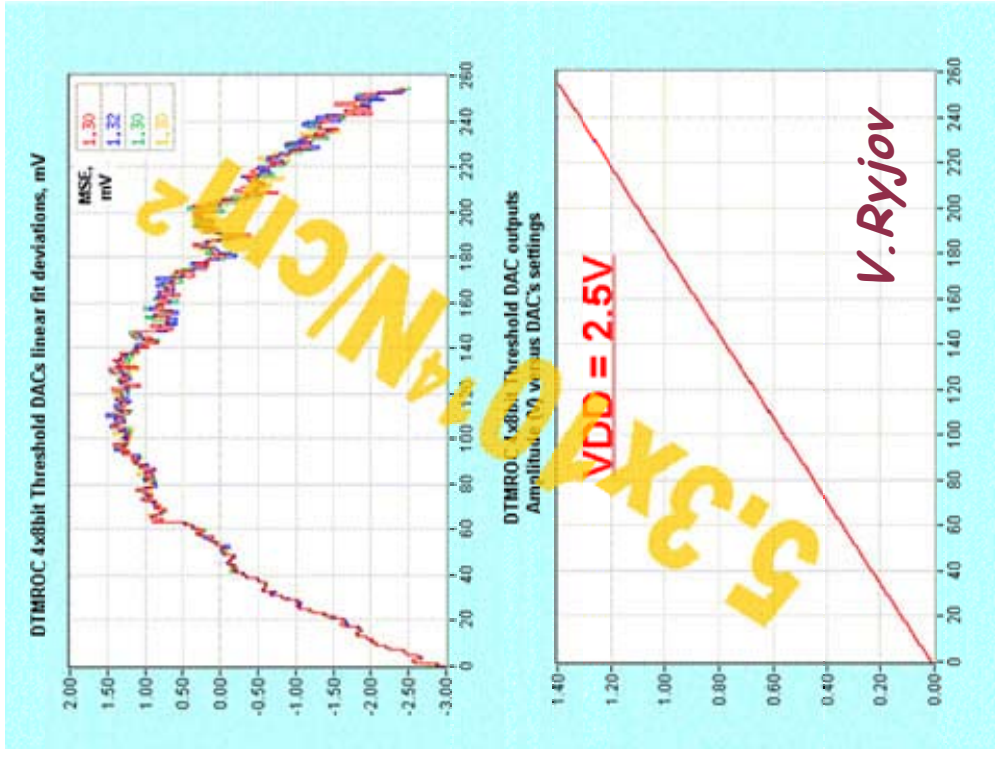
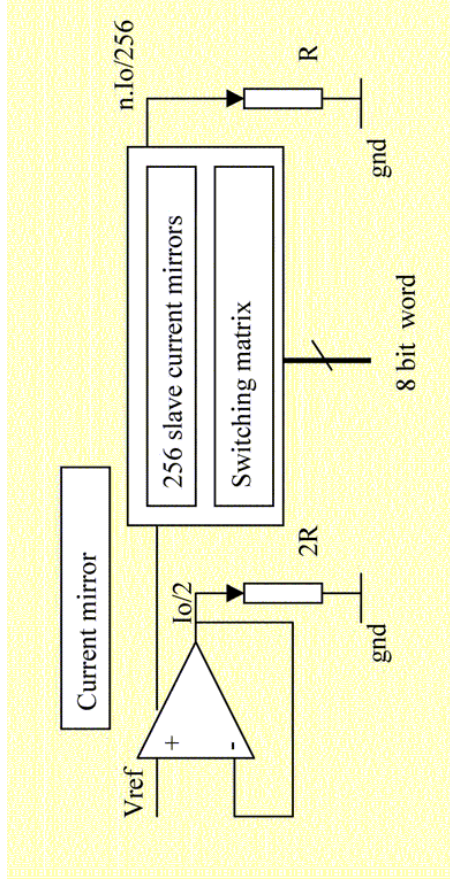
- Full/Reduced read-out : 444/380 bits per event, including Header
- LVDS-compatible, tristate drivers -> 40 Mbits/s copper links
- "Wire-OR" - for self triggering fast-out option - selected ternary inputs contribute to the chip-level trigger
Up to 15 DTMROCs can be "OR'ed on a common buss



DTMROC-S DAC's

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- Internal bandgap reference 1.26V
- Current mirror master - 128 PMOS unit devices ($L=8\mu\text{m}$, $W=5\mu\text{m}$)
- 256 identical PMOS slave current mirrors per DAC



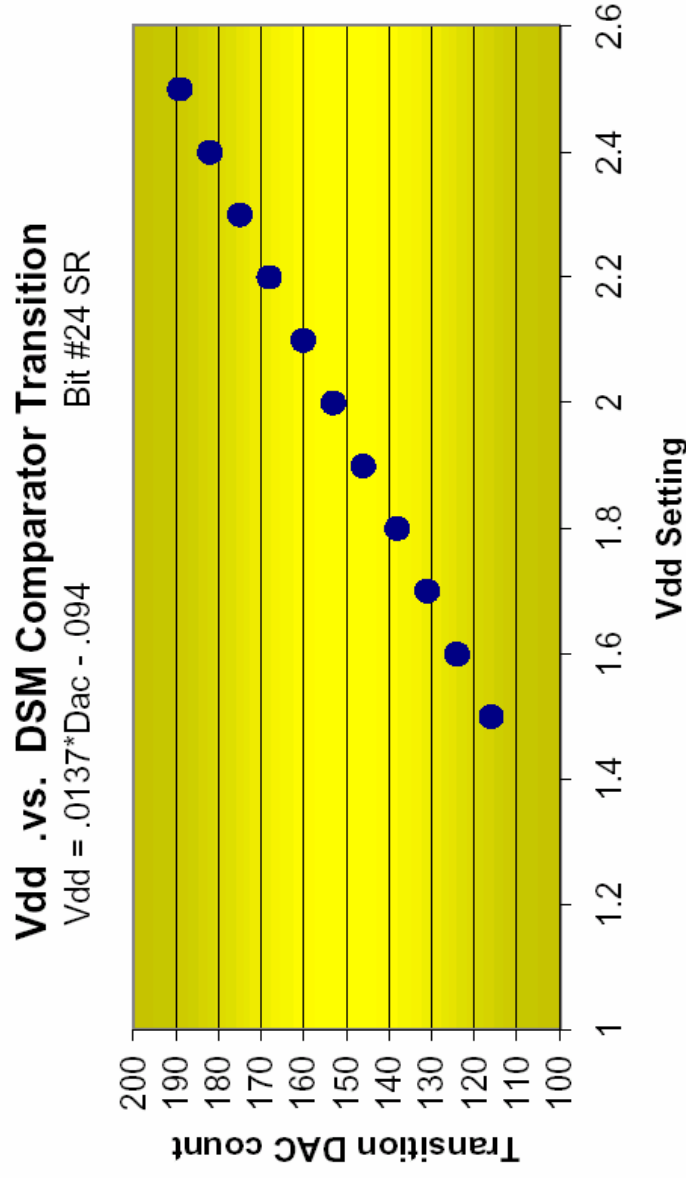
DTMROC-S

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Analog Sensing

- *Two DACs*
- *Four Comparators*
 - *Temperature*
 - *VDD*
 - *Ext Voltage 1*
 - *Ext Voltage 2*



Vdd Sense remained at 191 from 26 - 55 C

DTMROC-S

testability

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- *General-purpose 32-bits Status Register*
- *Logical OR of all DTMROC error indicators in the Data Header field*
- *Parity check logic for all internal registers*
- *Lock status, a "watch dog" and a "dynamic" check circuitries examine the DLL*
- *JTAG Boundary-Scan*
- *Special scan mode - configures all DTMROC flip-flops as a large shift register controlled via JTAG interface*
- *Memory Build-In-Self-Test (BIST) controlled via the Configuration register and JTAG interface*

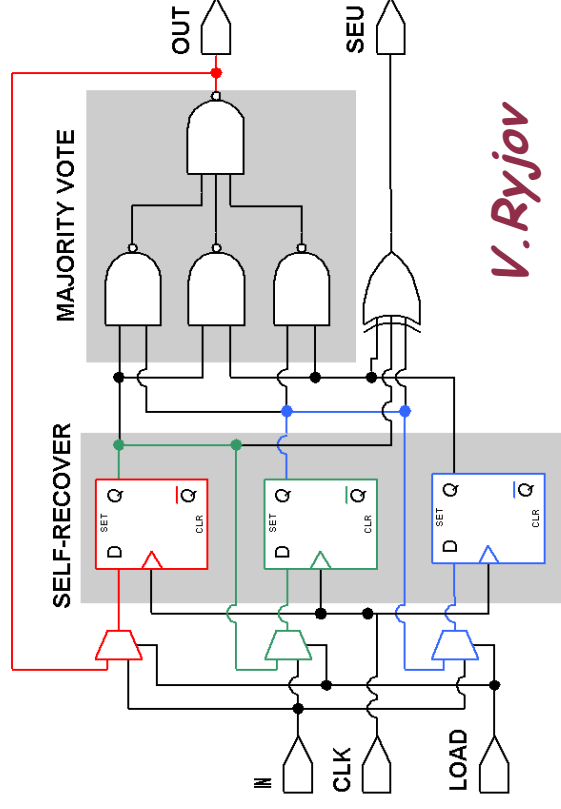
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SEU Protection

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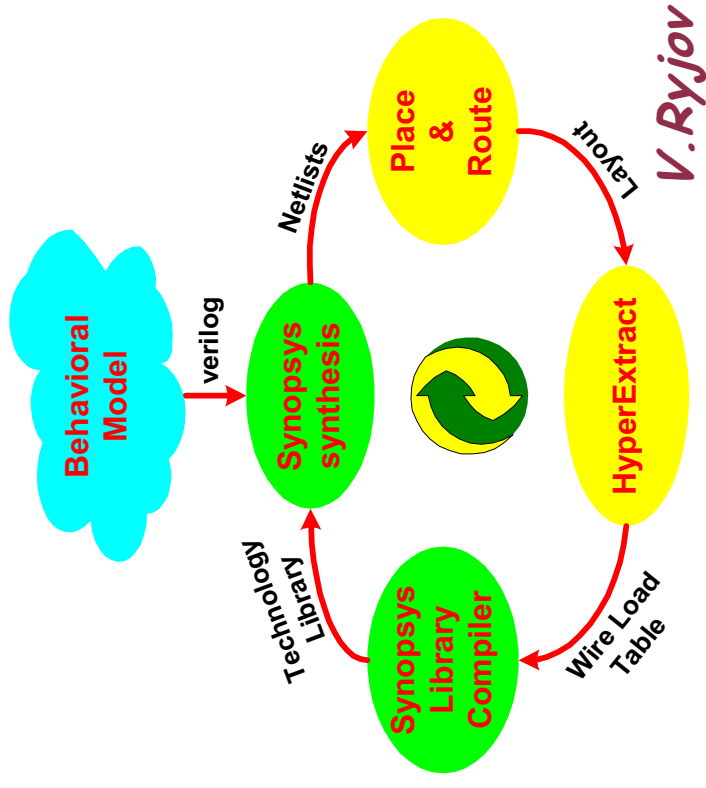
- *Internal registers are equipped with parity error check*
- *The most critical parts are built of the SEU resistant and self-recovering elements based on triple logic with majority vote.*
- *Statistics circuit monitors the number of detected SEU's*



DTMROC-S Design Tools (CERN based)

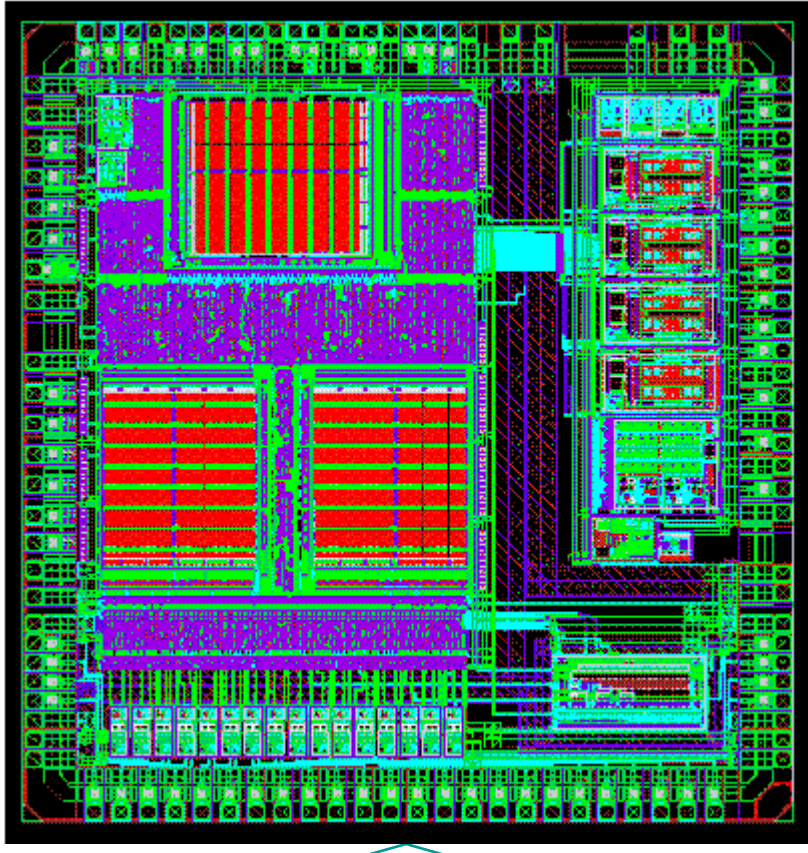
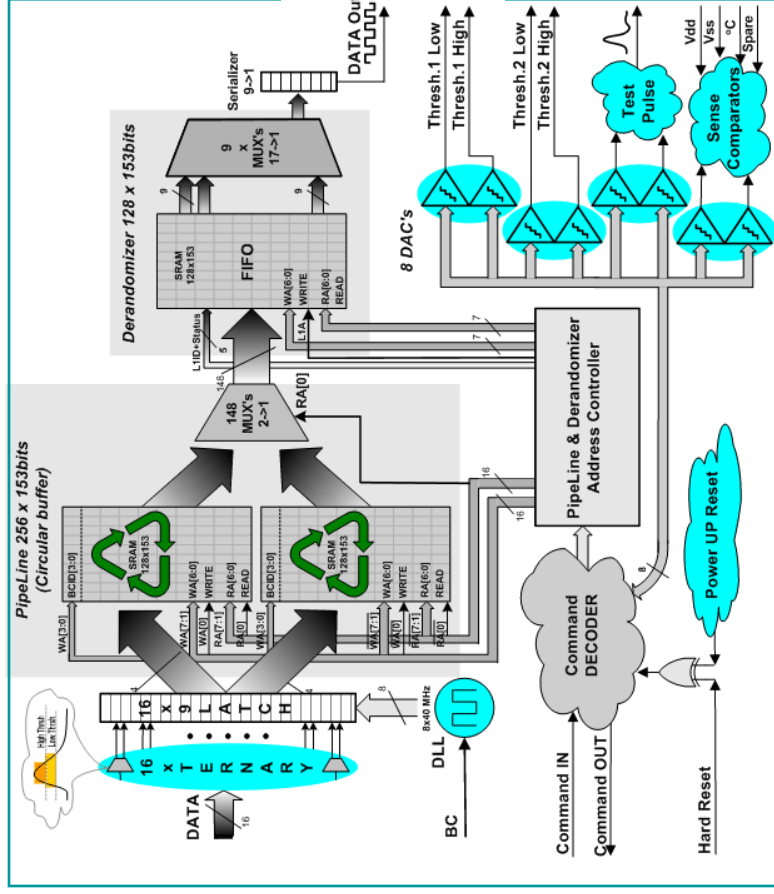
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- Verilog modelling
- Synopsys synthesis tools
- Silicon Ensemble Place&Route tools
- Completely scripted physical design flow
- Number of synthesis-layout cycles to predict post-route timing during RTL synthesis
- NC Verilog Simulator – Interleaved Native Compiled Code Architecture



DTMROC-S Layout

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~500k Transistors

Die size 5.2x5.0 mm²

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DTMROC-S

Fab

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- Submitted/fabricated (.25um process) in Jan 2002
 - Wafer size 8" (350 μ m) \rightarrow 1017 useable dies per wafer
- 850 chips tested on the mixed signal IMS Tester at CERN
- 5 process corner (85/92/100/115/125%) evaluated
- 87% Yield for 850 chips
- Irradiation tolerance test at CEA Saclay Pagure facility in July 2002
- SEU sensitivity evaluated at the CERN PS in July 2002
- Test Beam at the CERN H8 in August-September 2002

DTMROC-S

Radiation Testing

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Total Ionizing Dose tolerance

- Tested at CEA Saclay Pagure facility in July 2002
- 7 Mrad total dose / 1.33 MeV gamma radiation
- ~10% increase in the DAC's output voltage after irradiation, no DNL change
- No variations in the power consumption and the chip performance

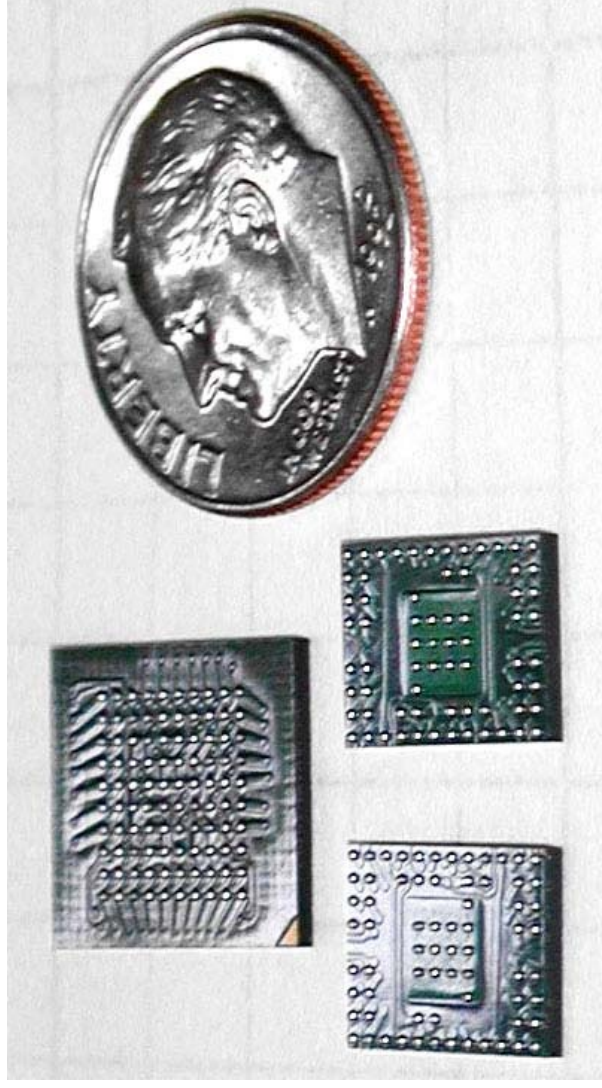
SEU sensitivity

- Evaluated at the CERN PS irradiation facility in July 2002
- Integrated fluence of 1.8×10^{14} p/cm² on 24GeV beam
- SEU cross-section for a single D flip-flop in different internal registers varies from 0.8×10^{-14} to 1.2×10^{-14} cm²
- Impact of SEU's in the vital components is suppressed by self-recovering logic

ASDBLR & DTMROC Packaging Labeling

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Fine Pitch Ball Grid Arrays



Laser Marked packages
2D Bar code
Human Readable
numbering



ASIC Testing

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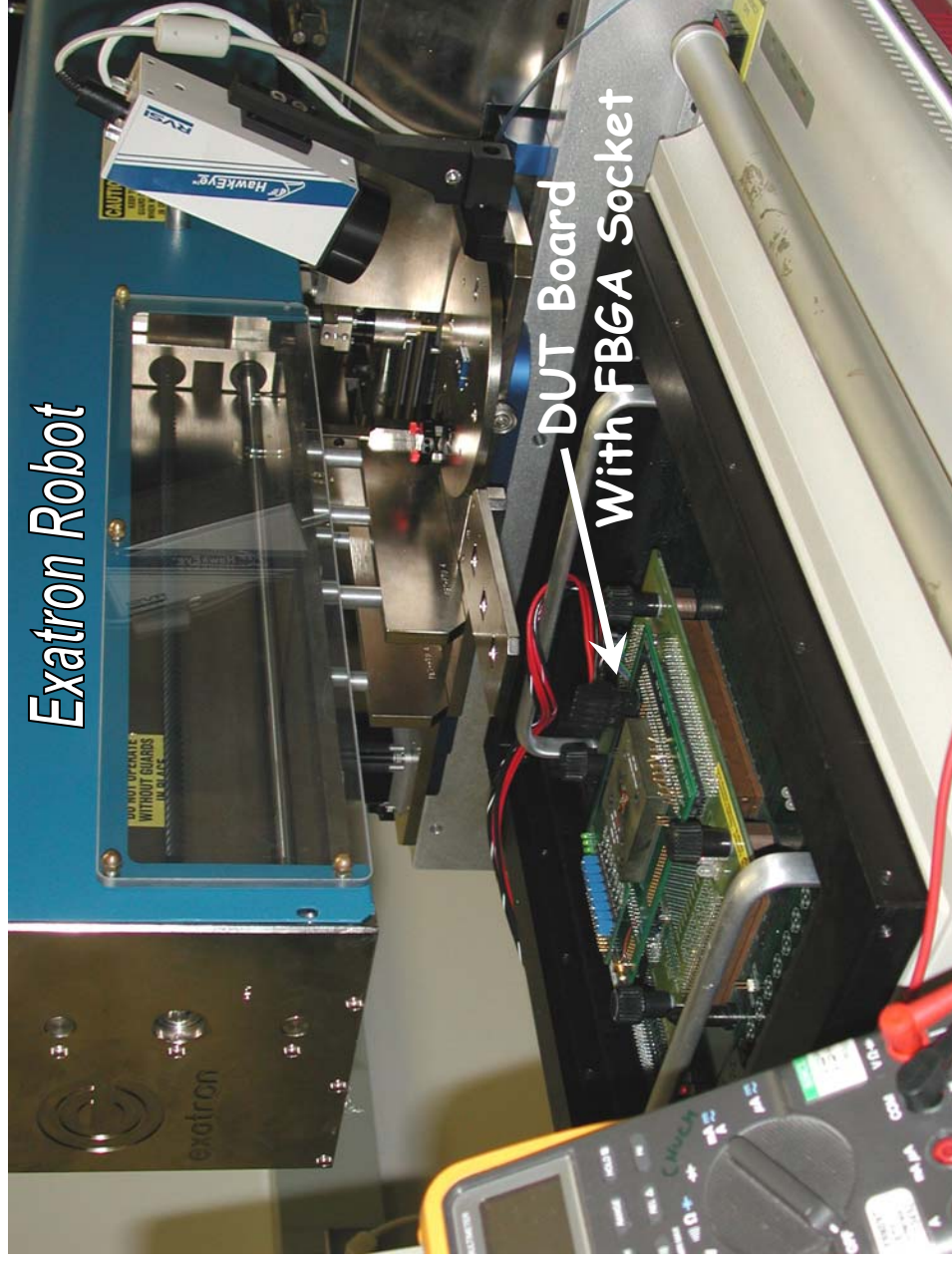
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ASDBLR

DUT Board on IMS

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IMS Tests on ASDBLR

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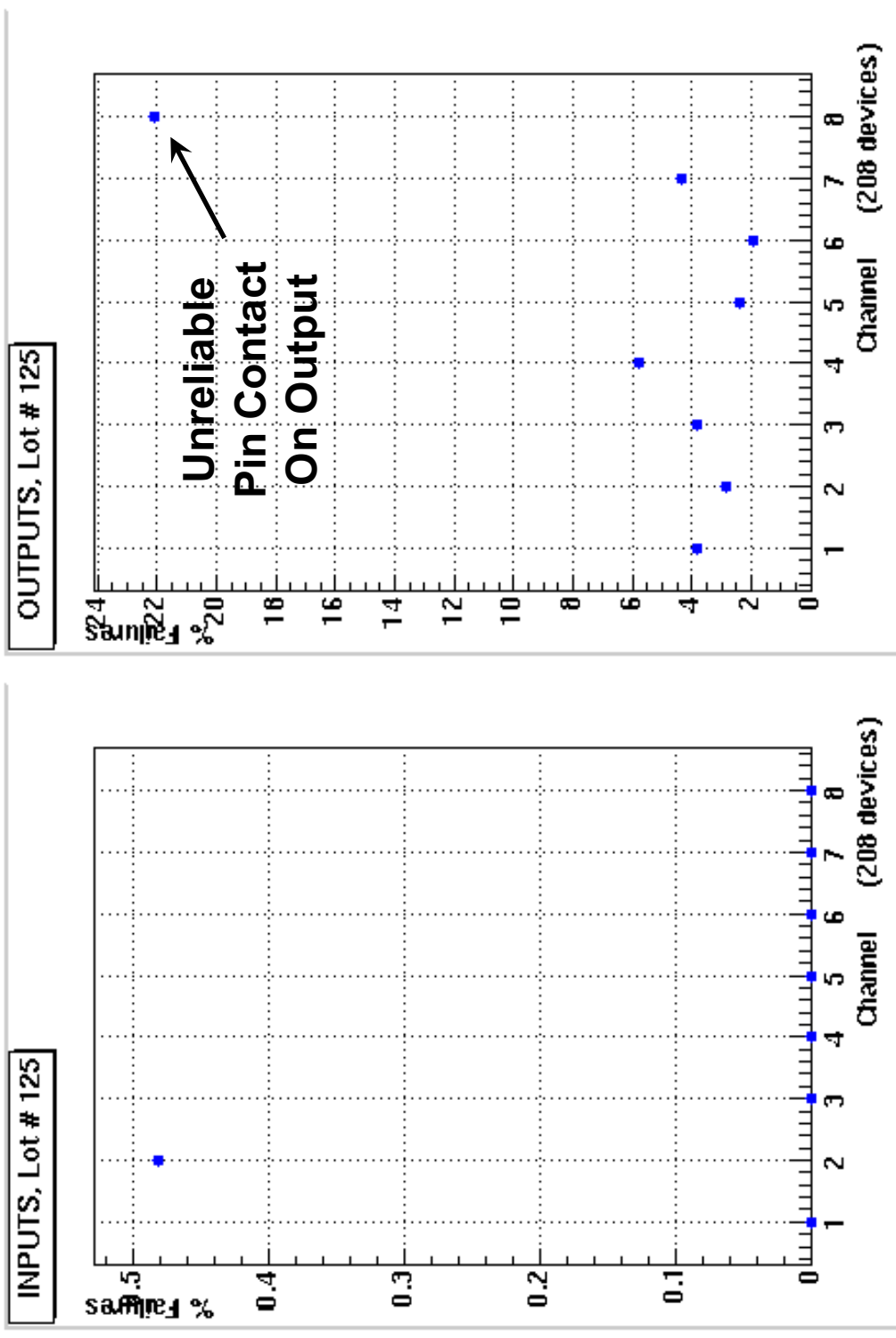
Read Bar code and record test (event) Number

- **Supply Current**
- **Input voltage/resistance**
- **Output current / switching**
- **Low Threshold response to 0, 2, 3 fC input**
- **High Threshold response to 30 fC.**

Write Results to SQL data base

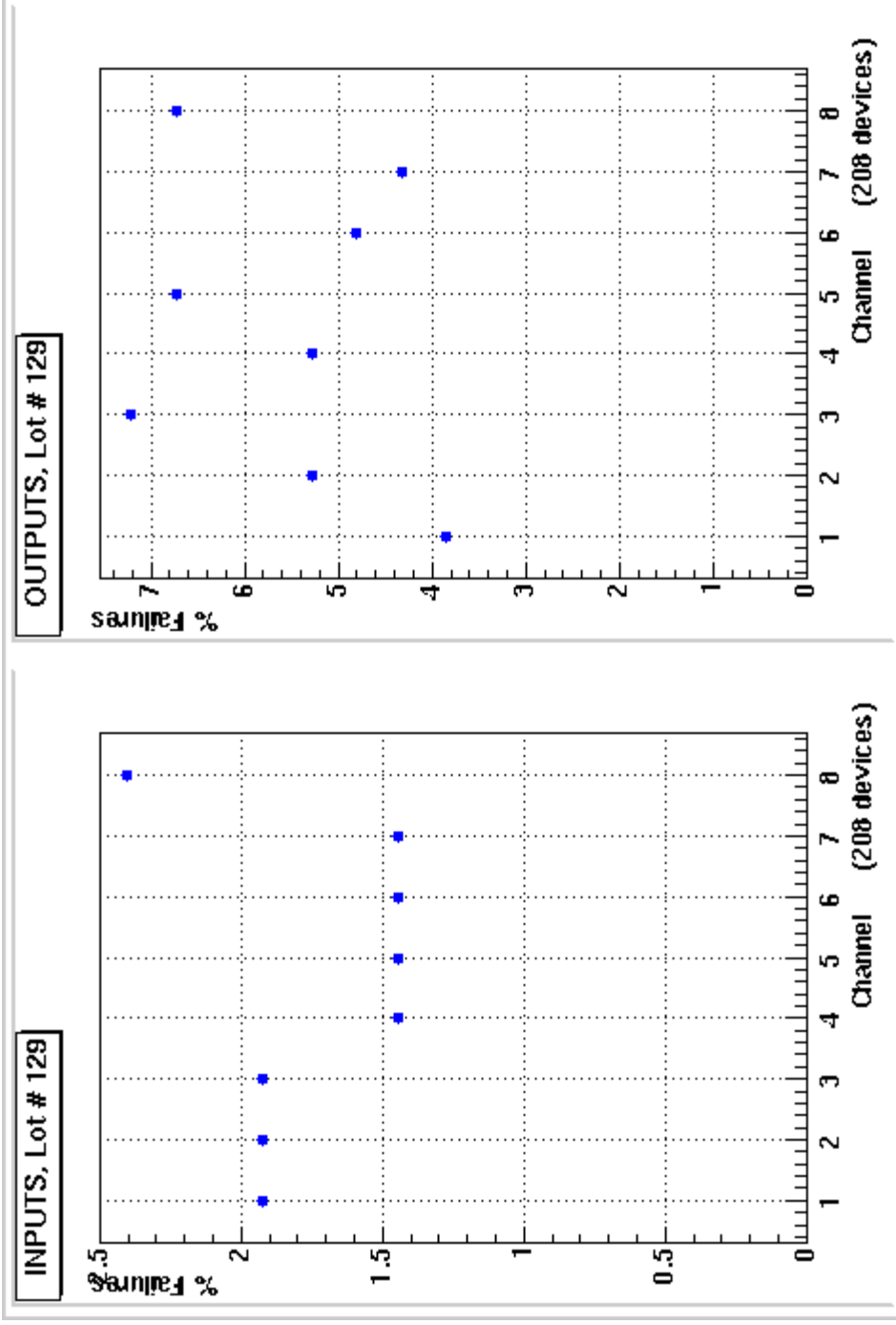
Failures Due to Socket Pin Reliability

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Using Forced Air to clean pogo pins

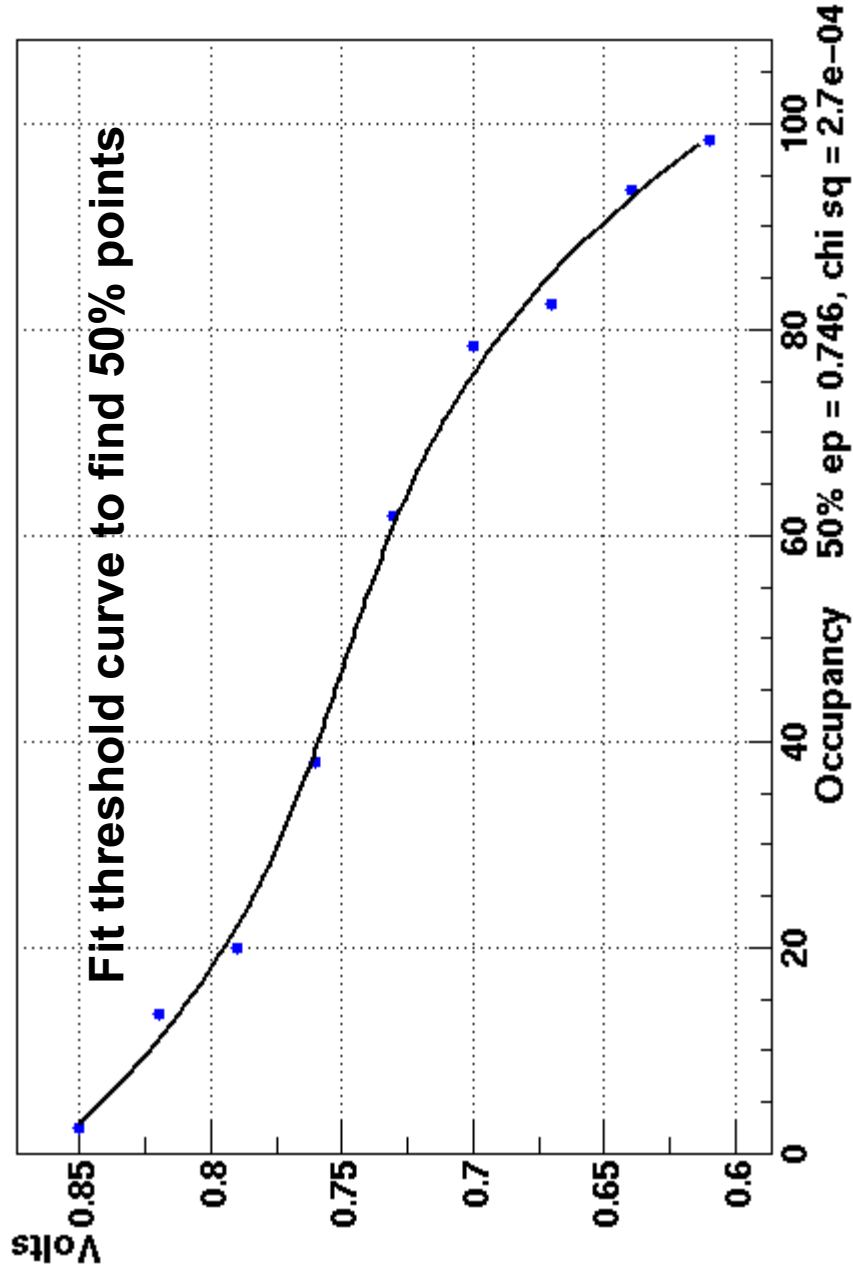
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Finding ASDBLR 50% Threshold

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Q1 TestNum 8633, Ch5, 30mv Sp



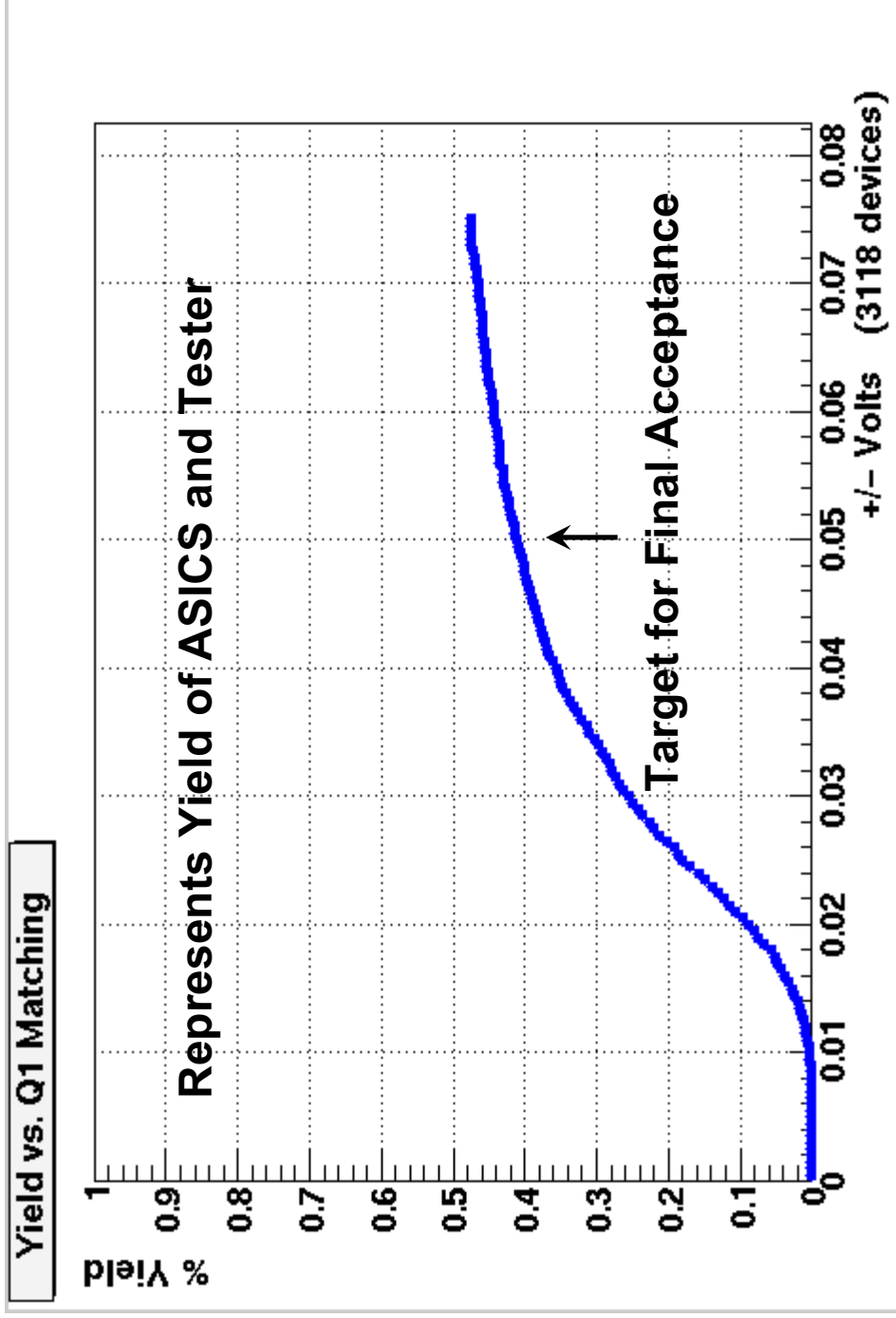
IMS Beta Stage Testing Experience

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- First 3000 chips demonstrate minor problems.
- Socket Pins must be cleared with forced air daily.
- Some wandering of the Threshold 50% points day to day.
- Bar code too close to chip label, leads to ~5% read errors.

False failure rate ~10% presently
Should improve over time.

Yield on First 3000 Devices **ATLAS TRT** with Beta Testing version **FEE2003**

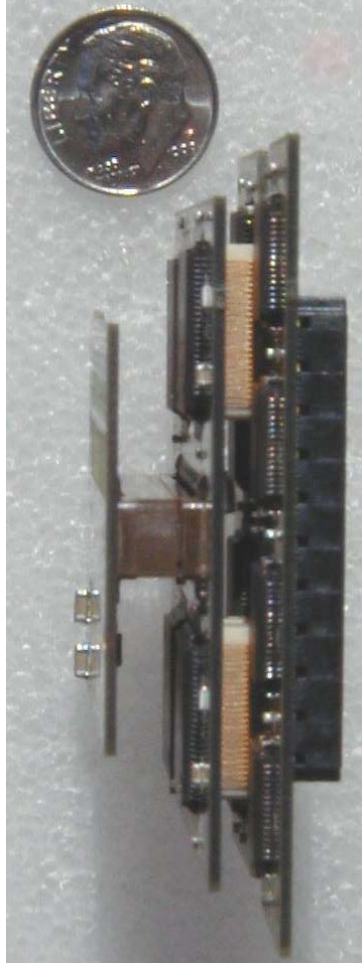


End Cap Wheel Boards

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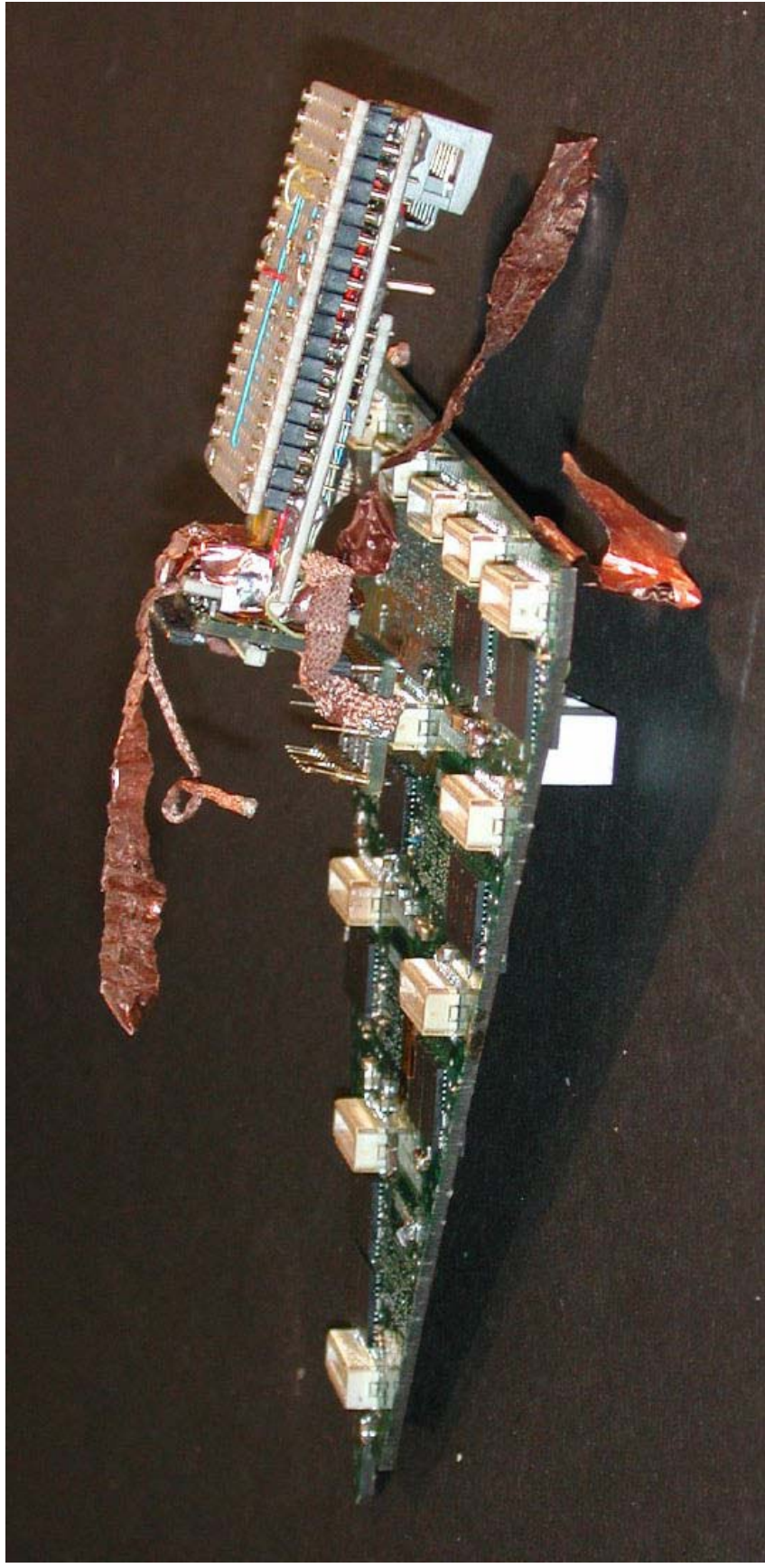
- 192 channels per assembly
- 2 DTM Board's = 1 virtual module.
 - 1/32 of endcap type A wheel
- Flexible interconnect between 64 channel DTMROC boards allows 192 channel board to follow curvature of wheel tread.
- Initial noise measurements on prototype detector show operation at 2fC possible.

Side view of the stackup of one 64 channel ASD board, one (old) 64 channel DTM board, and a connector board



192 channel DTMROC board

**Barrel Module Board with ATLAS TRT
15 ASDBLR / DTMROC FEE2003
triplets**



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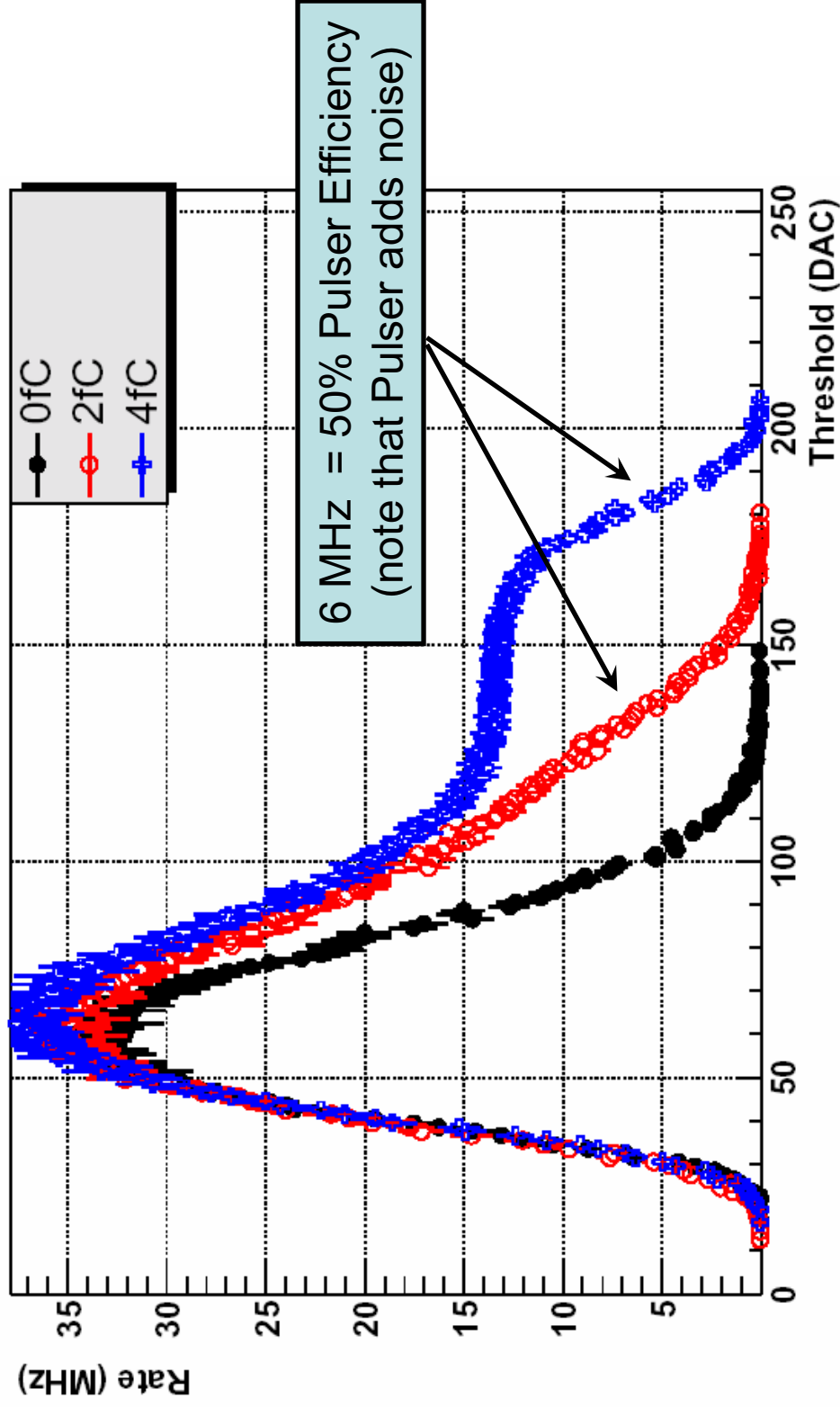
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Noise Rate Plot with Barrel ModuleBoard and Pulsar

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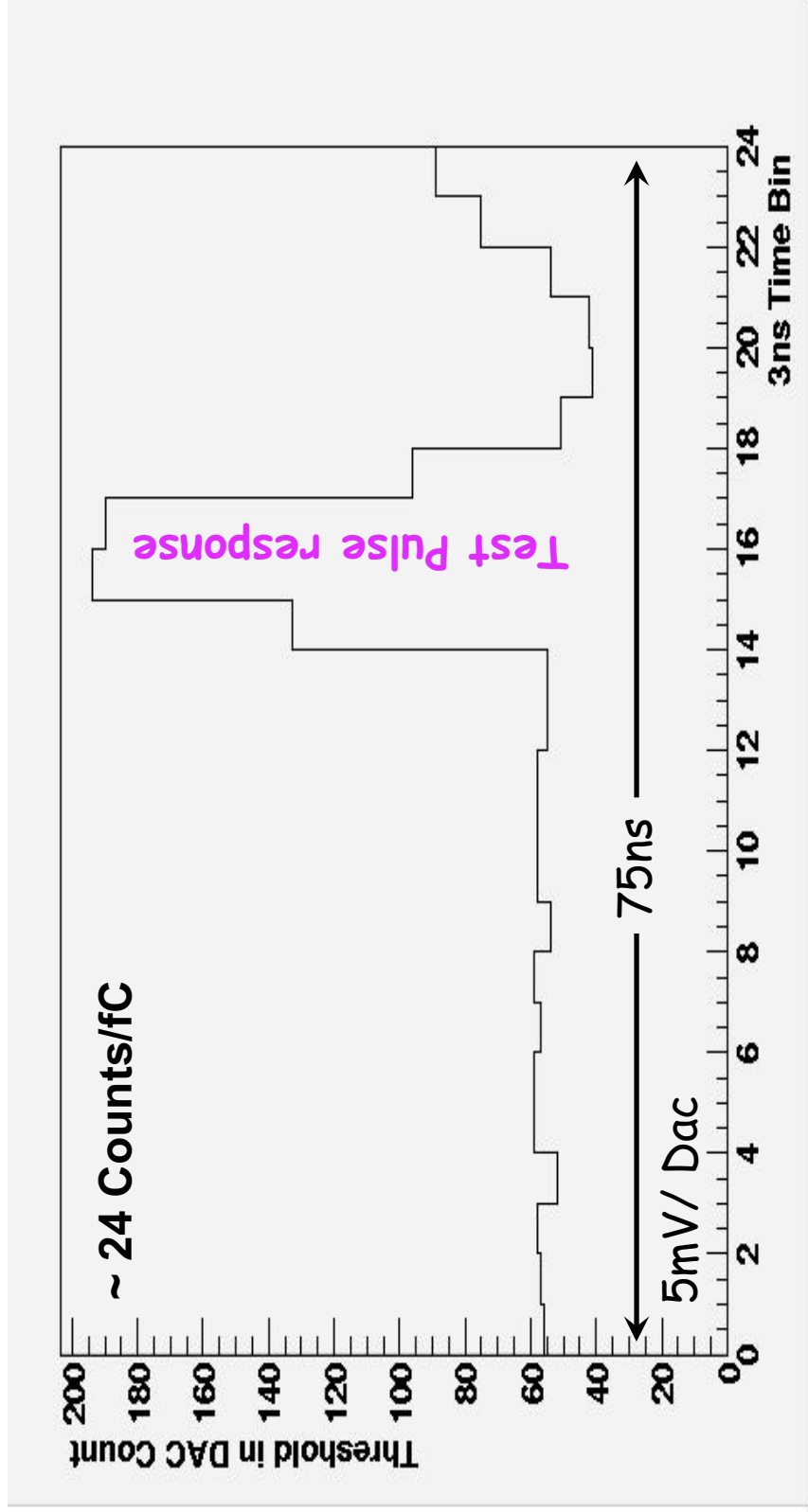
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Analog and Digital Readout on the Barrel Module Board (good Channel)

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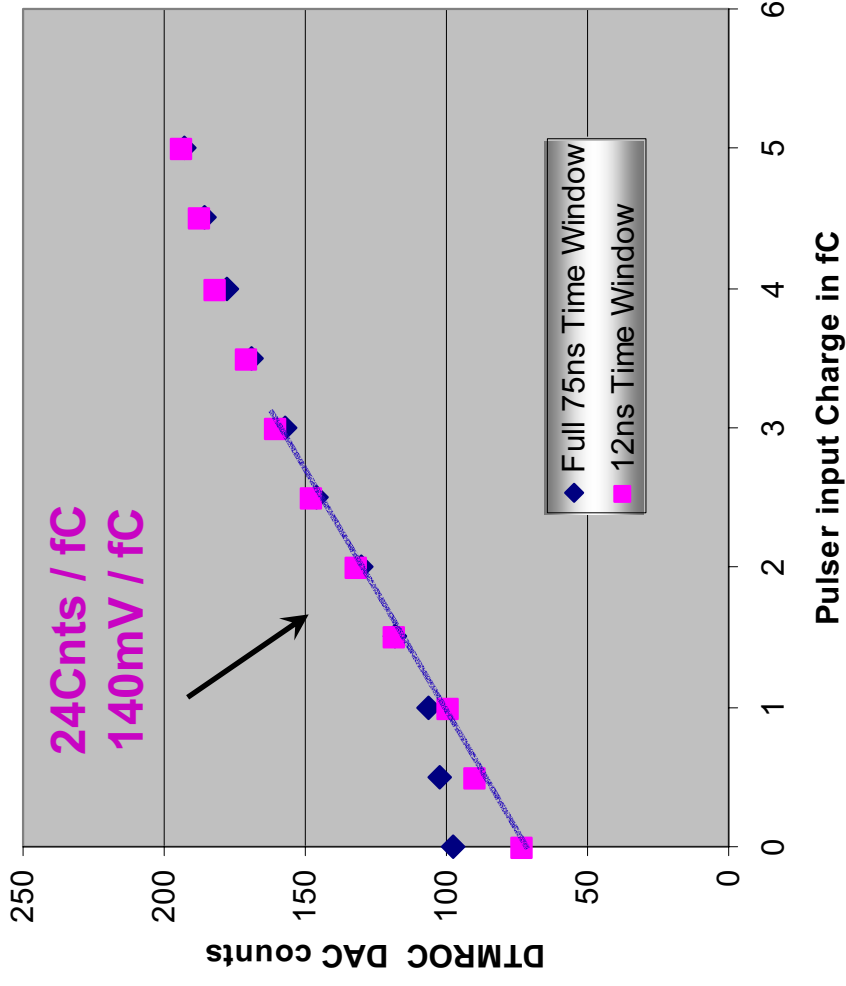
50% Efficiency Dac Setting by Time Bin



Beating Down Pulser Noise using DTMROC Timing window

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50% Threshold VS Input Charge

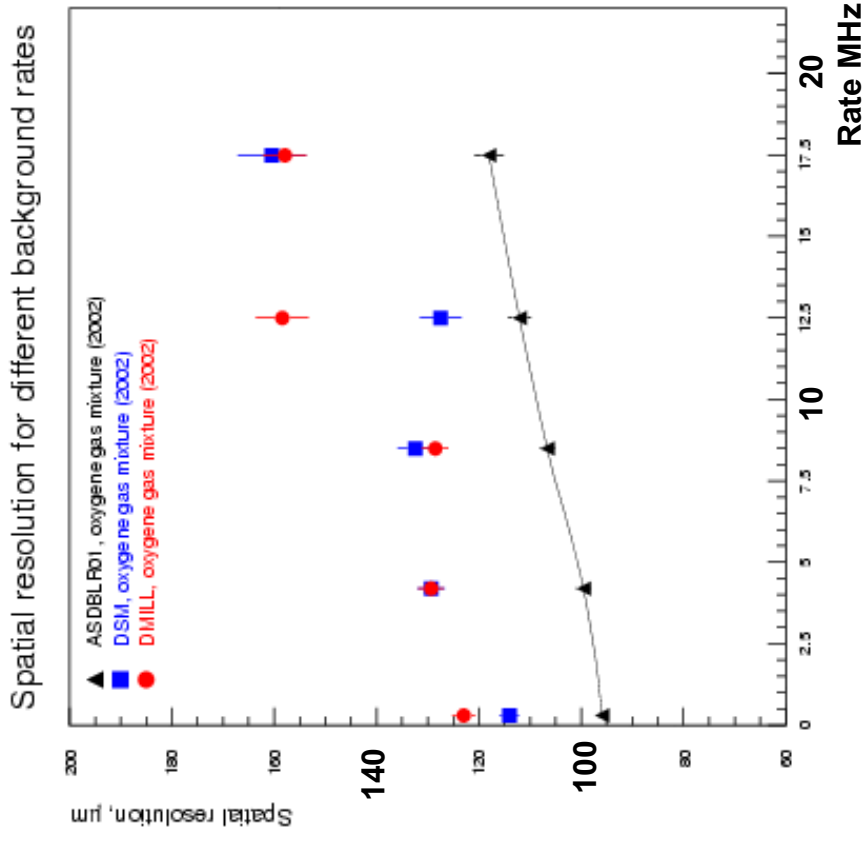
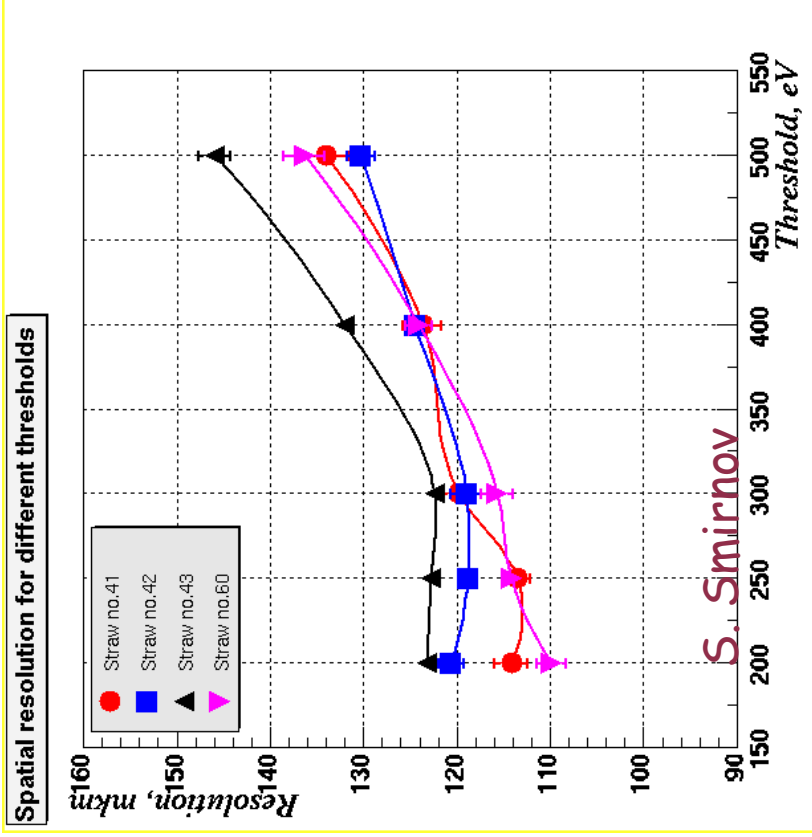


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Test Beam Measurements Spatial Resolution

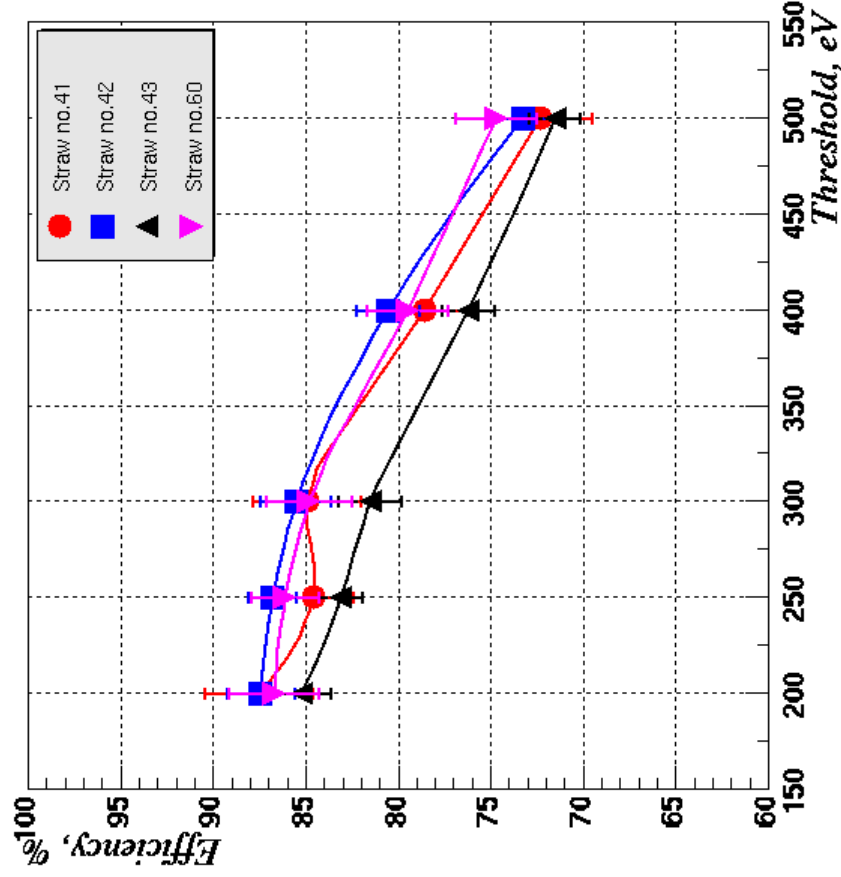
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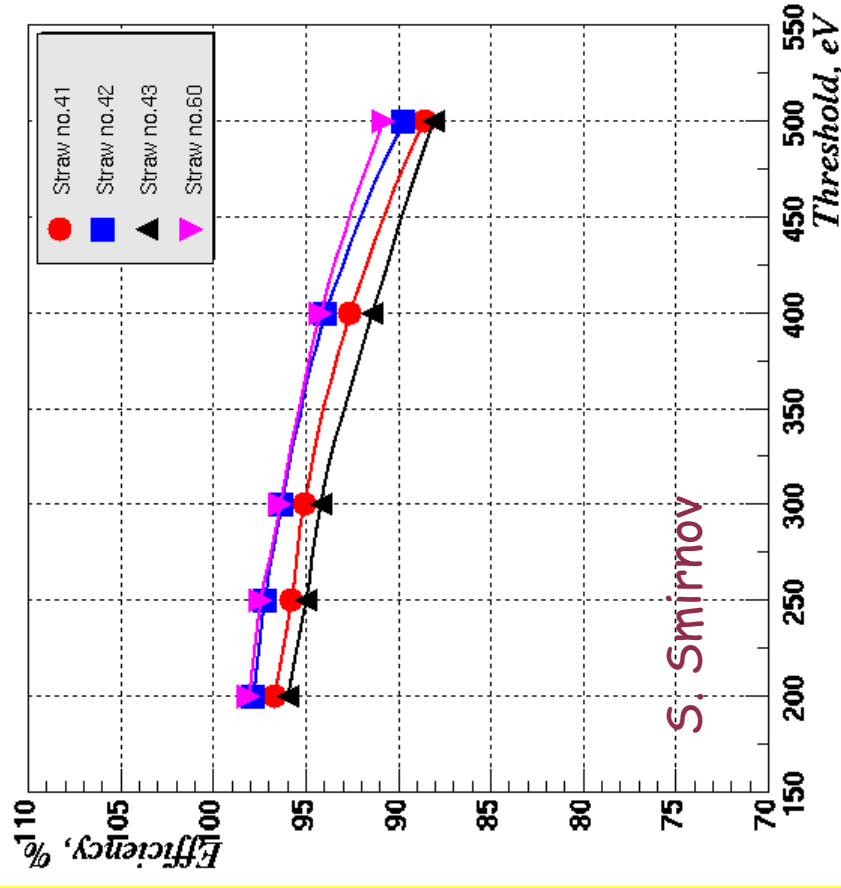
Test Beam Performance of Production ASICS and near final prototype boards.

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2.5-sigma efficiency for different thresholds



Total efficiency for different thresholds



S. Smirnov

Summary

ATLAS TRT
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- ASDBLR and DTMROC ASICs are in production and have been shown to meet TRT design objectives.
- Development of Production ASIC Testing Facility is nearly finished.
- Design of Boards with both analog and digital ASICs on them is underway and we have very promising results to date.
- Radiation Testing of ASDBLR ASICs indicates n_{pn} neutron sensitivity that may limit lifetime to ~8 years when safety factors are considered.
- Thermal neutron content of TRT environment needs study.