The ASDBLR and DTMROC Detector Mounted Readout for the ATLAS TRT

Mitch Newcomer for the ATLAS TRT Electronics Group

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TRT Wheels
Radially Aligned Straws (320K channels)

TRT Front End Electronics
Axially aligned 100K channels

Barrel Modules
Detector Mounted Readout Objectives

- Low Noise/Low threshold operation $\rightarrow \sim 2000e$ ENC
  $< 300KHz$ spontaneous straw tube trigger rate
- 1ns time resolution $\rightarrow \sim 130\mu m$ position resolution
- High Rate operation $\rightarrow$ 20MHz with stable threshold
  (100:1 Signal variation)
- Radiation Tolerance $\rightarrow$ $3.5 \times 10^{14}$ n/cm 5MRad
- Reliable operation of high bandwidth Analog and Digital readout ASICs without interference
- ATLAS Read Out Driver Compatibility
Readout Electronics

basic block

16 channel custom ASIC triplet
Implementation of the ASDBLR Straw Tube Readout
ASIC in DMILL Technology
N. Dressnandt, N. Lam, F.M. Newcomer, R. Van Berg and H.H. Williams

An Amplifier-Shaper-Discriminator with Baseline Restoration
for the ATLAS Transition Radiation Tracker
B. Bevensee, F.M. Newcomer, R. P. Van Berg and H.H. Williams

http://www.hep.upenn.edu/atlas
ASDBLR
8 Ch Analog Front End

Avalanche Straw signal with ion tail

Differential Signal Processing

Dual Preamp

Shaper Tail cancellation

Baseline Restorer

Discriminator

Tracker

Gain ~2X10^4

Negative HV

Stray

Shaper BLR (Top) (under)

20ns/box

Tracking Comparator Input gain ~18mV/fC
Track Threshold Gain ~ 120mV/fC
TR Threshold Gain ~ 10mV/fC

Ternary Out

20ns/box

DTMROC

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ASDBLR Basic Design Spec

- Power ~ 40mW/ch.
- Preamp Input protection ~ 2.8mJ.
- Analog Gain ~ 18mV/fC at Comparator input.
- Double Pulse Resolution ~ 25 – 50ns dependent on 1st pulse amplitude.
- Spontaneous Trigger Rate at 2fC threshold ~ 300KHz.
- High Threshold Maximum Range → 140fC.
- Ternary (comparator) output levels (nominal Design):

<table>
<thead>
<tr>
<th>Signal</th>
<th>Tern Pos</th>
<th>Tern Neg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiescent</td>
<td>-400μA</td>
<td>0μA</td>
</tr>
<tr>
<td>Track only</td>
<td>-200μA</td>
<td>-200μA</td>
</tr>
<tr>
<td>Track &amp; TR</td>
<td>0μA</td>
<td>-400μA</td>
</tr>
</tbody>
</table>
ASDBLR Implementation

- Process - Rad Tolerant 0.8um BiCMOS Technology (DMILL)
- Designed at the discrete device level using SPICE for Simulation
- Channel Complexity 160 Bipolar Transistors / 10 CMOS Switches
  160 Resistors / 105 Capacitors

- Channel based Layout ~
  Avoided metal runs over transistors/resistors.
  Double vias where possible.
  Separated Analog and Comparator/Ternary Driver Power
  Dedicated power bus distribution at the channel level.
  Substrate Contact and Power buss isolation between ch.
  Preamp Supply filter on each channel.

- Eight (nearly) identical Channels on 340um Pitch

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ASDBLR design Cycle

Schematic Level Design and Simulation

Layout Driven Schematic Revision

Foundry Provided Library Parts

Develop New Library Parts

Layout

Netlist Extraction with parasitics Simulation with Extracted Schematic

Fabrication (20 weeks)

Test Devices

Package

Performance Driven Schematic Revision

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Final Design Improvements

- Reduce area of input protection network → Reduce Capacitance 11pF → 5pF.
- Increase Input transistor current to 7.5uA/m reduce beta loss.
- Increase analog gain by 50% to reduce sensitivity to device matching in comparator. (56mV/fC at BLR output)

Measured Results

- Input referred threshold matching good, RMS < 0.25fC
- Noise ~ 2100e ENC on board with ~5pF capacitance (100e/pf).
- Power ~ 40mW/channel.
- High Rate operation ~ demonstrated to 20MHz (pulser tests)
Production ASDBLR

Dual Preamps intermingled layout
Input Transistors in cross Quad Configuration
Input protection NPN Transistors
Expanded Geometry Emitter Stripes 4 x 30 um

Comparators
B L R's
Shapers
Preamps

3.3 X 3.6mm

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ASDBLR Radiation Testing

• Gamma Testing up to 7MRad with no significant performance degradation.

• 1MeV NEIL Neutron Testing to $5 \times 10^{14}$ (10 year with safety factor) shows a significant reduction in beta resulting in lower gain and increasing the channel to channel threshold offset. At Beta = 30 the gain is lowered by $\sim 50\%$.
  - DMILL NPN Beta is sensitive to Thermal Neutrons
  More study needed. Moderator re-evaluation?
Neutrons

Thermal Neutrons present at the Ljubjana facility point out a possible weakness using the DMILL Process. Careful comparison of these results with the expected exposure in the ATLAS ID need to be performed.

All devices annealed at 150° C for 48 hrs.
ASDBLR Radiation Testing report NSS 2002

Summary of Device tests to 11 / 2002

<table>
<thead>
<tr>
<th>ASDBLR</th>
<th># chips</th>
<th>Power on Date</th>
<th>Type Dose $^1$</th>
<th>Change in Resistance</th>
<th>Post Rad NPN Beta</th>
</tr>
</thead>
<tbody>
<tr>
<td>99</td>
<td>3</td>
<td>4/00</td>
<td>5X10$^{13}$ n</td>
<td>NA</td>
<td>84</td>
</tr>
<tr>
<td>3</td>
<td>4/00</td>
<td>1X10$^{14}$ n</td>
<td>NA</td>
<td>52</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>x 5/01</td>
<td>5Mrad $^\gamma$</td>
<td>5%</td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>9</td>
<td>10/01</td>
<td>3.5X10$^{14}$ n</td>
<td>1.5%</td>
<td>55 $^3$</td>
</tr>
<tr>
<td>01</td>
<td>6 x 6/02</td>
<td>1.5X10$^{14}$ p</td>
<td>5%</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>16 x 7/02</td>
<td>7MRad $^\gamma$</td>
<td>8%</td>
<td>130</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>10 x 5/02</td>
<td>3.5X10$^{14}$ n</td>
<td>10.4%</td>
<td>11 $^2,3$</td>
<td></td>
</tr>
</tbody>
</table>

$^1$ n and p dose is in units of particles/cm$^2$.
$^2$ Thermal neutron dose high ~10$^{14}$ n/cm$^2$.
$^3$ After annealing 23hrs@150C

The measured current gain of DMILL NPN transistors after exposure to 3.5X10$^{14}$n/cm$^2$ and prior to annealing. The arrows show the operating points chosen for various parts of the ASDBLR channel design. After annealing the beta increased by a factor of two.

From: Radiation Hardness: Design Approach and Measurements of the ASDBLR ASIC for the ATLAS TRT

Nandor Dressnandt, Mitch Newcomer, member IEEE, Ole Rohne and Steven Passmore

See NSS 2002 Conference Record
CERN MicroElectronics and Penn

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DTMROC References

Implementation of the DTMROC-S ASIC for the ATLAS TRT Detector in a 0.25µm CMOS technology


NSS 2002 Conference Record

Progress in the Development of the DTMROC Time Measurement Chip for the ATLAS Transition Radiation Tracker (TRT)


http://hep.upenn.edu/atlas
DTMROC
functional Blocks
DTMROC-S
Time Marking

32 elements delay chain, phase detector, charge pump

40MHz Clock → 3ns time bins

- 8 equally spaced clock outputs used to sample straw track pulses

- 50% duty cycle clock regenerated to run the chip core logic
DTMROC-S
Memory / Pipeline

Dual-port 128×153-bit SRAM (2.39kB)

V. Ryjov

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DTMROC-S
I/O

- Full/Reduced read-out: 444/380 bits per event, including Header
- LVDS-compatible, tristate drivers → 40 Mbits/s copper links
- Wire-OR” - for self triggering
fast-out option - selected
ternary inputs contribute
to the chip-level trigger
Up to 15 DTMROCs can be
“OR’ed on a common buss
DTMROC-S DAC's

- Internal bandgap reference 1.26V
- Current mirror master - 128 PMOS unit devices (L=8um, W=5um)
- 256 identical PMOS slave current mirrors per DAC

V.Ryjov
DTMROC-S
Analog Sensing

- Two DACs
- Four Comparators
  - Temperature
  - VDD
  - Ext Voltage 1
  - Ext Voltage 2

Vdd Sense remained at 191 from 26 - 55 C
DTMROC-S testability

- General-purpose 32-bits Status Register
- Logical OR of all DTMROC error indicators in the Data Header field
- Parity check logic for all internal registers
- Lock status, a “watch dog” and a “dynamic” check circuitries examine the DLL
- JTAG Boundary-Scan
- Special scan mode - configures all DTMROC flip-flops as a large shift register controlled via JTAG interface
- Memory Build-In-Self-Test (BIST) controlled via the Configuration register and JTAG interface
Internal registers are equipped with parity error check.

The most critical parts are built of the SEU resistant and self-recovering elements based on triple logic with majority vote.

Statistics circuit monitors the number of detected SEU’s.
DTMROC-S
Design Tools
(CERN based)

- Verilog modelling
- Synopsys synthesis tools
- Silicon Ensemble Place&Route tools
- Completely scripted physical design flow
- Number of synthesis-layout cycles to predict post-route timing during RTL synthesis
- NC Verilog Simulator – Interleaved Native Compiled Code Architecture

Behavioral Model

Synopsys synthesis

Verilog

Synopsys Library Compiler

Netlists

Place & Route

Technology Library

NetLoad Table

HyperExtract

Layout

V.Ryjov
DTMROC-S Layout

~500k Transistors

Die size 5.2×5.0 mm²
DTMROC-S
Fab

- Submitted/fabricated (.25um process) in Jan 2002
  - Wafer size 8" (350µm) → 1017 useable dies per wafer
- 850 chips tested on the mixed signal IMS Tester at CERN
- 5 process corner (85/92/100/115/125%) evaluated
- 87% Yield for 850 chips
- Irradiation tolerance test at CEA Saclay Pagure facility in July 2002
- SEU sensitivity evaluated at the CERN PS in July 2002
- Test Beam at the CERN H8 in August-September 2002
DTMROC-S  
Radiation Testing

**Total Ionizing Dose tolerance**
- Tested at CEA Saclay Pagure facility in July 2002
- 7 Mrad total dose / 1.33 MeV gamma radiation
- ~10% increase in the DAC’s output voltage after irradiation, no DNL change
- No variations in the power consumption and the chip performance

**SEU sensitivity**
- Evaluated at the CERN PS irradiation facility in July 2002
- Integrated fluence of $1.8 \times 10^{14} \text{p/cm}^2$ on 24GeV beam
- SEU cross-section for a single D flip-flop in different internal registers varies from $0.8 \times 10^{-14}$ to $1.2 \times 10^{-14} \text{cm}^2$
- Impact of SEU’s in the vital components is suppressed by self-recovering logic
ASDBLR & DTMROC
Packaging  Labeling

Fine Pitch Ball Grid Arrays

Laser Marked packages
2D  Bar code
Human Readable
numbering

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ASIC Testing
ASDBLR
DUT Board on IMS

DUT Board
With FBGA Socket

Exatron Robot

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IMS Tests on ASDBLR

Read Bar code and record test (event) Number

- Supply Current
- Input voltage/resistance
- Output current / switching
- Low Threshold response to 0, 2, 3 fC input
- High Threshold response to 30 fC.

Write Results to SQL data base
Failures Due to Socket Pin Reliability

INPUTS, Lot # 125

OUTPUTS, Lot # 125

Unreliable Pin Contact On Output

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Using Forced Air to clean pogo pins
Finding ASDBLR
50% Threshold

Q1 TestNum 8633, Ch5, 30mv Sp

Fit threshold curve to find 50% points

Volts

0 0.6 0.65 0.7 0.75 0.8 0.85

0 20 40 60 80 100

Occupancy

50% ep = 0.746, chi sq = 2.7e−04
First 3000 chips demonstrate minor problems.

Socket pins must be cleared with forced air daily.

Some wandering of the threshold 50% points day to day.

Bar code too close to chip label, leads to ~5% read errors.

False failure rate ~10% presently. Should improve over time.
Yield on First 3000 Devices with Beta Testing version

Yield vs. Q1 Matching

Represents Yield of ASICS and Tester

Target for Final Acceptance

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End Cap Wheel Boards

- 192 channels per assembly
- 2 DTM Board’s = 1 virtual module.
  - 1/32 of endcap type A wheel
- Flexible interconnect between 64 channel DTMROC boards allows 192 channel board to follow curvature of wheel tread.
- Initial noise measurements on prototype detector show operation at 2fC possible.
Barrel Module Board with 15 ASDBLR / DTMROC triplets
Noise Rate Plot with Barrel ModuleBoard and Pulser

6 MHz = 50% Pulser Efficiency (note that Pulser adds noise)
Analog and Digital Readout on the Barrel Module Board (good Channel)

50% Efficiency Dac Setting by Time Bin

~ 24 Counts/fC

75ns

5mV/ Dac

Test Pulse response
**Beating Down Pulser Noise using DTMROC Timing window**

**ATLAS TRT FEE2003**

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**50% Threshold VS Input Charge**

![Graph showing the relationship between DTMROC DAC counts and pulser input charge, with 50% threshold. The graph includes data points for full 75ns time window and 12ns time window, indicating 24 Cnts / fC and 140 mV / fC.]
Test Beam Measurements
Spatial Resolution

Spatial resolution for different thresholds

S. Smirnov

Spatial resolution for different background rates

AS DBL R01, oxygen gas mixture (2002)
DSM, oxygen gas mixture (2002)
DMILL, oxygen gas mixture (2002)

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Test Beam Performance of Production ASICS and near final prototype boards.

2.5-sigma efficiency for different thresholds

Total efficiency for different thresholds

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Summary

• ASDBLR and DTMROC ASICs are in production and have been shown to meet TRT design objectives.
• Development of Production ASIC Testing Facility is nearly finished.
• Design of Boards with both analog and digital ASICs on them is underway and we have very promising results to date.
• Radiation Testing of ASDBLR ASICs indicates npn neutron sensitivity that may limit lifetime to ~8 years when safety factors are considered.
• Thermal neutron content of TRT environment needs study.