

Test Results of the TRT Barrel Front End Type 1B Prototype Boards

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Abstract

We report on the test results of the type 1B TRT barrel front-end boards performed with a TRT barrel sector prototype at CERN, and with a single module prototype at the University of Pennsylvania. The experimental setup, grounding connections, and the measurement methodology used for the characterization of the boards (noise rates at the operational thresholds, digital clock pickup, and data read-out induced noise) are described in detail. Preliminary measurements of the electromagnetic interference between modules are reported. We conclude that the noise performance of the type 1B boards is completely satisfactory: 2% occupancy is achieved for thresholds of ≈ 115 DAC counts, which are 50% efficient for 250 eV signals. However, electromagnetic interference between different instrumented modules resulting in a few channels with higher noise is observed. Further studies in a multi-module environment are currently under way.

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1 Introduction

This note describes the test measurements performed with almost final prototypes of the TRT front-end electronics of the back side of the type 1 modules. A TRT barrel sector prototype at CERN, and a single module at the University of Pennsylvania was used for the tests. The note is organized as follows: Section 2 describes the TRT barrel module and barrel sector prototypes used for the testing at UPenn and CERN, respectively. Section 3 gives a succinct description of the type 1 back side boards. The design highlights the most relevant succinct features, and the design development history from early prototypes is described in detail in the Appendix 10. Section 4 describes the grounding necessary for the optimal noise performance of the boards. Section 5 describes the methodology and physical measurements used for the characterization of the board performance. Section 6 discusses the test results performed both at UPenn and CERN. Section 7 reports some preliminary results in module to module electromagnetic interference observed with the CERN sector module prototype. Finally, Section 8 summarizes the obtained test results.

2 Sector and Module Prototype

The barrel section of the TRT [1] is comprised of three cylindrical rings, each containing 32 identical and independent modules of 144 cm length. The anode wires are electrically separated in the middle by a glass wire joint and are read out from both ends. Boards used to read out one side are conventionally designated F (front) type¹ while the boards used to read out the other side are named B (back) type. From the innermost to the outermost, modules are called *type 1*, *type 2* and *type 3*, respectively (Figure 1). Each module on each side is read out by two different types of boards. The board with the lower number of read out channels has the suffix *S* (small) in its denomination, while the other one has the suffix *L* (large). Therefore, *e.g.*, a board located in a type 2 module, front side and with the lowest number of read out channels will be referred to as *2FS*. Figure 2 shows the relative space positioning of the different boards. Table 1 summarizes the number of electronic readout channels and straws corresponding to each board².

2.1 Experimental Setup at Penn

Figure 3 shows the experimental setup used at Penn for the characterization of the 1BS and 1BL boards. A type 1 barrel module was inserted inside of a PVC cylinder of the same length and held by means of insulating foam in the center of the cylinder. The

¹This denomination is taken to be consistent with the side denomination as provided in the module passports.

²The readout electronics is segmented in units of 16 readout channels (triplets consisting of 2 ASDBLR chips and 1 DTMROC chip, see Section 3), while the number of straws for each module is not a multiple of 16, and therefore some electronic channels are not connected to any straw).

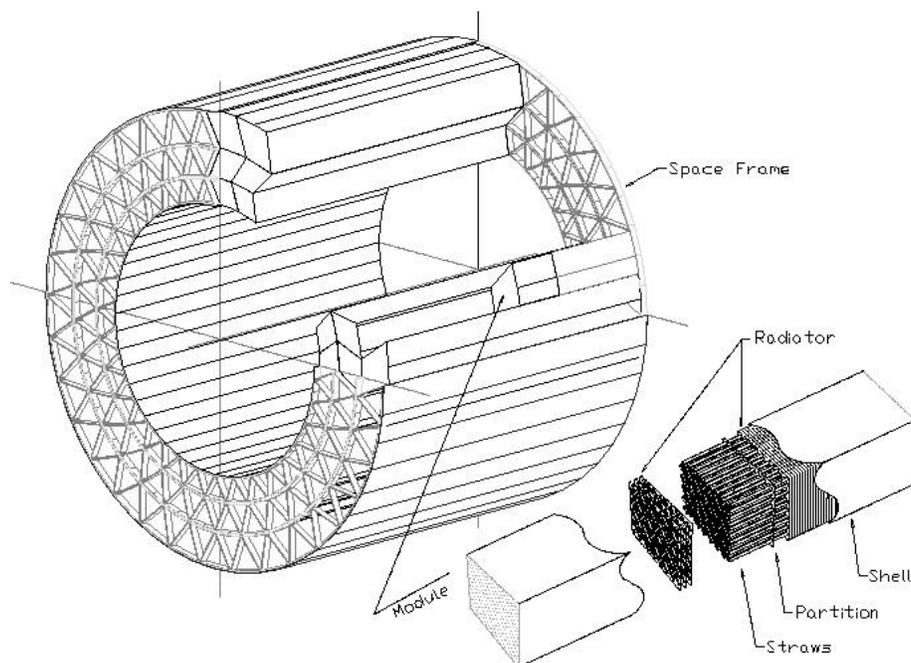


Figure 1: Layout of the barrel TRT with the three concentric rings of 32 identical modules each. Also represented is an exploded view of one module, showing the carbon fiber shell, the wire support, the radiator for the generation of transition radiation photons, and the straws.



Figure 2: Schematic representation of the position of each front end board on the end of each module.

PVC tube was covered with aluminum foil to mimic the designed Faraday shield of the barrel. At each end of the module an aluminum mock-up of the support structure for the modules was attached. These structures were electrically isolated from the module, but connected to the aluminum foil of the Faraday shield.

BOARD	Module Type	DTMROC's	Read Out Channels	Straws
1BS/1FS	1	10	160	153
1BL/1FL	1	11	176	176
2BS/2FS	2	15	240	240
2BL/2FL	2	18	288	280
3BS/3FS	3	23	368	363
3BL/3FL	3	27	432	430

Table 1: Module type, number of DTMROC's chips, number of electronics' read out channels and number of the straws for each front end board type. Note that the number of straws is less than the number of electronics' readout channels, and therefore some of the latter are not connected to any straw.

For the read out, the DAQ system consisted of one mini ROD and one TTC with their corresponding patch panel. The cables connecting the patch panel to the end boards were $\approx 4 - 6$ m long³. The patch panel was connected to the mini ROD and TTC with short flat cables, that are radically different from the final ones which will be approximately 100 m long.

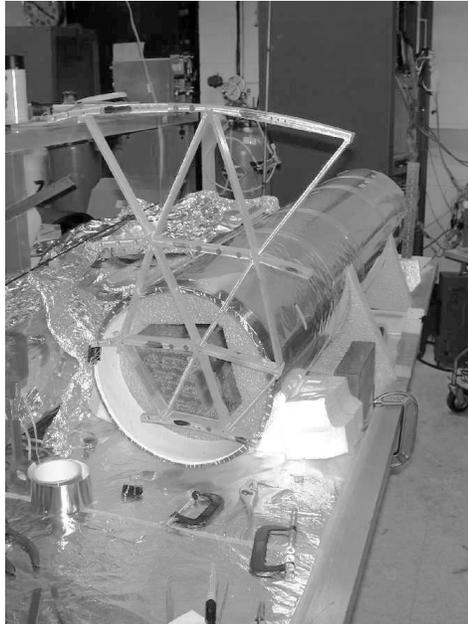


Figure 3: View of the module type 1 setup used at Penn for the test of the boards.

³The final cables will be approximately 13 m long.

2.2 Experimental Setup at CERN

Figure 4 shows the experimental setup at CERN, in the H8 test beam area. The barrel sector prototype with two type 1 modules and 1 type 2 module from the August 2003 test beam was used. The sector prototype was instrumented on one side with one 1FS, one 1FL and one 2FL board, and on the other side with a new 1BS, and one new 1BL board. The whole structure was covered with a thin cooper sheet acting as a Faraday shield. The sides of the sector not instrumented with front end boards were covered with metallic plates that mimic the electronics' cooling plates; whether the boards themselves were covered with their corresponding cooling plates depended on the type of tests and measurements. Neither the high voltage nor the cooling system was connected⁴.

For the read-out, a similar system to the one at Penn was used, but with longer cables (≈ 20 m) between the patch panel and the mini Rod and TTC VME crate.

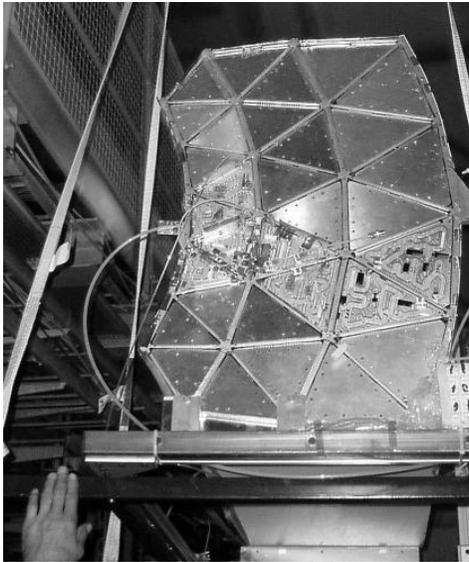


Figure 4: View of the sector prototype at the H8 test beam area at CERN. Only two type 1 modules, and one type 2 module are inserted inside the space frame.

3 Type 1B Front-End Boards

The TRT barrel electronics are located in a very narrow region at each end of the modules, where cables, electronics, the cooling system and the support system must fit into a space of 25 mm along the direction of the beam (Figure 5) [2].

The basic front end readout block consists of two ASDBLR chips (of 8 channels each) for analog processing of the signal from the straws, and one DTMROC chip (16 channels) for time measurements and pipelined data readout[3]. To host triplets of

⁴For cooling purposes a simple fan was used.

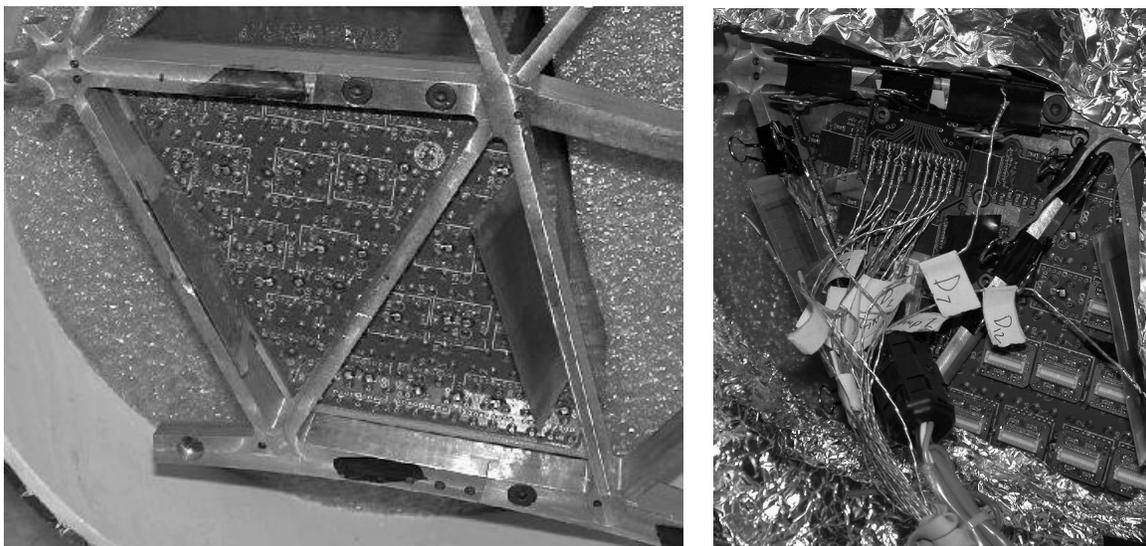


Figure 5: Left Figure: view of the end of a Type I barrel module. The support structure splits the trapezoidal cross section into two triangles. A single read out board is housed in each triangle. The straw wire anodes are arranged in groups of 16 straws with 6 ground connections (in the picture, these groups of 16 straws are enclosed in a white rectangle) that are connected with a single input protection board to two ASDBLRs. On the left side, the high voltage Kapton cable, covered with a Kapton film, is shown. Right Figure: view of the end of a Type I barrel module with a read out board (without cooling plate) in the upper triangle (only the data cables are shown, not the straw high voltage connections, cooling pipes or gas pipes). In the bottom triangle, several input protection boards -stuffed with protection resistors and diodes- are shown. Each input protection board connects two ASDBLRs to 16 straws.

two ASDBLRs and one DTMROC, several board designs and approaches have been investigated; the final design converged on a single board that houses the ASDBLRs on one side and the DTMROCs chips on the other side (Figure 6). A detailed exposition of the design highlights and development history is given in the Appendix.

4 Grounding Connections

Proper grounding connections are a very delicate issue, since they define the different reference voltages with a direct impact on the return currents. Figure 7 shows the grounding scheme adopted in the current setup, and Figure 8 the actual connections that were implemented. In the original scheme [2], the ideal signal return path will follow from the ASD preamplifier to its power ground (analog ground), and then through 6 pins in the protection input board to the tension plate to the common ground of all the high voltage decoupling capacitors. However, from the early stages of the front-end board design, it was observed that external currents induced by the bouncing of the DTMROC power ground and other sources (see the Appendix) were added to this

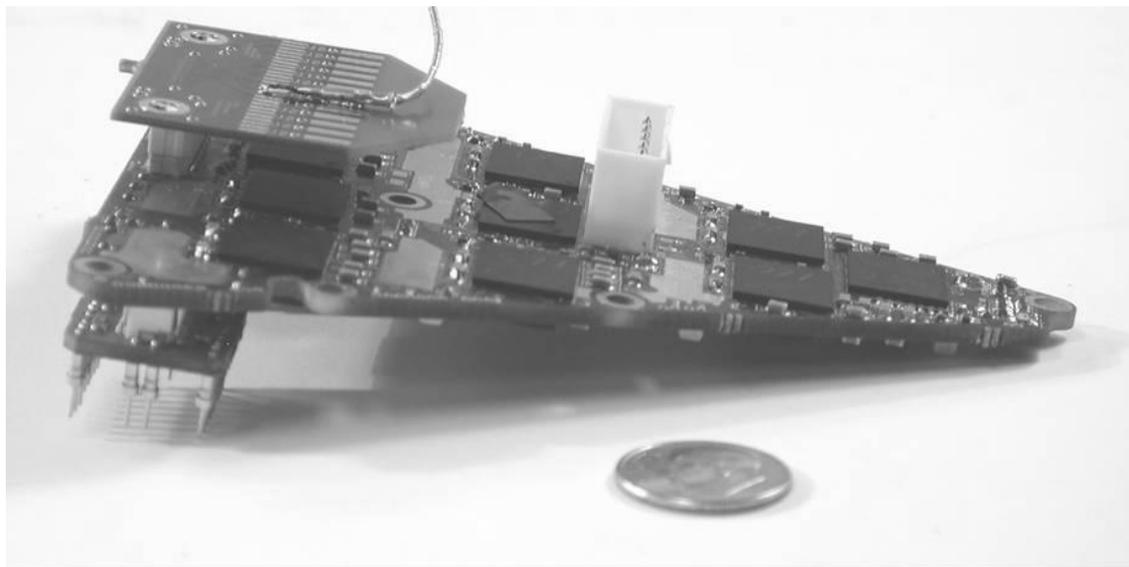


Figure 6: Lateral view of 1FS barrel board. Top side corresponds to the digital side, where 10 DTMROCs in FBGA packages are seen surface mounted. On the left side, in one location at the bottom, one protection input board is attached. An unstuffed PCB board for the data cables is attached to the top of the board. The white connector in the center of the board is the power connector.

return path, corrupting the straw signal. To redirect such currents and avoid their overlap with the signal return, a low impedance path has been created attaching the analog ground directly from the ASDBLR side of the front end board (Figure 9) to the space frame. The massive space frame serves to maintain an equipotential among modules so that energy from clock and other noise sources is channeled to a common reference while the straw readout measures the difference between the reference and the straw anode. However, it must be noted that the addition of several modules can potentially change the environment of current flow. Tests with several modules are currently under way and will be reported in a future note.

5 Methodology for Performance Characterization

To characterize the performance of the boards, a set of operational parameters must be defined that allows us to determine what signal efficiency is achieved for an acceptable noise rate. In this section we discuss the signal efficiency, and the methods used to measure and characterize the noise rate.

5.1 Signal Efficiency

A detailed description of the whole signal processing chain can be found in reference [3]. The final data available for tracking reconstruction consists of a stream of 27 bits

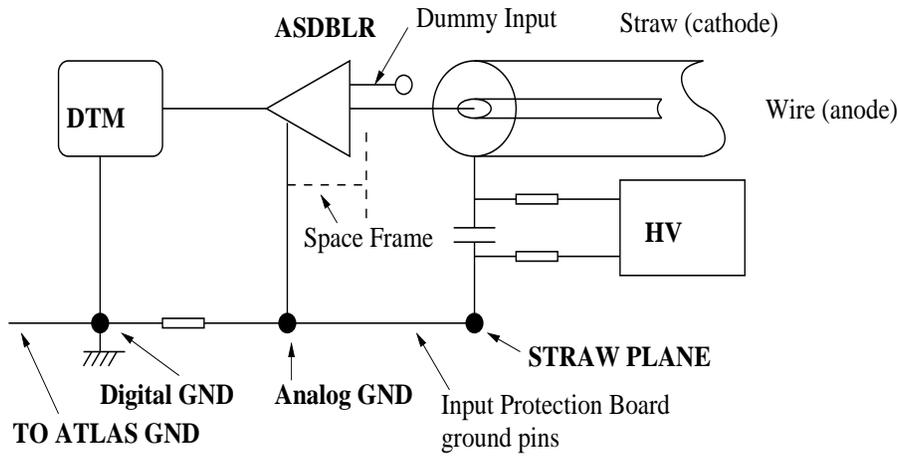


Figure 7: Conceptual design of the grounding connections. The dashed lines represent the connection between the analog ground of the ASDBLR from dedicated pads on the barrel front-end board to the space frame. This connection was not foreseen in the original design.

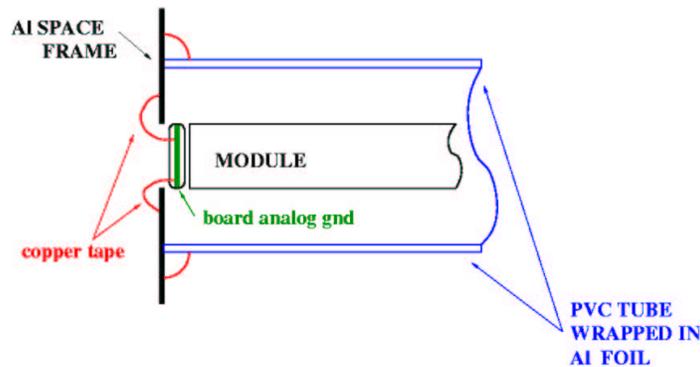


Figure 8: Grounding scheme of the setup. The analog ground of the board was attached to the Aluminum space frame by means of copper tape. The aluminum space frame is also attached with copper tape to the PVC tube wrapped in aluminum foil, which is attached to a large metal table. The cooling plate (not shown) is placed immediately on the top of the board from the outer side and was left floating for these tests.

for each straw, corresponding to three successive bunch crossings. For each bunch crossing, one bit is used to mark the presence of a signal above the high threshold at any time during the bunch crossing (the high threshold hit)⁵, and the remaining 8 bits

⁵ After the incoming signal from the straw has been shaped and the base line restored, the ASDBLR has two different individually programmable comparators for each channel. A low level comparator detects the presence of the first primary electrons produced by the ionization of the gas by the crossing charged particles, and a high level comparator, set to a higher level ($\times 10$), detects transition radiation photons produced by the incoming charged particles traversing the straw and the radiator material between straws. For each bunch crossing, the DTMROC digitizes the ASDBLR low level comparator output into eight 3.12 ns time bins, and the high level comparator output is stored in one bit, signaling

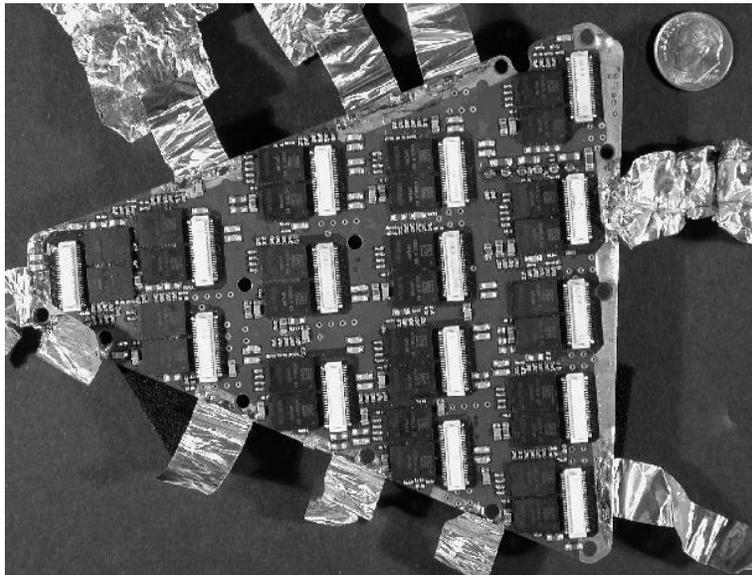


Figure 9: View of a 2FS board from the ASDBLR side. The copper strips are used to attach the analog ground to the space frame through a specially designed metal strip following most of the board border.

are used to mark the presence of a signal above the low threshold (low threshold hit) in successive time bins of 3.12 ns ($8 \times 3.12 = 25$ ns, a complete bunch crossing). Therefore, the high threshold hit allows for the detection of the presence of a transition radiation photon, characterized by its high energy deposition in a bunch crossing, while the low threshold allows one to detect and measure the time when hits due to gas ionization by charge particles occur.

In order to detect hits due to ionization by charge particles with acceptable time resolution, and thus position resolution, the thresholds must be set sufficiently low. The amount of charge collected by the anode wire depends both on the gas gain and the trajectory of the charged particle inside the straw[2]. The ASDBLR has been designed to collect the charge in a window of 7.5 ns (collecting about 15% of the total charge including all of the so called electron component of the ionization), and to cancel the long tail (several hundreds of ns) which is due to the drift of the slower positive ions. It is optimal for the track comparator threshold to be as low as feasible for two reasons. First, for high detection efficiency, we would like to detect tracks that traverse only a small part of the straw's cross section, and therefore dislodge only a few primary electrons. More importantly for the best drift time resolution, we would like to detect the avalanche signal from the first primary ions arriving at the wire. Primary electrons from tracks traversing the straw near the center will drift to the wire over 35 ns. Only the earliest electrons can be used to determine the point of closest approach to the wire. Since the drift velocity is $\approx 100 \mu\text{m}/\text{ns}$, errors of 1 ns can significantly distort the drift time accuracy. Typically, the low threshold must be set low enough to be efficient

its presence or absence during the whole bunch crossing.

for pulses of 2 – 3 fC.⁶

Low Hit Definition

A low threshold hit can be defined in two different ways: as the presence of a low threshold comparator hit in any of the 8 time bins in any of the three bunch crossings (levels), or as the presence of a transition (leading edges) from low to high comparator outputs in a single time bin.

Calibration

Figure 10 shows a calibration curve obtained by injecting a known charge into one of the ASDBLR channels. To inject the charge, a switching current transistor pair controlled by a Lecroy 9211 pulser is used. The switching pulse had a 3 ns rise time and was ≈ 5 ns FWHM (Figure 11) The generated pulse was injected into the ASDBLR through the input pins of the protection input board. An external capacitor is added in parallel with the output of the injector to mimic the capacitance of the straw. The charge is measured by integrating the pulse over a 7.5 ns window with the oscilloscope. This procedure does not take into account the different pulse shape due to the gas ionization properties and other parameters, but has the advantage of its easy reproducibility. In this case, the DAC threshold that characterizes the pulse are defined as the thresholds for which the probability to find one low hit level (see previous section) in any of the three bunch crossings (75 ns window) when the pulse is injected is 50%. Figure 10 shows the calibration curve obtained for the two different time windows: 3 bunch crossings (75 ns) and a 12 ns window. The linear region for the 75 ns window extends from ≈ 1.5 fC pulses up to 4 fC. The upper limit was intended by design, while the lower limit is set by the noise of the system. This circumstance is proven by the fact that with a smaller time window for which a low threshold hit can be observed, linearity is conserved down to input pulses of ≈ 0.5 fC.

The procedure described above for calibration is only orientative, since the differentiation of the step pulse does not exactly mimic a signal which originates by ionization in the gas, and only serves for the purpose of having a fast check among different setups. A more definitive calibration was obtained during the August 2003 test beam [4]. In the test beam terminology, signal particles are not defined by the deposited charge, but by their deposited energy, corresponding to a well defined detector gas gain and other parameters. Table 2 shows the correspondence between particle deposited energy in eV and 50% efficient threshold settings, as used in the August 2003 test beam[4].

5.2 Noise Rate

Among other factors, the limited bandwidth of the data readout system imposes a limit on the number of channels with data that can be readout, and therefore on the

⁶Deposited charge is measured with respect to a deposition time window of 7.5 ns.

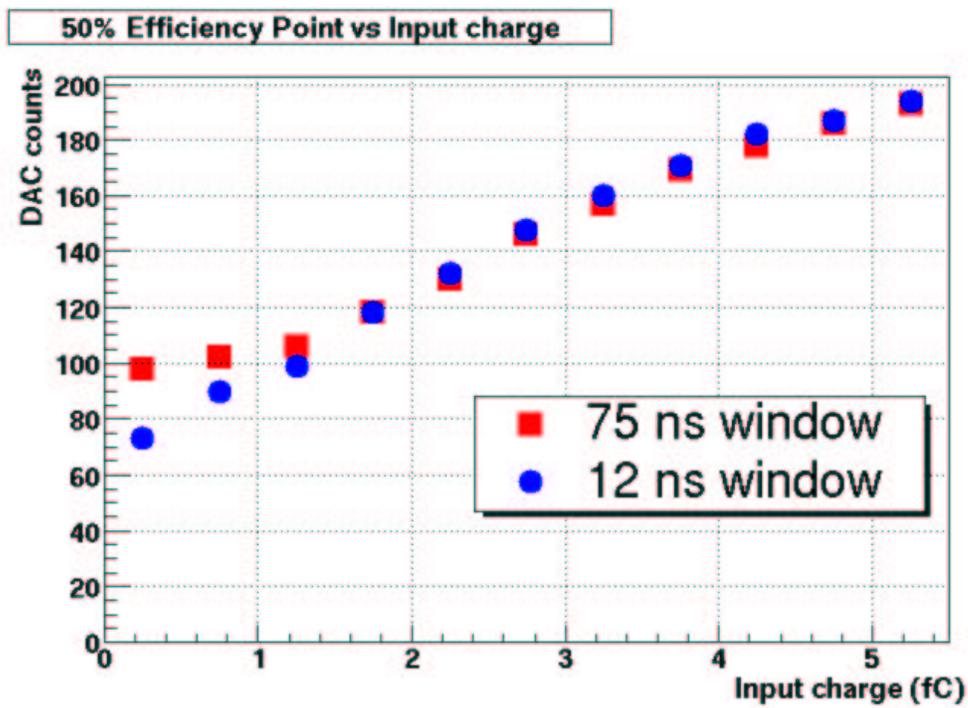


Figure 10: Calibration curve for one channel of a 1FS barrel board. A step pulse injector is attached to one input pin of a protection input board.

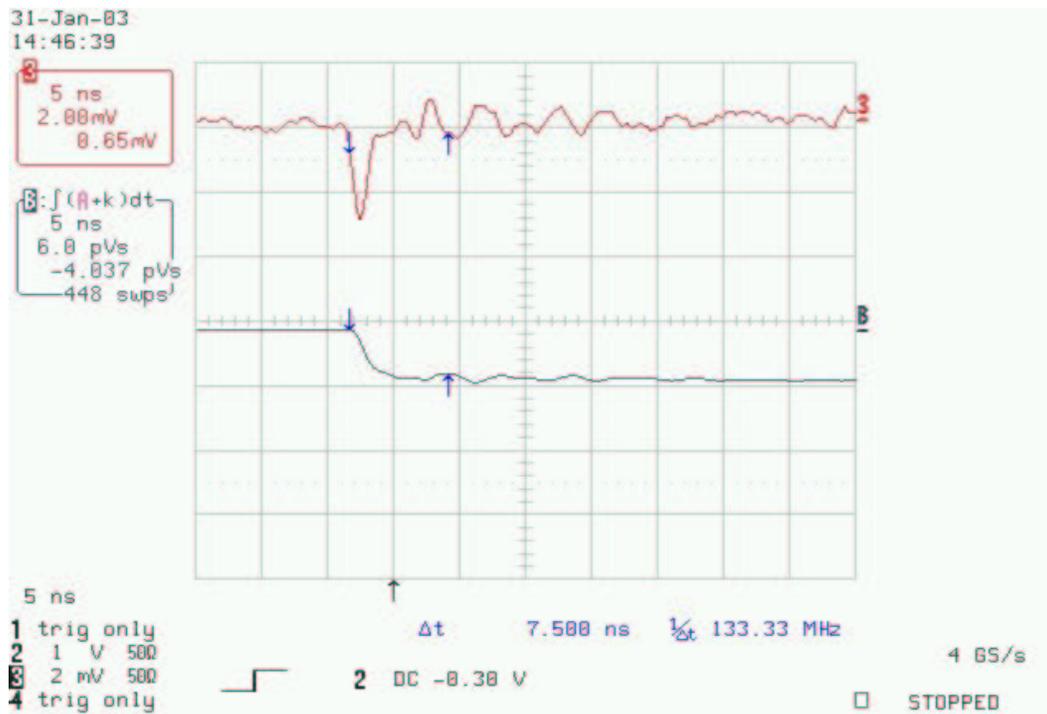


Figure 11: Scope screen shot of the calibration pulse injected to the ASDBLR.

eV	Threshold (DAC cts)
200	103
250	115
300	125
400	142
500	162

Table 2: Correspondence between particle deposited energy in eV and the 50% efficiency threshold in DAC counts, according to the August 2003 test beam results [4].

number of channels where a low threshold hit can be present.

To quantify and characterize the noise, the following four measures have been defined:

1. 300 kHz Noise Rate Thresholds
2. Clock Pickup Amplitude
3. Noise Slope
4. Data Read Out Pickup

5.2.1 300 kHz Noise Rate Thresholds

For low threshold hits in the TRT, a 2 – 3% occupancy level per channel is the upper limit[2]. If we consider a low threshold hit as a *leading edge* (see previous section), a 2% occupancy limit means having only 2 leading edges for every 100 acquired events. Since an event consists of 3 bunch crossings, lasting 75 ns, a 2% noise occupancy results in a noise event rate of 260 kHz. Therefore, a magnitude that serves to characterize the board performance and is easy to compute is the threshold for which a noise rate of 300 kHz is achieved. Figure 12 shows the noise rate as a function of the threshold for a typical channel of a 1BS board, attached to a module. In the ASDBLR, straw signals are expected to be negative going pulses, with a zero threshold for the comparator corresponding roughly to 40-50 DAC counts. Therefore, in the region between 40 to 50 DAC counts (near the zero threshold of the comparator) we observe the maximum noise rate corresponding to the maximum bandwidth of the ASDBLR (≈ 35 MHz). For lower thresholds the comparator is almost always fired, and therefore no transitions or edges are observed. In the case depicted in Figure 12, for thresholds bigger than 50 DAC counts the slope of the curve reflects the noise of the system.

5.2.2 Clock Pickup Measurement

One of the major issues in the design of an analog-digital system is the noise induced in the analog part of the system by the clock of the digital part (see Appendix). This

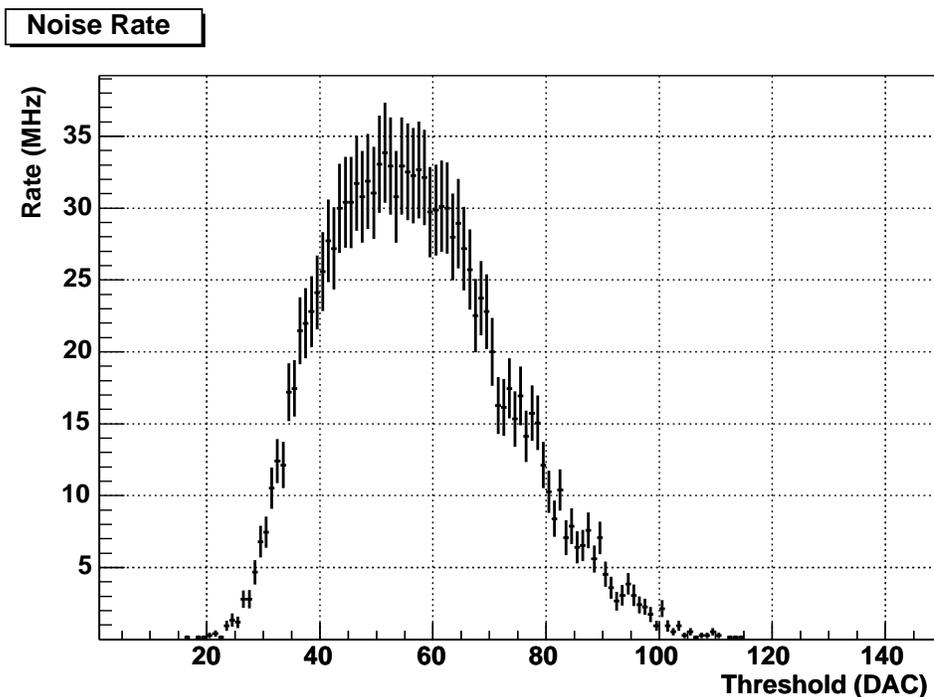


Figure 12: Typical noise rate curve for a TRT barrel channel attached to a module.

noise is synchronous with the frequency of the digital clock. One symptom is an increased number of leading edges or levels at regular time intervals, coinciding with the clock frequency. To quantify it, the following procedure has been developed. A threshold scan is performed, and for each time bin (3.12 ns) and threshold value, the probability to find a level (simply a low threshold bit set) is computed (Figure 13). After that, for each time bin we plot as a function of the time bin the threshold for which a 50% probability is reached (Figure 14). For channels with significant clock noise, a sinusoidal pattern is typical. The *Clock Pickup noise* is then defined as the difference between the maximum and the minimum 50% threshold value in all of the 24 time bins (corresponding to the 3 bunch crossings).

5.2.3 Noise Slope Measurement

Another way to characterize the noise is by measuring the slope of a threshold scan curve (Figure 15). For each threshold setting, the probability of having a level (simply a low threshold bit set to 1) over the 75 ns is computed, and plotted as a function of the threshold setting. For thresholds lower than ≈ 50 DAC counts the probability is always 100%, since the zero level of the ASDBLR comparator is ≈ 40 DAC counts. As the threshold increases, this probability decreases, and for high enough thresholds it turns to 0. In the absence of input signals, one can assume that the probability to have

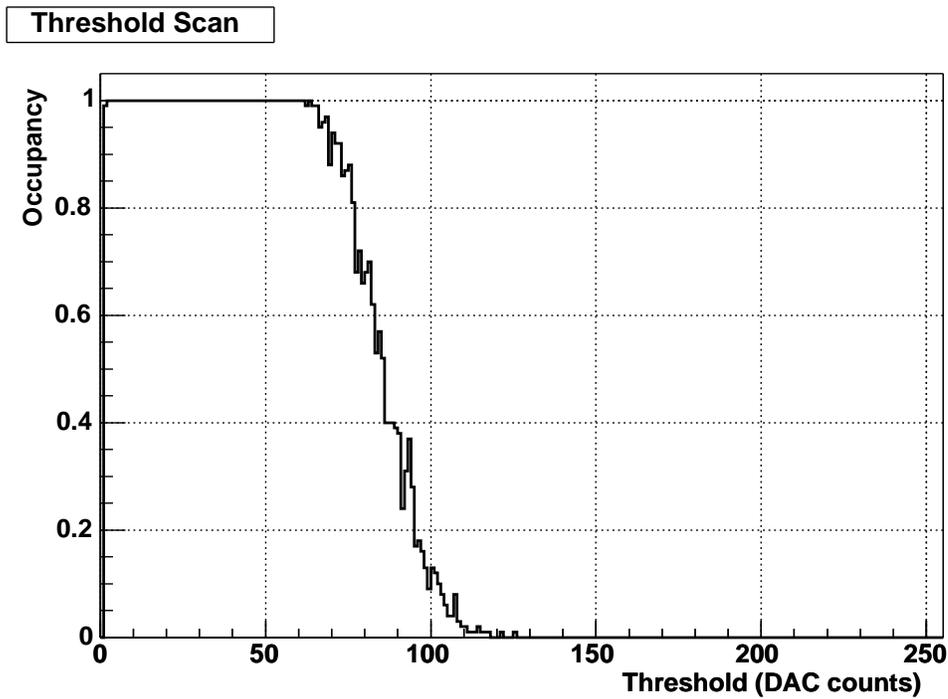


Figure 13: Typical threshold scan curve for a channel attached to a straw.

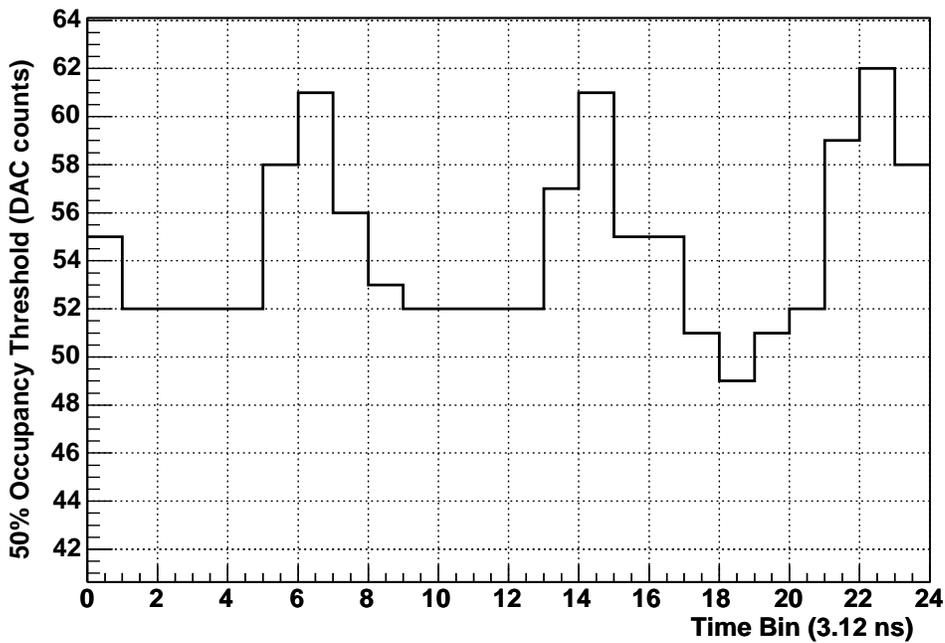


Figure 14: Typical clock pickup plot for a channel attached to a straw.

a low threshold hit follows a Gaussian distribution.⁷ Therefore, one can fit a threshold

⁷In the absence of a signal, the typical amount of noise charge seen by the ASDBLR due to the attached capacitance of the input protection boards, input protection network and straws is of the

scan to the following function

$$1 - \int_0^{255} e^{-\frac{(x-x_0)^2}{2\pi\sigma^2}} dx$$

and from the fit extract the values for x_0 (the 50% probability point) and σ (the noise). Figure 15 shows a typical threshold scan together with the fitted function.

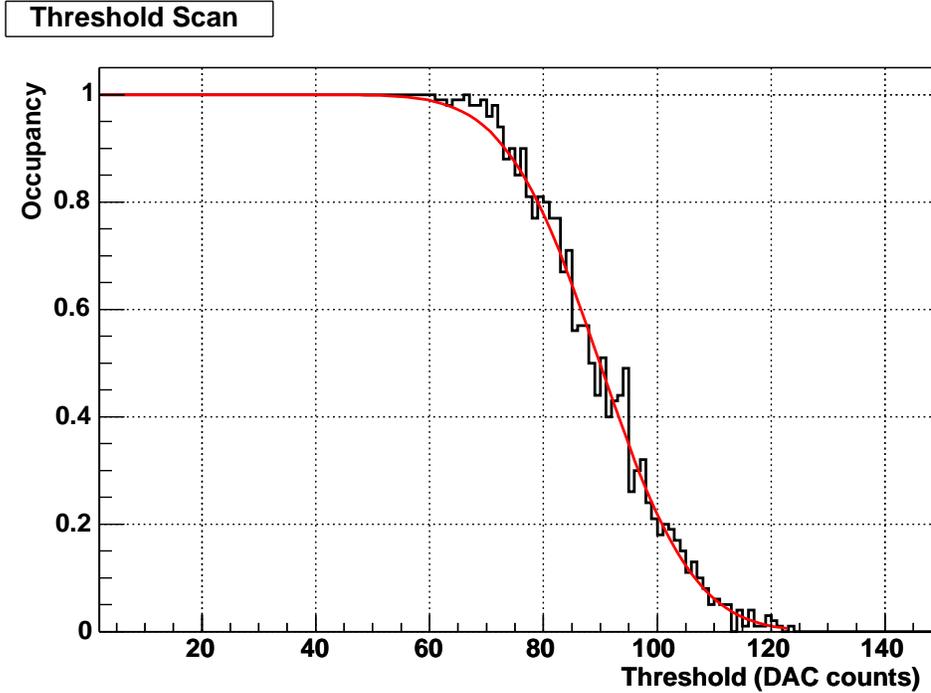


Figure 15: Typical threshold scan (black histogram) for an ASDBLR barrel board channel attached to a barrel module. The fitted *erfc* function is plotted in red.

5.2.4 Data Read-Out Pickup

With the actual bench test setup, triggers are produced from a workstation with a frequency of a few hundred Hertz. Once the ASDBLR is powered and the thresholds are set⁸ the ASDBLR sends whatever input signal pulses are over threshold to the DTMROC. The DTMROC digitizes the ASDBLR comparator outputs, and stores them in a pipeline of programmable depth (up to several microseconds). When the DTMROC receives a Level 1 Accept, it sends the data present in the last cells of the pipeline to the ROD buffer via Low Voltage Differential Signals (LVDS). A time delay in the TTC board allows for the synchronization the arrival of the Level 1 Accept signal with the presence of the event of interest at the last cell of the pipeline.

order of one femtoCoulombs, where the ASDBLR is linear.

⁸When the ASDBLR is first powered, the threshold are pre-set to the maximum value, and therefore no data is sent out to the DTMROC.

In our test bench conditions, where the acquisition rate is very low, it is unlikely that the acquisition of the event of interest by the ASDBLR and the data of the previous event read out from the DTMROC coincide in time. However, the situation is radically different in the real LHC operation environment, with data acquisition rates of the order of 100 kHz. In such situation, output to input feedback can take place, *e.g.* through the test pulse lines that run from the DTMROC to the inputs of the ASDBLR (Figure 16).⁹

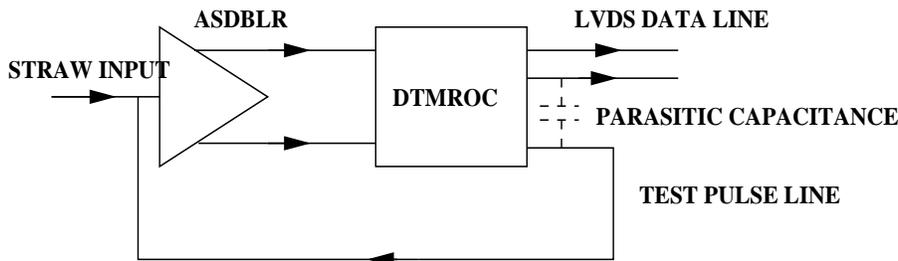


Figure 16: Cartoon depiction of output to input feedback through test pulse lines. The DTMROC provides two test pulse lines directly to the odd and even channels of the ASDBLR, respectively. Activity in nearby lines like the Low Voltage Differential Signal lines of the DTMROC data out can induce noise in the test pulse lines, and therefore in the inputs of the ASDBLR.

To measure the 300kHz threshold noise rate in the worst of the cases, when the event acquired by the ASDBLR coincides in time with the data of the previous event read out from the DTMROC, and therefore when we have the highest level of electrical activity on the board, the following setup up has been implemented (Figure 17). The TTC is programmed by software to send out a test pulse signal through the front end panel. This test pulse signal is sent to a Lecroy 9211 pulser, where two TTL compatible pulses are generated. These two pulses are sent back to the TTC to produce two L1A triggers, and two events are acquired. The time interval between the two L1A triggers has to be chosen in such a way that when the second L1A trigger is received by the DTMROC, the event that was acquired by the ASDBLR when the first event was read out is present at the last cell of the pipeline. The second event is acquired during the readout of the first, while the data lines for each DTMROC on the board are active, sending out the data required by the first L1A trigger. This time interval can be computed or measured. To do the latter, a wire coming from the data output lines at the termination resistors on the board can be attached to the input of the ASDBLR with an appropriate resistor and capacitor for a convenient shaping.¹⁰ In such way, a signal can be detected when the data is read out. Figure 18 shows a threshold scan for the first event and the data read out event when the data out lines are connected to the input of the ASDBLR.

⁹This has been a major design issue, and special care has been taken in isolating the test pulse traces in the board from data out lines.

¹⁰The ASDBLR integrates only the first 7.5 ns of signal.

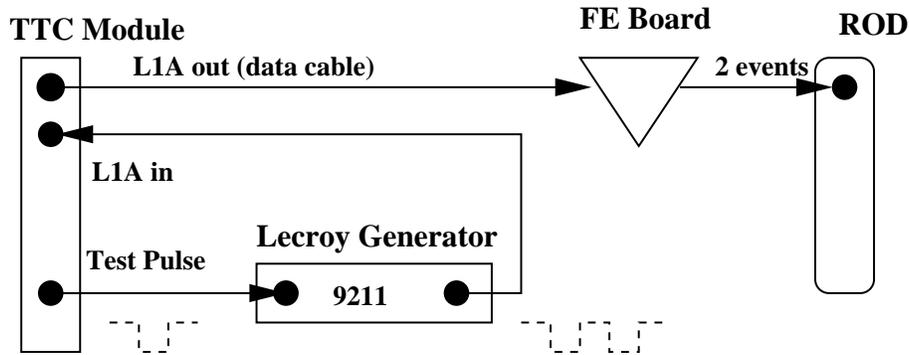


Figure 17: Cartoon depiction of the setup used for the data readout noise measurement. Through software and through the front panel test pulse lemo connectors of the TTC, a TTL signal is sent to a Lecroy pulse generator where two TTL pulse with an appropriate delay are generated. These two pulses are directed to the external L1A input connector of the TTC that delivers two L1A triggers to the board.

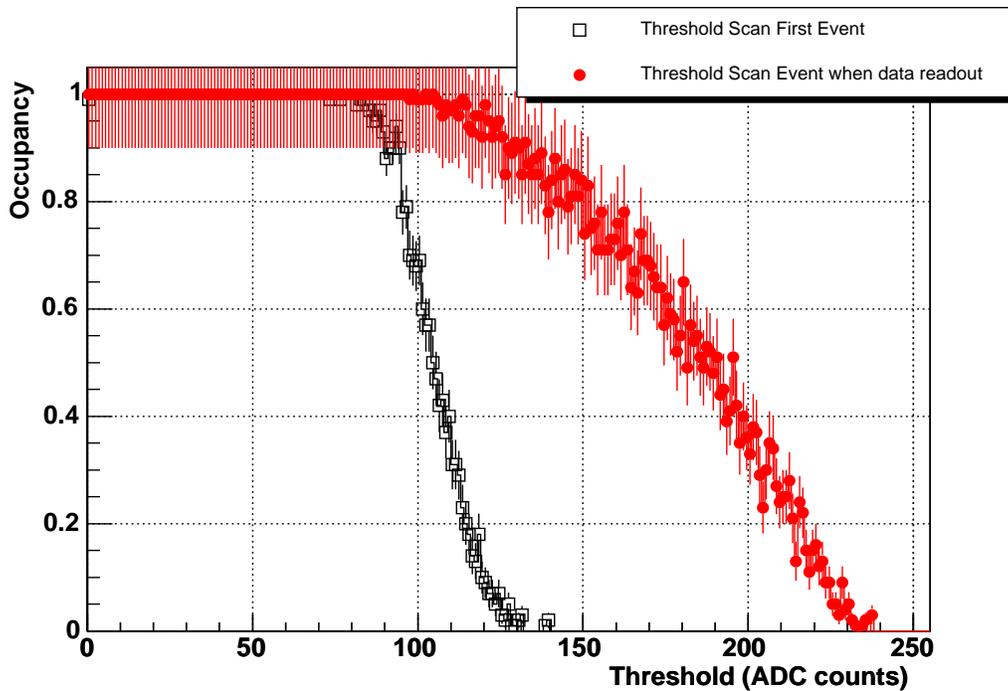


Figure 18: Threshold scan for the data readout noise. Threshold scan for the first event (open squares) and for the event synchronous with the data readout of the first one (red solid circles). In this case charge was injected with a wire to the input of the ASDBLR directly from the termination resistor of the data out line.

6 Performance Tests

The latest version¹¹ of the 1BS and 1BL boards were tested at CERN and UPenn with the setup described in the previous Sections. The aim of the tests was to characterize the noise performance of the boards, as well as check the consistency of the measurements performed at two different locations with somewhat different setups and environments. The measurements performed were:

- 300 kHz noise rate thresholds, with the boards plugged and unplugged to the module, in different modules (at CERN) and with or without the cooling plate.
- Clock Noise pickup in the same conditions
- Data read out noise and noise measurements.

6.1 Thresholds for 300 kHz Noise Rate and Clock Pickup

Figure 19 shows the 300 kHz noise rate thresholds for all the channels of the 1BS and 1BL boards, respectively. Noise thresholds are pretty uniform across the different DTMROCs, with values around 110 DAC counts for 1BL and 100 DAC counts for the 1BS, that are 50% efficient for 200 and 250 eV electrons, respectively (see Section 5), well within specifications. Notice that for 1BL positions 10 and 11 have somewhat lower 300 kHz noise rate thresholds, while for 1BS positions 2 to 7 are the ones with somewhat lower thresholds. This is understood as due to the length of the straws, since for these positions the straw wires are significantly shorter, and therefore the reduced attached capacitance decreases the noise. Several channels on position 6 of the 1BL board also show reduced noise thresholds at the UPenn setup. These channels are not connected by design to any straw.

Figure 20 shows the clock noise pickup for 1BL and 1BS at the CERN and UPenn setup, respectively. The clock noise is pretty uniform across the different positions and is typically at the level of 10 DAC counts. Preliminary measurements to be reported in a future note show that such clock noise levels do not affect the time resolution for identifying low threshold hits from ionizing particles.

Figure 21 shows the 300 kHz noise rate when the 1BS board is plugged separately into two different modules at CERN. As we can observe, the difference between modules is negligible. (Note that position 4 shows lower noise rates in one module. This is due to the fact that that position was not connected to the straws in that module in this particular measurement).

Figure 21 also shows the 300 kHz noise rate for the 1BS board with and without the cooling plate. The cooling plate is a thin metal plate attached to the top of the DTMROCs. In the present setup the cooling plate has been left floating, since a slight increase of the noise is observed when it is attached to the digital ground. As Figure 21

¹¹As December 2003

shows, when the cooling plate is left floating, it has no effect on the noise performance of the board.

6.2 Noise Measurements and Data Read Out Pickup

Figure 22 shows the noise pickup for the 1BS board for all the positions. The noise is quite uniform for all the positions, with typical values of 10 DAC counts, corresponding to approximately 0.3 fC. As in the case of the 300 kHz noise rate thresholds, positions with larger straws have increased noise. This circumstance is clearly seen in Figure 24, where for the 1BL board, the shorter straws, which are near the apex show a lower noise level.

Figure 23 shows the data read out noise for a channel of one 1BS board attached to the module. No significant noise behavior was found for any channel on either board.

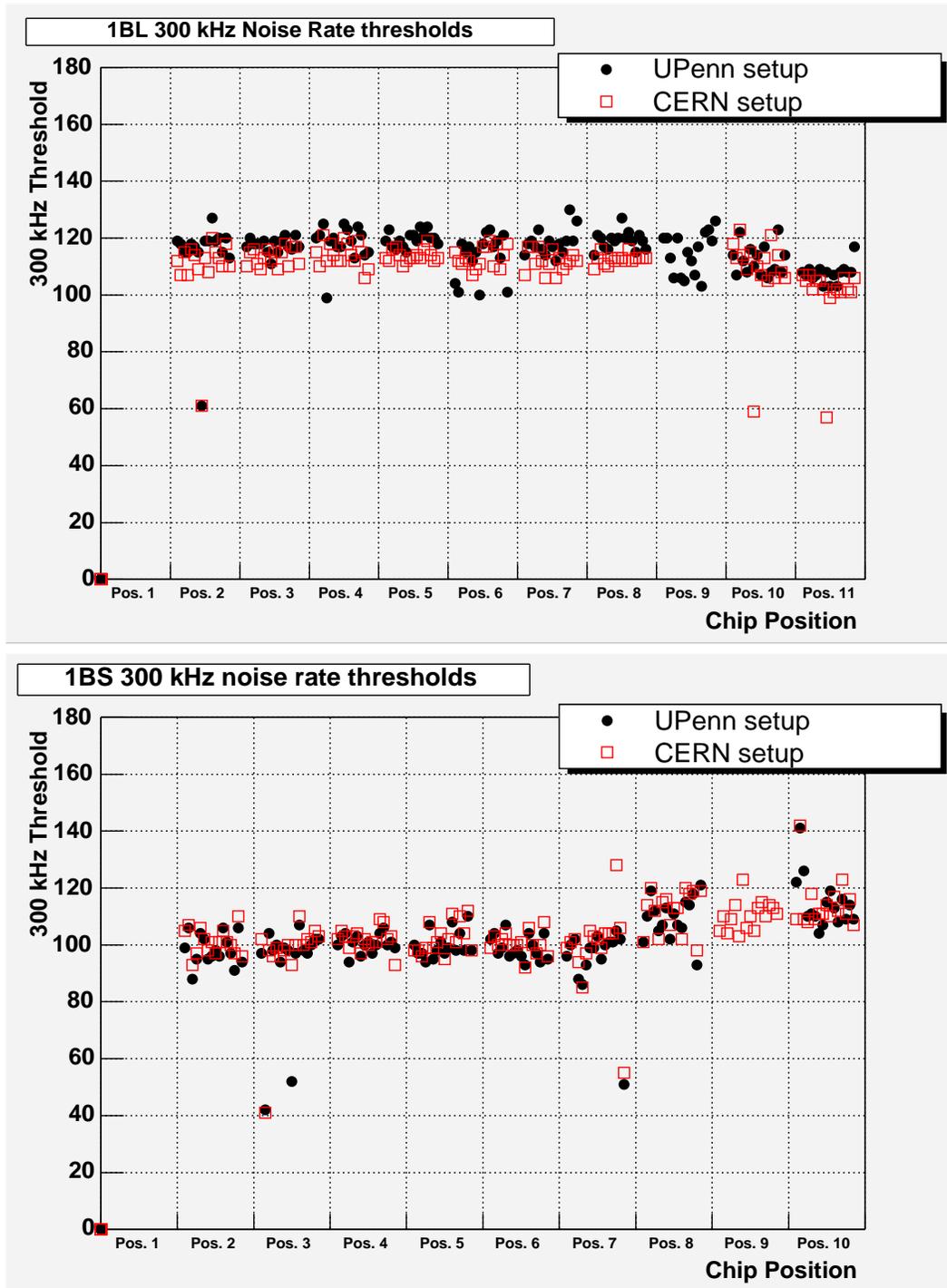


Figure 19: 300 kHz noise rate threshold for the 1BL (top Figure) and 1BS boards (bottom Figure) at the CERN setup (open red squares) and the UPenn setup (black solid circles). In both cases the cooling plate was not attached. Looking at the board from the DTMROC side, with the base of the isosceles triangle facing downwards, position 1 corresponds to the first bottom left DTMROC. Then the enumeration snakes upwards to the apex.

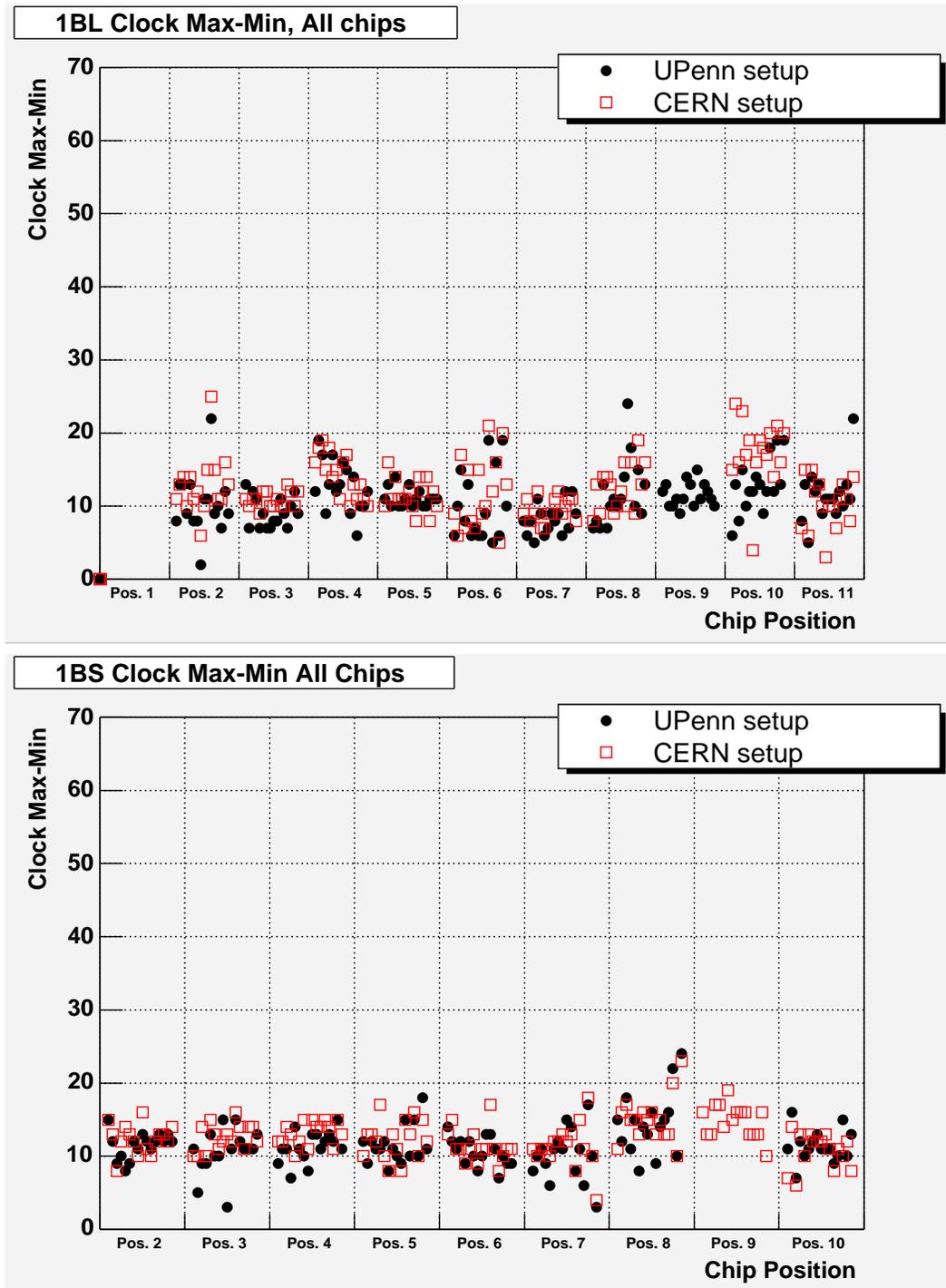


Figure 20: Clock noise pickup for the 1BL (top Figure) and 1BS boards (bottom Figure) at the CERN setup (open red squares) and the UPenn setup (black solid circles). In both cases the cooling plate was not attached. Looking at the board from the DTMROC side, with the base of the isosceles triangle facing downwards, position 1 corresponds to the first bottom left DTMROC. Then the enumeration snakes upwards to the apex.

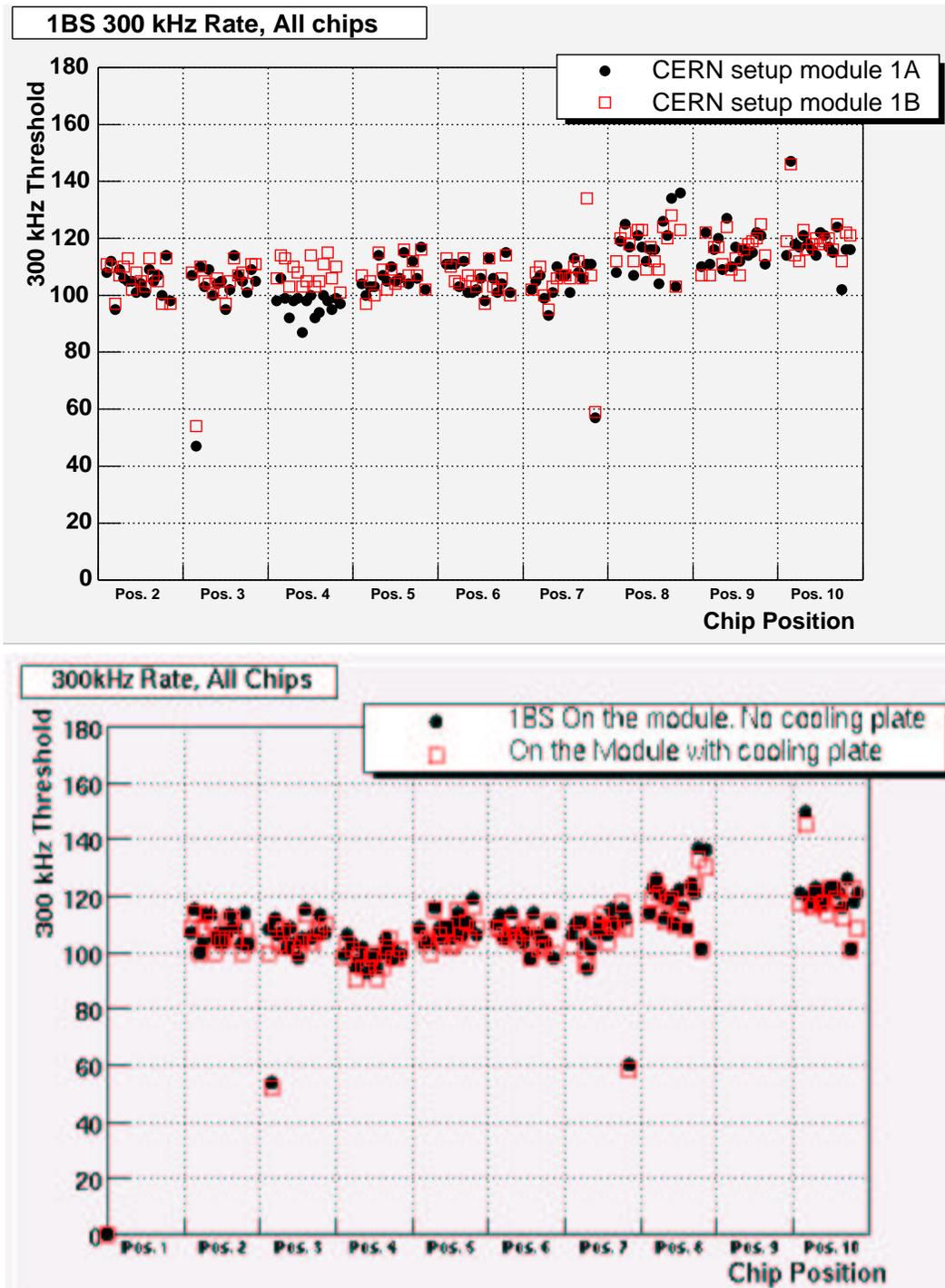


Figure 21: 300 kHz noise rate thresholds for the 1BS board at different modules (top Figure) and with or without cooling plate attached (bottom Figure).

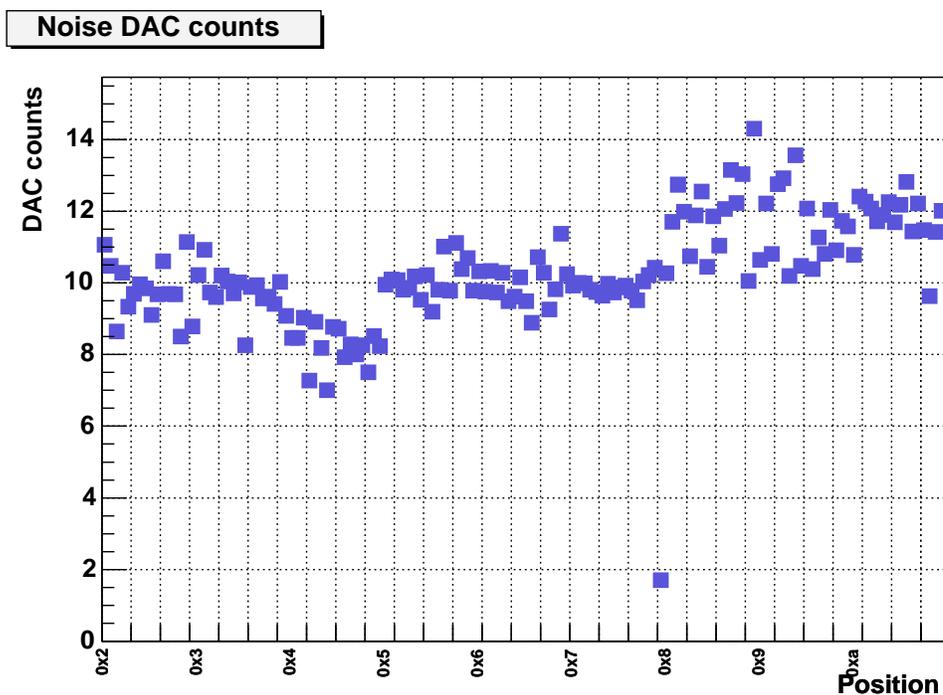


Figure 22: Noise level in DAC counts for all the channels of the 1BS board.

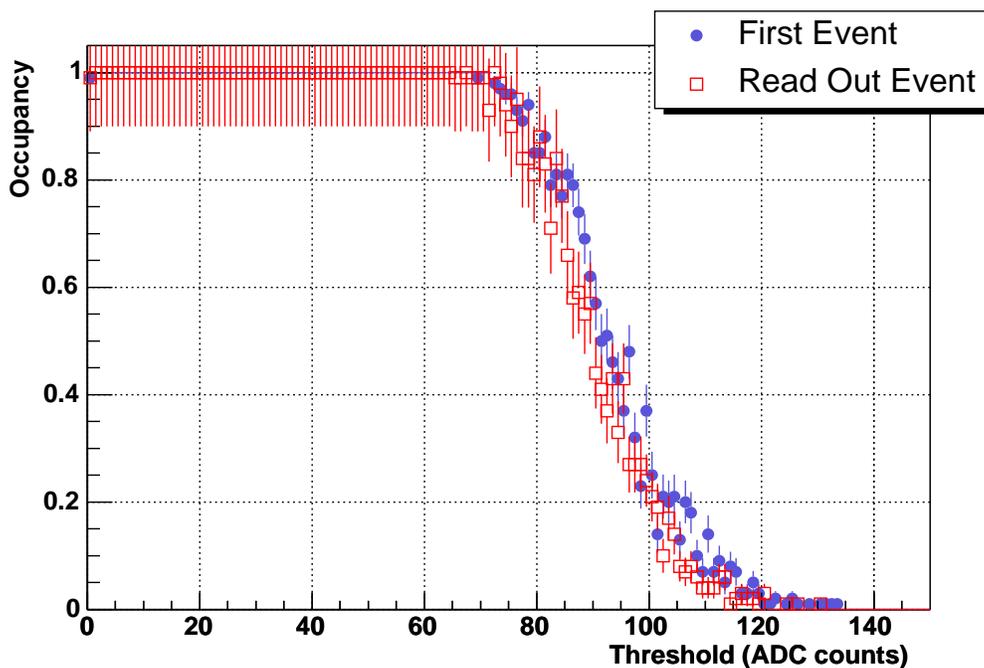


Figure 23: Data readout noise for one 1BS board attached to the module. Blue solid dots represent the threshold scan for the first event. Red open squares represent the threshold scan for the second event, acquired when the first one is read out.

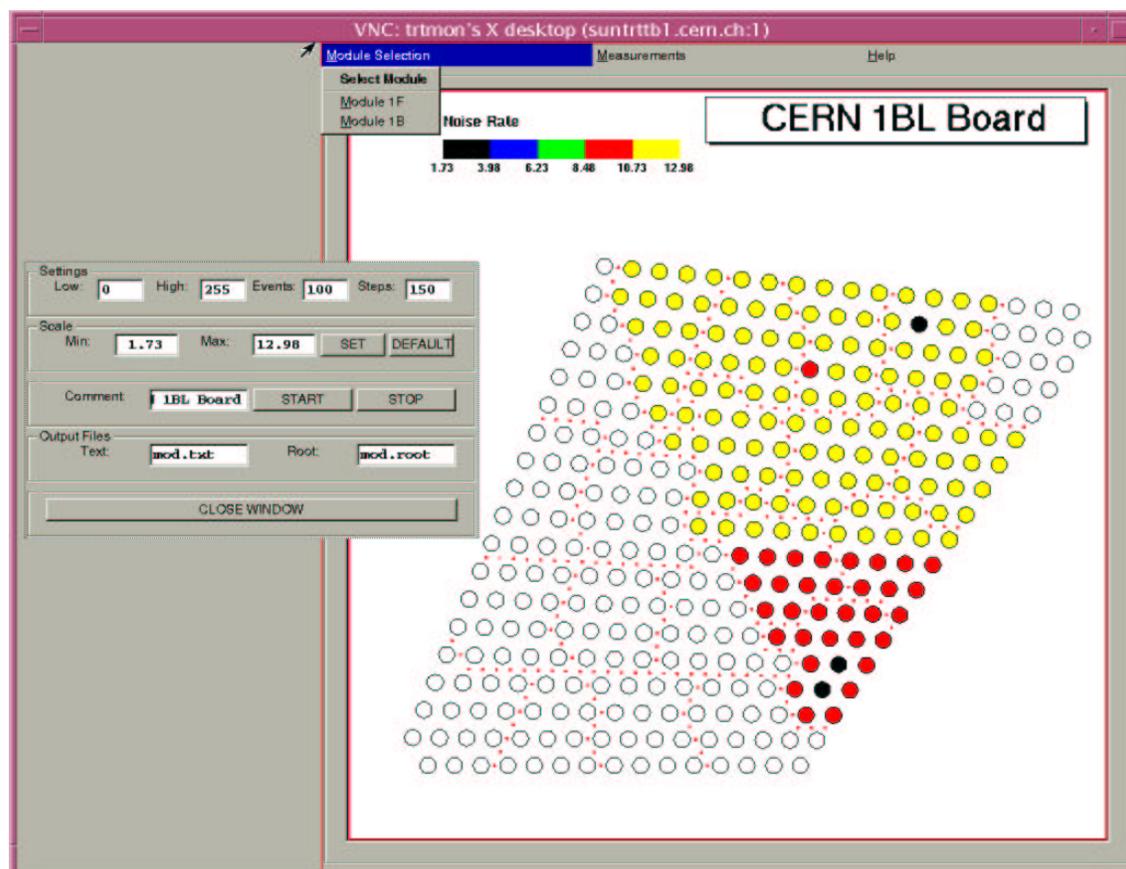


Figure 24: Geometric display of the 1BL board. The color scale correspond to the noise levels in DAC counts.

7 Module to Module Interference

At the CERN setup, two Type 1 modules were installed. We tested that the noise behavior of the boards was not affected by the boards that were attached to the other end of the module. This was tested by simply switching the boards on the other side on/off, with a completely negligible effect on the 1BS and 1BL boards under study. However, the situation was different when we switched on/off the boards that were plugged not into the other end of the same module, but into the other end of a neighboring Type 1 module (Figure 25). For certain locations, a high increase of the noise was observed. As shown in Figure 25, the increase in noise was mainly due to clock-pick up noise. However, it must be noted that the boards on the opposite side belong to a previous design version, with a worse attachment of the analog ground to the space frame. By improving this attachment, a better performance was achieved (Figure 26), although some channels retained with a higher noise. This sensitivity is currently under study in a multi-module environment and results will be reported in a future note.

8 Conclusions

Close to final prototypes of the 1BS and 1BL barrel front end boards have been tested with a barrel sector prototype at CERN, and with a single module prototype at the University of Pennsylvania. The measurements are in completely agreement in both setups and show that the noise performance of the boards is completely satisfactory, with noise occupancy levels of $\approx 2\%$ for 50% thresholds for 200, 250 eV electrons, well within specifications. However, noise sensitivities due to module to module interference had been observed and deserve further studies, concerning the grounding and shielding schemes.

9 Acknowledgments

We would like to thank Prof. Brig Williams and Rick VanBerg (University of Pennsylvania, USA) for their frequent discussions and insightful comments and questions. Mr Rick VanBerg had the original idea of the barrel front end board as a single analog-digital board, and pushed the design through, against all odds and difficulties. Thanks to Bjorn Lundberg (Lund University, Sweden) and Nandor Dressnandt (University of Pennsylvania) for their explanations about the boards' technical design. They designed the different prototypes of the boards and implemented successive modifications that continuously enhanced their performance. The DAQ software developed for the measurements presented in this note was built upon a previous version from Paul Keener (University of Pennsylvania), who was always willing to assist us. Godwin Mayers (University of Pennsylvania) made use of his artistic gifts to assemble for us these complicated boards with extreme reliability and speed.

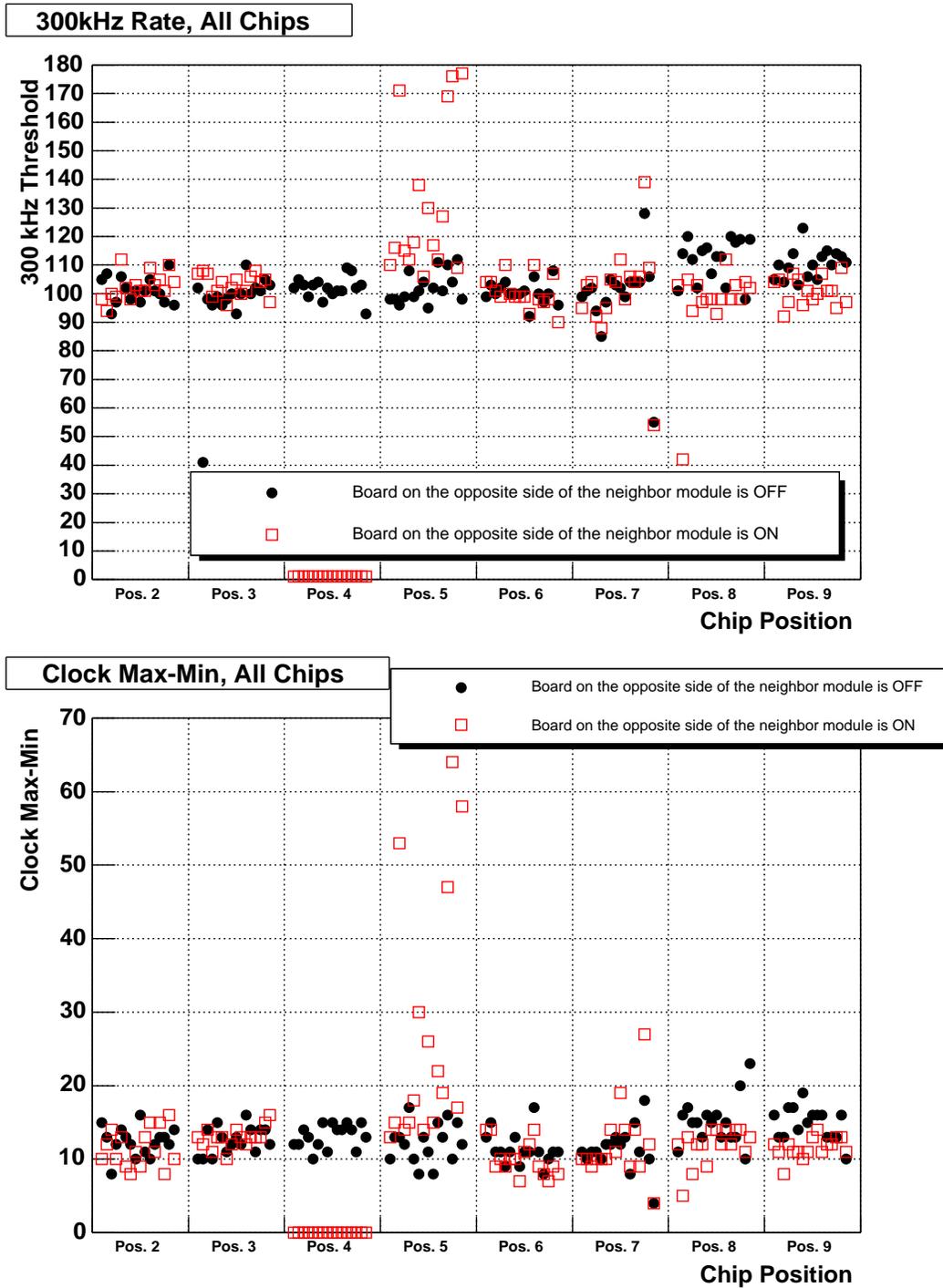


Figure 25: 300 kHz noise rate (top Figure) and clock pick-up noise (bottom Figure) for one 1BS board when the 1FL board on the opposite side of the neighboring module is *off* (black solid circles) and *on* (open red squares). Position 4 was taken out of the read out chain.

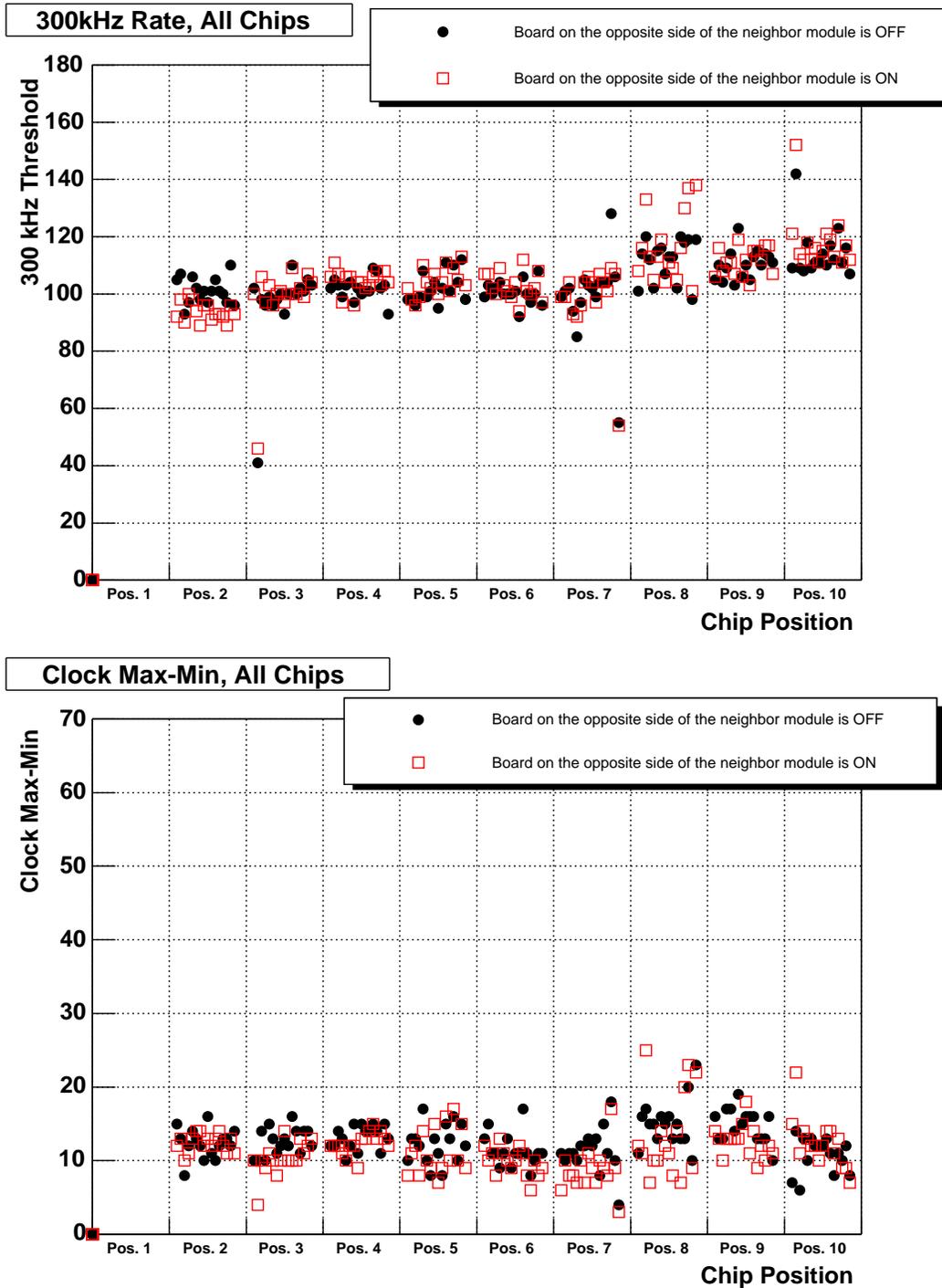


Figure 26: 300 kHz noise rate (top Figure) and clock pick-up noise (bottom Figure) for one 1BS board when the 1FL board on the opposite side of the neighboring module is *off* (black solid circles) and *on* (open red squares). In both cases the attachment of the 1FL analog ground to the space frame was improved.

10 APPENDIX

TRT barrel electronics are located in a very narrow region at each of the barrel modules, where cables, electronics, cooling pipes and plates, the support frame, cooling and module gas lines are allocated approximately 25 mm along the direction of the beam. The readout density is $1/30$ wire/ mm^2 , twice that of the end-cap wheels.

The first prototype for the readout triplets¹² was the stamp board design (Figure 27). It consisted of two stamp boards connected with Kapton. In one board the DTMROC in TQFP packages was placed in one side, with an output to the wires connector in the other side. The other stamp board hosted the two wire bonded ASDBLRs on one side, and the input straw wire connectors on the other side. This design had the advantage of an unique design for all the different triplets regardless of their position. To connect the triplets, a *snake cable* was designed to be plugged into the output connector of the DTMROC stamp board (Figure 28). This design was abandoned due to the very low manufacturing yields, as well as the poor isolation from the digital lines resulting in very high noise levels. As posterior investigations showed, the reduced space available in the board does not allow for the creation of large ground planes that serves as effective shielding against the digital noise. Another concern was the low yield of manufacturing the *snake cable*, as well as design issues like the achievement of uniform power distribution to the DTMROCs due to its connection in series.

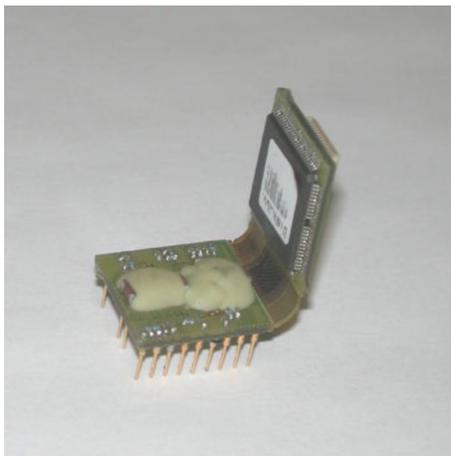


Figure 27: Stamp flex board. In the upper board one DTMROC in TQFP package is shown. In the bottom board, two ASDBLRs with protective pot are shown.

The next iteration consisted of the design of two and three stack boards by a joint effort of Lund University and University of Pennsylvania (Figure 29), and the use of custom fine pitch ball grid arrays for the packaging of both the DTMROC and the ASDBLR (Figure 30). In this design, the Kapton connection between the DTMROC

¹²The basic readout unit is a triplet consisting of two ASDBLR chips of 8 channels, connected to one DTMROC chip[3].

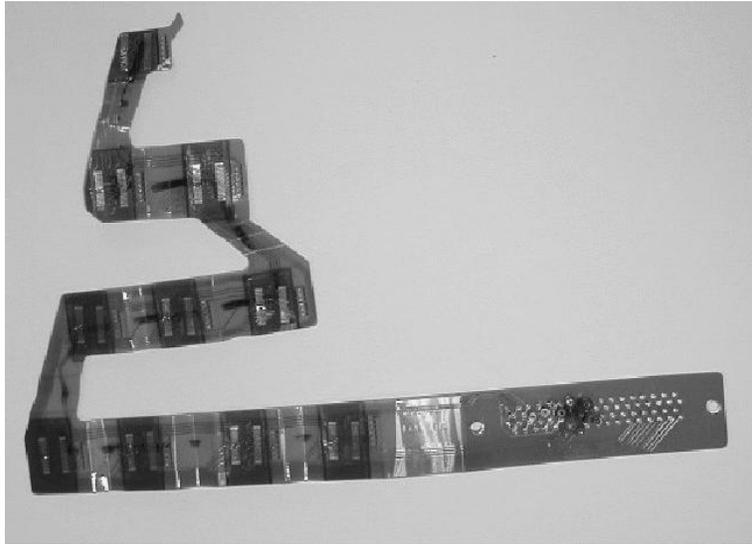


Figure 28: *Snake* cable for the connection of the stamp flex boards.

board and the ASDBLR board was abandoned in favor of conventional connectors. Two designs were pursued. One where the DTMROC and the ASDBLR were hosted on two different boards (the three stack board) and other design where both the DTMROC and the ASDBLR were hosted in the same board (the two stack board). The two stack design presented a very large noise problem due to the interaction of the digital with the analog side, while the reduced area of the board offered minimal options for the shielding and rerouting of the more sensitive parts. The three stack version also presented important noise problems, with the added concern of the design of an effective cooling system for the board hosting the ASDBLRs.

All these designs were abandoned in favor of a single digital and analog board approach (see Figure 6 Section 3), where due to the different mechanical geometry of the different TRT modules, up to 12 different boards should be designed.

The single board approach allowed for the implementation of the following design principles:

- The extended surface of the board allowed the implementation of extended ground planes to isolate the analog and digital domains (Figure 31). At the same time, its thickness allowed them to be isolated vertically, reducing the capacitive coupling between the analog and digital power planes.
- The analog ground plane could be extended horizontally to cover almost all the surface of the board, and at the borders extended vertically with an edge plate to enclose all the analog part of the board (Figure 32). The implementation of such edge plating allows us to connect the analog ground to the space frame of the module. This design rule was motivated because from early stages of the front-end board design, it was observed that external currents induced by the bouncing of the DTMROC power ground and other sources coupled to the signal

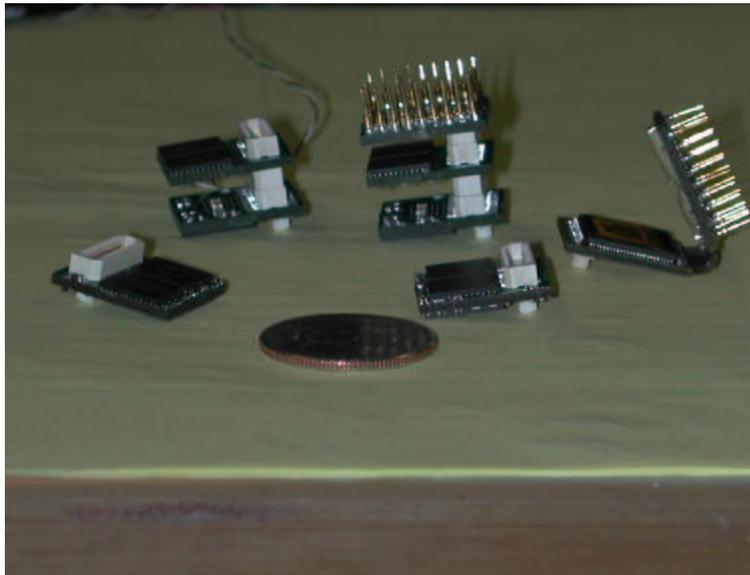


Figure 29: Different prototypes of stack boards for the hosting of one DTMROC and two ASDBLR chips. From left to right: one two stack board, one three stack board, one three stack board with the protection input board to the straw wires attached, one two stack board and one stamp flex board.

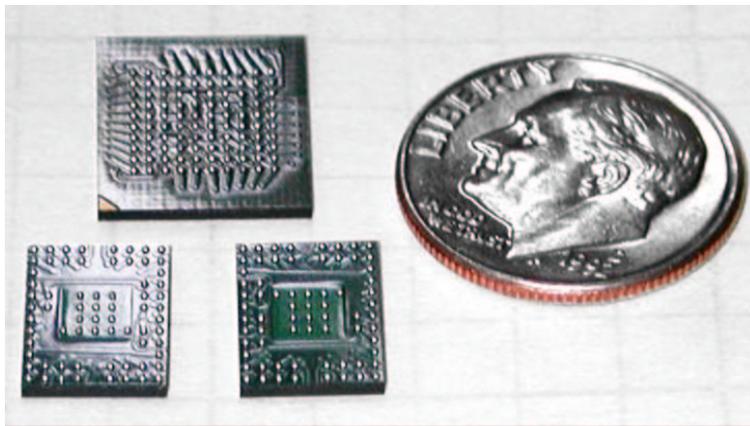


Figure 30: Custom Fine Pitch Ball Grid Arrays packages for the DTMROC, (upper package), and the ASDBLR (bottom package). The dimension for the DTMROC package is 11×13 mm, and for the ASDBLR 7.2×9.6 mm.

return path (see Section 4), were greatly deteriorating the noise performance (Figure 33). It must be noted that after the analog ground edge plating was implemented, the sensitivity of the noise to the quality of the connections between the analog ground and the space frame was greatly reduced. However, it still plays a significant role in reducing the noise.

- The extended surface of the board allowed a careful routing of power distribution and the most sensitive data lines, like *e.g.* the test pulse lines. The DTMROC

provides two test pulse lines ([3]) directly connected to the inputs of the ASDBLR chip. Special care was taken to isolated those lines from high activity lines like clock lines, data output lines, *etc.*. One sensitive issue was the location of vertical vias carrying digital clock signals. It was discovered that when such vias where located on the top of input traces, an unacceptable synchronous clock noise was observed (Figure33). The multilayer structure and the available space allowed us to avoid such effects.

- The analog and digital ground could be kept separated, connected by a great number of resistors located everywhere in the board. This allowed us to have control of the current flow by a careful choice of the resistors' value.

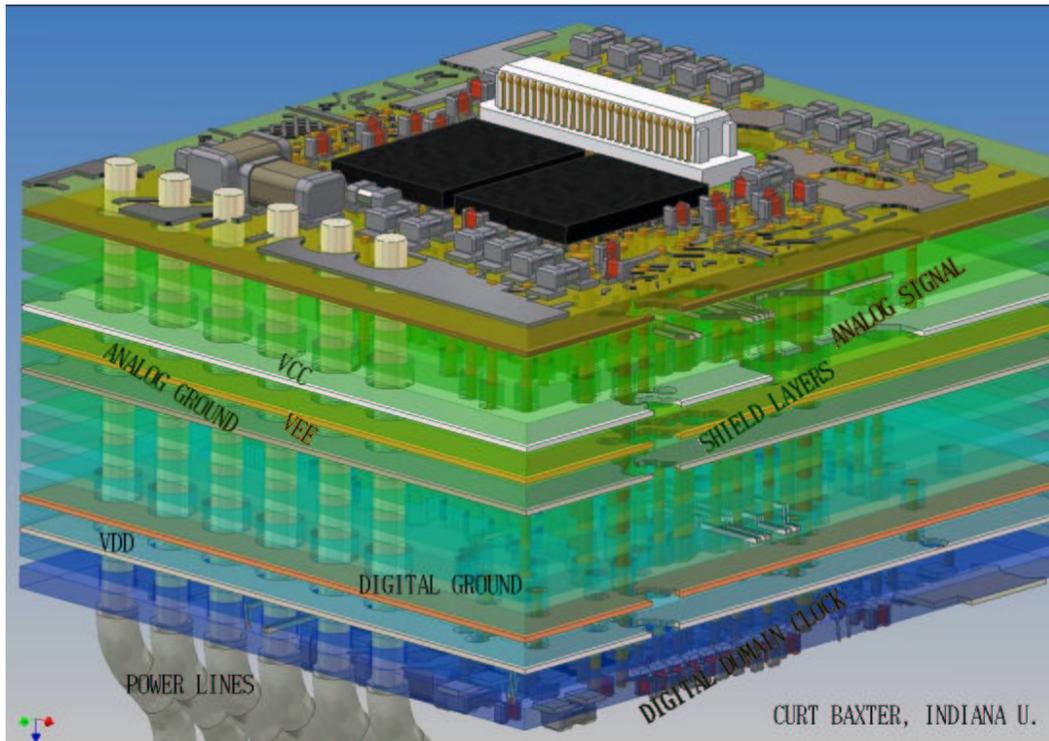


Figure 31: Sliced view of a barrel board. On the top, two ASDBLRs with their corresponding input connector are shown. (Courtesy of Curt Baxter, Indiana University.)

Figure 34 shows a typical layer distribution for a barrel front-end board.

Estimation of the DTMROC V_{dd} filter capacitance

The DTMROC is a 40 MHz clocked device (Figure 35), with a measured per chip current ranging from 1.1 A when the clock is *on*, down to 0.89 A when the clock is *off*. Such bouncing should be locally filtered in order to avoid oscillations on the level of the digital ground that can propagate to the analog ground. The design of the barrel board as an extended single board allows to locate a great number of decoupling capacitors

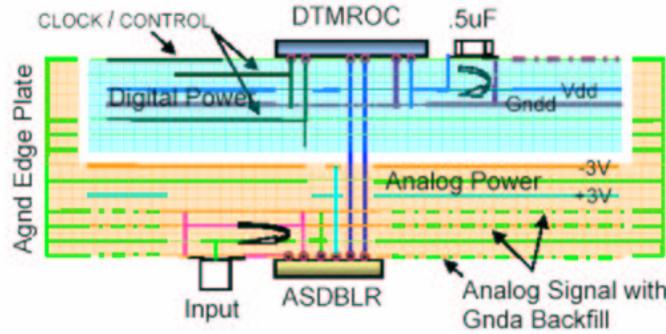


Figure 32: Transverse scheme of a barrel board. One DTMROC and one of the underlying ASDBLRs are shown.

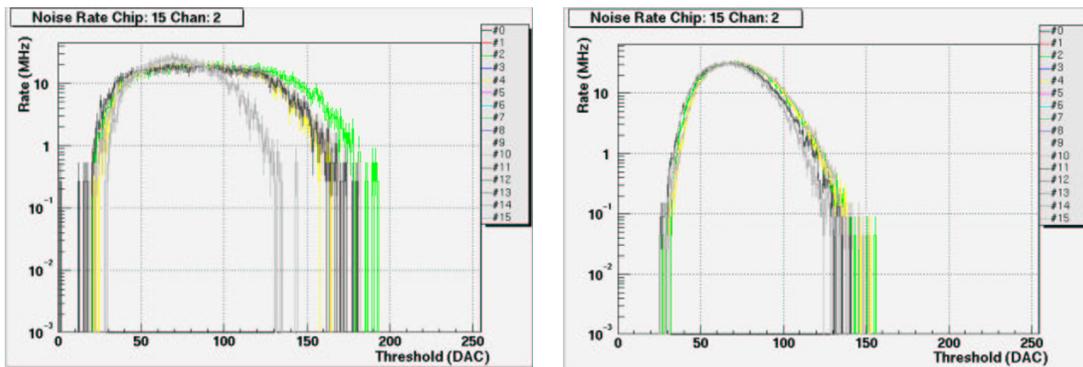


Figure 33: Noise rate curve for an early version of a 2FS board when the analog ground is not attached to the space frame (left Figure) and when it is attached to the space frame by means of copper tape (right Figure, see also Figure 9 in Section 4).

near each DTMROC. Figure 36 shows the improvement achieved in the bouncing of the digital ground by passing from 2 to 6 $0.2\mu F$ decoupling capacitors in one DTMROC location.

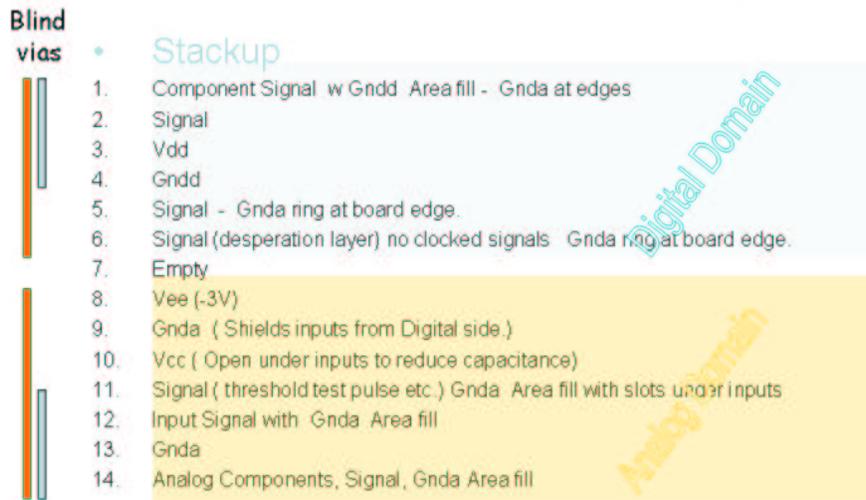


Figure 34: Layer scheme of a barrel board.

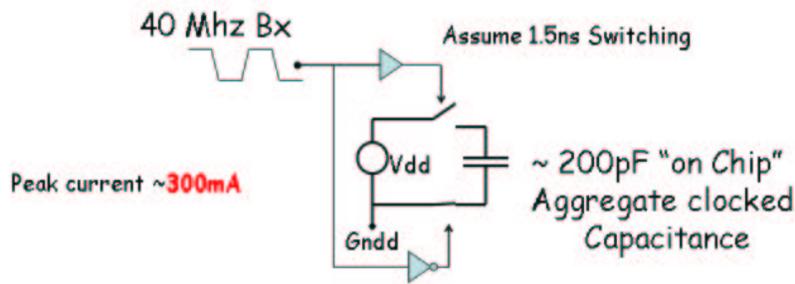


Figure 35: DTMROC chip clocking current model.

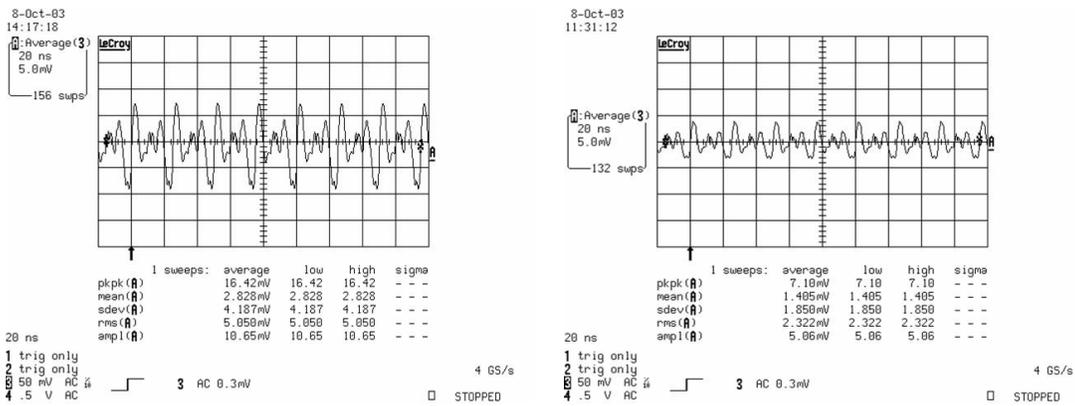


Figure 36: Oscilloscope screen shot of the voltage at the digital ground plane, when only 2 0.2μF decoupling capacitors are near the DTMROC chip (left Figure), and with 6 decoupling capacitors. The peak to peak value goes down from 17 mV to 7 mV.

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