PULSAR/Computer Interface Plans

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10 October 2003
October PULSAR Meeting
Original Goal

• Demonstration of data flow
  – L2 primitive data from PULSAR to PC and back to PULSAR

• “Sufficiently fast”
  – Transfer < 10µs ?

• Took on algorithm issues as well
  – Transfer+Algos: 15 – 20µs ?
Basic Architecture
4 CPU / Box
4 Boxes
Preferred Architecture

• 4 Box, 2 CPU per Box
  – Run 4 copies of the same system
  – Fixed L2 buffer / Box mapping?

• Pros
  – Maximizes available link bandwidth
  – Minimizes process interference
    • Maximizes available CPU cycles
  – Easier spares scenario
  – Overall simpler architecture
Preferred Architecture (2)

• Cons
  – Need to coordinate 4 boxes
  – Need 2 “output” PULSARs
  – Need 4 input channels for trigger bits
  – Need to sequence trigger decisions
    • To do in PULSAR
Lots to Worry About

• User friendly Start / Stop algo code
• User friendly / fast tagset selection
• Error recovery
  – Code crash
  – Machine crash
  – …
• OS configuration
• Control network design
Lots to Worry About (2)

- Statistics collection
  - L2 prescale
  - General bookkeeping
- Monitoring
- Rate limiting trigger implementation
- Implications on PULSAR firmware
  - L2 primitive steering to CPUs, etc.
- ...
Next Steps

- **4th Quarter 2003**
  - Work with Yale on simulation of L2 processing
  - Prototype control mechanisms
  - Investigate DAQ interface

- **1st Quarter 2004**
  - Fix architecture
  - Implement DAQ interface
  - Finalize control mechanisms