ATLAS Detector Upgrade
focus on Inner Detector

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for the
HEP Instrumentation Group
HEP Instrumentation Group

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Nandor Dressnandt, Paul Keener, Walt Kononenko, Godwin Mayers, Mitch Newcomer, Mike Reilly and Invaluable student help

With this group we have the good fortune to be able to play a meaningful lead role in several parts of the ATLAS UpGrade
This Talk

• Will be somewhat reductionist in starting with Silicon and emerging with an ATLAS Upgrade.
• Will not defend the upgrade based on expected Physics.
• Will assume some Unfamiliarity with the baseline ATLAS detector and will review the Inner tracker systems.
• Will describe the Novel Next Gen tracking sensors at the end.

• One hope is to encourage additional interest from within the department in Upgrade Activities especially Novel sensors that may play an important role in future detector systems either at ATLAS or some future detector.
ATLAS Detector at LHC

• Designed for Luminosity of $10^{34} \text{ p/cm}^2/\text{s}$

• In the first 5 years 700 fb$^{-1}$* Integrated Luminosity
  – Most sensors in the inner tracker have occupancies of up to several percent @ design luminosity. TRT occupancies are highest.

• First Colliding Beams  Spring/Summer 2009

* SLHC Upgrade Plans envision 3000 fb$^{-1}$
With first LHC collisions set to occur in 2009 why consider a super LHC ATLAS detector now?

Designing and building the ATLAS detector was a daunting task. It is one of the most complex instruments built by people.

\[ \text{Concept to Reality has taken } \sim 15\text{ years} \]

• By starting now we can take advantage of experienced designers battle hardened by the realities of producing a working detector system.

• Higher luminosity will occur in stages at LHC. A new Linac will increase the Available beam current, possibly by 2014. A better focusing scheme will intensify the concentration of protons in the interaction point and a tightening of the length of proton bunches is expected to increase the luminosity to \( 10^{35} \) by 2017.

• Even at the proposed Luminosity of \( 10^{34} \text{ p/cm}^2/\text{s} \) sub-systems within the detector will need replacement in the first few years of LHC operation.

• An obvious strategy is to focus contributions on systems with the highest priority for replacement as beam luminosity evolves upwards.
Silicon Tracking Detectors

- Ionization Energy 3.6eV
- 390 eV/um
- Gain ~1
- Typical Signal 30,000e
- Charge Collection time ~30ns
- Charge Collection node shape determines tracking coordinate precision.

Pixels ~ 50um X 400um
Strips ~ 50um X 10cm
The ATLAS Pixel Detector
Each ASIC 2800 ch

Pixel Sensor and RO 2800 channel Prototype ~ 2002
Barrel  67 million Pixels  13 million pixels Discs

6.5KW power @2V
10% Radiation Length Material
Useful to an Exposure of 50MRad
The Silicon Strip Tracker (SCT)

SCT detectors are AC-coupled, single-sided strip detectors based on p+ strip implants in an n-type silicon bulk. The strips are biased through polysilicon or implant resistors from a common bias line which surrounds all strips on a wafer. The detector edge and guard ring design varies depending on the manufacturer. Due to radiation induced changes of the bulk effective doping concentration, we require the detectors (and all related components on hybrid and supply system) to operate reliably up to 500 V. After irradiation we expect an operation voltage of approximately 350 V with the measured pre-irradiation values for the full depletion voltage typically in the range of 60–80 V.

ATLAS irradiation studies of n-in-n and p-in-n silicon microstrip detectors, P. Allport et.al. NIM A435 (1999)
SCT barrel module

Four silicon strip detectors, reverse biased p+ - n. 6 x 6 cm, 285μm thick

768 silicon strips, 80 μm pitch

Strip Alignment

Ola Kristoffer Øye – University of Bergen
Silicon Strip Detector  Barrel and (Partial) End Caps
6.3 million Strips  50um X 6 and 12 cm
61m²  Active Silicon  4.5mW per channel
Dressing Cables
For the SCT Barrel
The Transition Radiation Detector
TRT Barrel Detector
52K axially aligned 1.6M straws
Split anode wires.
104K Wire Readouts
@ LHC Design Luminosity operation
Inner Layers up to 20% occupancy
Outer Layers a few %
130µm RMS R – φ information
TRT End Cap Wheels
240K Straws Placed Radially outwards

Readout Electronics
Jack Fowler, Duke
Wiring the TRT
Pixel Detector & SCT
First Events

September 10, 2008
September 10, 2008 - A 'splash event' as ATLAS detects particles from nearby collisions from the first beams through the LHC
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Upgrades to The ATLAS Inner Detector

Goals for Upgrade

The goals for the Upgrade are:

1) Maintain at higher luminosity the same performance as the present ATLAS has at $10^{34}$ luminosity.

2) Allow collection of up to 6000 fb$^{-1}$ of data with good performance. This is nearly 10 times the data expected between 2009 and 2016, allowing a large increase in physics reach.

3) The resulting design, to be presented, works well in the range of $10^{34}$ to $10^{35}$ luminosity. Design is based on all silicon sensors.

Abe Seiden UCSC Report to Joint Oversight Group (JOG) 11/08
Detector robustness and performance have to fight for an higher than the today BL design luminosity ($2 \times 10^{34}$) at a smaller radius (3.7 cm instead 5.0 cm)
Items to Develop (R&D Program)

- Two types of pixel detectors:
  3-D detector for innermost layer (alternative diamond detector).
  n-on-p detector for 3 other layers (alternative is n-on-n detector).
- n-on-p short and long-strip detectors for the 5 strip layers.
- New front-end chips for these as well as associated controller and data collection chips. A major goal is to reduce power in the front-ends.
- New optical readout components (exploring several options for VCSELs and PIN diodes).
- New powering schemes (to power many modules per input power cable) to minimize mass in the detector and maintain safety for the chips.
- New mechanical scheme for holding individual sensors to reduce mass and complexity.
- New cooling system to improve on present detector (a possible choice is CO₂).

All items have been under development for the past few years and we plan to be ready for pre-production by June 2011.

Abe Seiden, UCSC JOG workshop 11/08
New All Silicon Tracker replaces current pixel, SCT and TRT:
- pixels,
- short strips (2.5cm)
- long strips (10cm)
SLHC predicted occupancy

Old assumptions - 230 events/BX...
(New estimates~400)

Few comments:
- At 4-6 cm pixels layer should be <300μ
- At 24 cm even short strips are have > 1% occupancy
- At 71 cm long strips have occupancy > 1%

Pavel Nevski  BNL
## SLHC Radiation Environment

### Radiation for 3000 fb⁻¹

Total Dose from Ionizing Particles

<table>
<thead>
<tr>
<th>Radius in cm</th>
<th>Det.</th>
<th>Dose in kGy</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.05</td>
<td>Pixel - 3d</td>
<td>15800</td>
</tr>
<tr>
<td>12.25</td>
<td>Pixel</td>
<td>2540</td>
</tr>
<tr>
<td>29.9</td>
<td>SCT SS</td>
<td>760</td>
</tr>
<tr>
<td>51.4</td>
<td>SCT SS</td>
<td>450</td>
</tr>
<tr>
<td>43.9</td>
<td>SCT SS</td>
<td>300</td>
</tr>
<tr>
<td>108</td>
<td>SCT LS</td>
<td>70</td>
</tr>
</tbody>
</table>

(158MRad)  (700KRad)

- Running up to 3000 fb⁻¹
  - Design for 6000 fb⁻¹
  - Should take about 6 years (?) † hadron rate for SEE
- Detector temperature ~-30°C (minimize damage to Silicon)
- Magnetic Field ~2T

Philippe Farthaout TWEPP 2008

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**Neutron 1MeV Equivalent Dose**

**NIEL**

**Inner tracker fluence predictions at the SLHC, using FLUKA2006.**
- Integrated luminosity of 3000 fb⁻¹
- av18 geometry (5cm moderator)
- No safety factors

Neutron 1MeV Equivalent Fluence:

- Z=300cm
- Z=150cm
- Z=0cm

Philippe Farthaout TWEPP 2008
Present ATLAS Pixel B-Layer

Innermost layer of the ATLAS Pixel Detector:

- Historically called B-layer. Sensor radius is 50mm, and layer consists of 22 carbon-carbon staves (11 evaporative cooling circuits), each supporting 13 modules:

- Total of 286 modules (16%) with 20 degree tilt angle, 13.2M channels, active area roughly 0.29 m², worst-case end-of-lifetime power load as high as 2.4kW.
- Features: two data fibers/module at 80Mbit/s each, all cooling connections on C-side (historical), operation to $10^{34}$ luminosity with 99% single hit efficiency.
- Staves are mounted inside carbon-fiber half-shells, which clamp to form the layer.
**B-Layer Replacement Concept:**

**Justification:** 300 fb\(^{-1}\) expected Life time

- With nominal luminosity profile, expect B-layer performance to start degrading after 2-3 years at LHC design luminosity or about 300 fb\(^{-1}\) (10\(^{15}\) NIEL dose, 50MRad ionizing dose). Expect reduced efficiency and modest reduction in point resolution.
- The performance of the B-Layer has a large impact on ATLAS physics performance, particularly for B-tagging. On the timescale of next several years, expect that improvements in technology should allow construction of a B-Layer with improved segmentation, greater radiation hardness, and reduced material.
- Propose to prepare an upgraded B-Layer for installation during the Winter 2012/2013 shutdown, after roughly 4 full years of ATLAS operation.

**Principal goals are:**

- **Reduction of material**, required to take full advantage of point resolution. This could use a combination of improved power distribution (reduced electrical services) and improved active fraction for the basic modules (closer to 90% rather than the present 71%). Present best estimate for pixel layer now is 2.5% X\(_0\) per layer. Would like to target between 1.5% X\(_0\) and 2.0% X\(_0\) per layer.

- **Improvement of segmentation**, useful to cope with higher occupancy and provide improved point resolution in one or both measurement coordinates. Ideally, would like to reduce pixel area by a factor 2-3. What is the optimal aspect ratio?

- **Increased radiation tolerance**, both for higher instantaneous luminosity and for higher total dose tolerance. Set nominal goal of a factor 3 increase, leading to instantaneous rate of 1x10\(^8\) cm\(^{-2}\)s\(^{-1}\), and a total dose of 3x10\(^{15}\) neutron equivalent. This is an intermediate step to SLHC, and would be consistent with operation at 30mm radius and the present LHC design luminosity up to SLHC (2016) period.
Projected U.S. Activities and Deliverables

Silicon Strips

- Leading role in the definition and implementation of the overall electronics architecture, including design contributions to specific elements. The definition of the overall electronics architecture (for strips and pixels) is currently being co-led by the U.S. (UCSC, Penn)

- Contribution to the procurement of front-end integrated circuits and local control integrated circuits. Testing of integrated circuits. This follows naturally from the role in defining the overall electronics architecture. (UCSC, Penn)

- Common design of powering and data transmission with the pixel detector, fabrication and test of unique elements of these systems. (UCSC, Ohio State, Oklahoma, Oklahoma State, SMU, SLAC)

- Development of planar sensors (in common in part with pixels), contribution to procurement costs and testing as part of a module assembly program in the U.S. (UCSC, BNL, Stony Brook, NYU, LBNL)

- Fabrication of a fraction of the local supports for silicon strip modules. The U.S. is currently leading the conceptual design of the preferred technique for holding, locating and cooling strip modules. Design and contribution to the global support structures. (Yale, BNL, LBNL)

- Mounting and testing of modules on local supports. It is essential that integrated structures be assembled world-wide and shipped to a central point (likely CERN) for final rapid integration into support structures to meet schedule constraints. (Yale, BNL, Stony Brook, NYU)

- Contributions to integration and installation at CERN. (BNL)
## Strips Detector in numbers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Radius [cm]</th>
<th>Phi segmentation</th>
<th>Number of modules per half single sided stave</th>
<th>Number of 128-ch FEIC per half single sided stave</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Short Strips</td>
<td>38</td>
<td>28</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>1</td>
<td>Short Strips</td>
<td>49</td>
<td>36</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>2</td>
<td>Short Strips</td>
<td>60</td>
<td>44</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>3</td>
<td>Long Strips</td>
<td>75</td>
<td>56</td>
<td>19</td>
<td>190</td>
</tr>
<tr>
<td>4</td>
<td>Long Strips</td>
<td>95</td>
<td>72</td>
<td>19</td>
<td>190</td>
</tr>
</tbody>
</table>

### Barrel

- **Total number of staves for the Barrel**: 236
- **Total number of modules for the Barrel**: 14,336
- **Total number of FEIC for the Barrel**: 270,080

### Endcap

- **Total number of staves for one End-cap**: 1,152
- **Total number of 128-ch FEIC for the two End-cap**: 57,088

### Total

- **Total number of 128-channel FEICs**: 327,168
- **Total amount of channels**: 41,877,504

- **Current SCT detector**
  - 4088 modules
  - 49k 128-channel FEIC
  - 6.3M channels

*Philippe Farthouat (CERN)*
Prototype Hybrid Realisation
November 2008

Unpopulated hybrid

Neighbouring ABCns wire bonded

Inter-chip bonding

From presentation by Ashley Grenall (Liverpool)
Inner Detector Upgrade Workshop

Flex thickness ~270 µm
Weight ≤2 g (unpopulated)

LVDS Repeater & Hybrid Power Card

ATLAS Upgrade

Hybrid Stuffed with Passives and 6 x ABCns

1280 Channel Module
First Generation Hybrid & ABCn first tests

What we presently know

- Hybrid connectivity confirmed to be ok
- Able to read back correctly thermistor temperature

- Wire bonded up single ABCn as a Master (M0), operating in Legacy mode
  - Disabled on-board Regulator + Shunt circuits (use external powering/regulation)
    - VDDD = 2.5 V, I = 110mA, VDDA = 2.2V I = 30mA (with clock supplied)
    - Specification is for a nominal of 96mA and 27mA!

- Clock feed through is enabled, default state for Masters on power-up
  - 40MHz clock is observed on Ldo outputs
  - Send command to disable Clock feed through - 40MHz clock goes away
    - Chip is responding to commands!
  - Send L1 trigger (toggle ABCn between data taking mode and Send_ID mode)
    - Observe No_Hit data packet and ABCn configuration data packet
    - ABCn responds to L1 triggers!

M0 Clock Feed Through

M73 response to L1 trigger
SCT Barrel Stave

A conceptual drawing of an SCT barrel stave. Details of powering, cabling control, monitoring and data collection are in early conceptual stages.
Prototypes and Designs

LBL

Stave-06

60 cm, 9 cm strip, 6 segments/side

1 meter, 3 cm strip, 30 segments/side
192 Watts (ABCD chip), ~2.4 % Xo + support structure

Stave-07

6 x 3 cm, 6 chips wide

Stave-08

1.2 meter, 2.5 cm strip, 48 segments/side ~250-300 Watts (@0.25 W/chip)
1.7 – 2.4 % Xo + support structure, depends upon coolant and hybrid design

Carl Haber   LBL

ATLAS Upgrade 10 x 10 cm, 10 chips wide
Serial powering of Staves

By powering each module in series a cable sized for a single module (2.5A). Can be used to minimize the material in the interaction area.

Features chain of 24 hybrids in series
Need to confirm we can do this
Alternative 2 * 12 in series
**DC to DC power distribution scheme**

With Efficient DC-DC conversion schemes, voltage and current can be traded off To lower power cable material required to supply detector mounted ASIC voltages.

10-12V

- **Conversion stage 1 (ratio 4-5.5)**
  - Vin=10V => high-V technology
  - Same ASIC development for analog and digital, only feedback resistive bridge is different

- **Conversion stage 2 (ratio 2)**
  - Embedded in controller or readout ASIC
  - Closely same converter for analog and digital (different current, hence different size of switching transistors): macros (IP blocks) in same technology

"analog bus" 2.5V

"digital bus" 1.8V

Controller ASIC

Readout ASICs
Module Data Rates

3.2 Gbits/s

160 Mbits/s

1.6 Gbits/s (20 * 80 Mbits/s)

8016 Mbits/s

800 Mbits/s

• Long strips and short strips are well balanced
  – 400 versus 380 FEIC

• Numbers without so much safety margin
  – Detector layout very likely to change

• Pixel will require more bandwidth

• Better design for more → x2

Philippe Farthouat (CERN)
Architecture

Although the data rates, radiation levels and first front end readouts have been identified, the overall architecture is not defined.

A *strip readout working group* has been formed and meets regularly to define an architecture that will enable designs to proceed.

Tradeoffs / Resources:

- Number and type of ASICs
- Command complexity vs hybrid real estate
- Redundancy vs hybrid real estate
- Data transfer protocol
- Data recovery techniques
Event size for a short strips module (40 128-channel FEICs). Current ATLAS SCT detector coding scheme

Mean size \(\sim 1600\) bits
## Fixed Length Data Transmission

<table>
<thead>
<tr>
<th>Fixed size packet for one non-empty ABCn</th>
<th>#bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>0</td>
</tr>
<tr>
<td>Chip ID</td>
<td>5</td>
</tr>
<tr>
<td>Data type</td>
<td>3</td>
</tr>
<tr>
<td>Sub-header</td>
<td>12</td>
</tr>
<tr>
<td>CRC</td>
<td>7</td>
</tr>
<tr>
<td>Payload</td>
<td>28</td>
</tr>
<tr>
<td>Stop</td>
<td>0</td>
</tr>
<tr>
<td>Total</td>
<td>55</td>
</tr>
</tbody>
</table>

- **Start**: No need
- **Chip ID**: Readout hybrid contains at most 20 chips
- **Data type**: Data, register readback, DCS, Test mode, ... Not more than 8 types
- **Sub-header**: Register address, DCS sub-type, etc and header for data. In the later, must contain BCID (8 to 12 bits) and L1ID (4 to 8 bits). Max length 12 - 20 bits
- **CRC**: 7 bits for protecting ChipID, Data type and sub-header (1 error recovery, 2 errors detection)
- **Payload**: Must be large enough so that most of events can totally fit in that space. If not, a second packet must be sent which has a large overhead. Simulations show a 21-hit average for 10 ABCn. Size of two isolated hits is 28 bits. Size for three is 42 bits
- **Stop**: No need

Many events with ‘0’ occupancy / ASIC see previous slide

‡ Only ASICS with data transmit.

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ATLAS Upgrade
One possible scheme

- The control of the transmission is very simple as the data are not analysed
  - Only number of bits transmitted is controlled
  - Packets from different events can be interleaved
- Note that we are not forced to have the data passing through all the chips; they could share a single bus FEICs‡ MC and only some arbitration mechanism is to be implemented
- Size of the Fifos optimised for keeping the level of data loss at the expected value
ASIC Technologies for the Upgrade

• What technology is most appropriate for a next generation detector.
  – Will it be available in 2014?
  – Will it offer acceptable low power operation?
  – Will it be affordable?
Overview of Technologies

- **CMOS 8RF-LM**: Low cost technology for Large Digital designs
- **CMOS 8RF-DM**: Low cost technology for Analog & RF designs
- **BiCMOS 8WL**: Cost effective technology for Low Power RF designs
- **BiCMOS 8HP**: High Performance technology for demanding RF designs
- **CMOS 9SF LP/RF**: High performance technology for dense designs

- 130 nm (CMOS and BiCMOS) and 90 nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.
CMOS8 RF Technology Tool Kit

Standard Features

- 130 nm lithography, twin-well on 1-2 Ω-cm non-epi P-substrate, low K dielectric
- Thin Oxide (22Å gate) FETs (1.2 /1.5V)
- Thin Oxide MOS Varactors
- Forward bias diodes
- N-well resistor
- 5 to 8 levels of metal
  - Thin and thick Cu metal (~0.3/0.55 μm)
  - Last metal options:
    LM: Cu 0.55μm   DM: 3 μm Cu + 4 μm Al
- Vertical Natural Capacitor
- Spiral inductors, RF Transmission lines
  - Series & Symmetrical inductors in DM wiring option only
- Electrically programmable fuses
- Wire bond or solder bump (C4) terminals

Optional Features

- Triple-well NFETs
- Thin Oxide Low power FETS
- Thin Oxide Low-Vt FETs
- Thick Oxide (52Å) 2.5V FETS
- Thick Oxide (52Å) 3.3V FETS
- Thin and thick Oxide Zero-Vt NFETs
- Thick Oxide MOS Varactors
- Hyperabrupt Varactor
- Polysilicon and diffused resistors
- TaN metal resistor
- Single and dual-layer MIM capacitor (DM option only)
Comparison of 250nm and 130nm Technologies

ABCN architecture in ¼ μm CMOS

![Diagram of ABCN architecture in ¼ μm CMOS]

250nm ABCn

<table>
<thead>
<tr>
<th>128 Channels / chip</th>
<th>VDD @ 2.5V</th>
<th>VDDA @ 2.2V</th>
<th>Current / chip</th>
<th>Power / chip</th>
<th>Power / module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analogue Supply</td>
<td>VDDA</td>
<td>27 mA</td>
<td>60 mW</td>
<td>1.2 W</td>
<td></td>
</tr>
<tr>
<td>Digital Supply*</td>
<td>VDD</td>
<td>92 mA</td>
<td>230 mW</td>
<td>4.6 W</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td><strong>290mW</strong></td>
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</table>

*SEU Tolerant Logic

Estimate for 130nm CMOS version

<table>
<thead>
<tr>
<th>130 nm Estimate</th>
<th>Supply</th>
<th>Short Strip Power, Current</th>
<th>Long Strip Power, current</th>
</tr>
</thead>
<tbody>
<tr>
<td>128 Channels / chip</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog</td>
<td>VDDA @ 1.2V</td>
<td>20 mW, 16mA</td>
<td>39 mW, 32mA</td>
</tr>
<tr>
<td>Digital Supply</td>
<td>VDD @ 0.9V</td>
<td>46 mW, 51mA</td>
<td>46 mW, 51mA</td>
</tr>
<tr>
<td><strong>Total Power</strong> / Chip</td>
<td>66 mW</td>
<td></td>
<td>85 mW</td>
</tr>
<tr>
<td>Total Power** / 20 Chip Module</td>
<td>1.3 W</td>
<td></td>
<td>1.7 W</td>
</tr>
</tbody>
</table>
Novel Tracker Technologies

• 3D -- Pixels for the inner detector

• InGrid for a Non Silicon TRT
3D Silicon Tracking

US Initiative -
**Sherwood Parker** – Hawaii, SLAC
S. Seidel - New Mexico
Kevin Einsweiler, Maurice Garcia-Sciveres (LBL)

![Diagram of 3D silicon tracking](image)

- **Active edge**: n, p⁺, 50 µm
- **3D**: particle, 500 µm
- **Standard Pixel or Strip**: PLANAR, 500 µm
- **Microcracks, chips induce surface leakage current**
3-D Silicon Tracking

- Low depletion fields
  Breakdown less likely
- Short Drift (50um)
  fast signals

Technology complex and still in development in the US and Europe.
3d Pixel Sensor for the Inner tracking layers

Introduction

The 3D sensor’s family

Full 3D
Active edge

3DC Fabricated at Stanford and tested with Atlas pixel
Readout - and SLHC fluences
Design at its 5th Generation

Being also fabricated at SINTEF in the ATLAS Upgrade framework as Part of the 3DC Consortium.
No data available yet

IRST and separately
CNM. Being presently fabricated
no data available yet

Double column
No active edge

ICEMos - Being presently fabricated
Work performed in the RD50 framework
No data available yet

Full 3D
No active edge

IRST/CNM fabricated in the RD50
Framework in 2005 Tested with SCTA
readout Electronics. Data and Simulations
show that the design is NOT radiation hard
For B-layer replacement.

Single column
No active edge
Suitable for ATLAS Pixels
Innermost layers
3D edge sensitivity using 13 keV X-rays at ALS-Berkeley

X-ray micro-beam scan, in 2 μm steps, of a 3D, n bulk and edges, 181 μm thick sensor. The left electrodes are p-type
Efficiency measured in test beam ~98%

Measurement Performed using a 2 μm beam

J. Hasi, C. Kenney,
J. Morse, S. Parker
**Ingrid**: Gas Filled Tracking for SLHC

One Gas filled Layer Provides all Track Coordinates

- 16 mm Ionization region
- Mesh
- Post Processing Creates Grid Structure and mesh
- Pixel chip
- Standard CMOS ASIC Technology with a Passivation Layer

X and Y from Pixel Position
Z from Pixel time
Ingrid is essentially a High Rate mini-Time Projection Chamber. The tracking information it provides can be available within a few hundred ns, making it suitable for Level 1 Trigger input.

Space point and two angles are measured:
- $\phi$ – In the pixel plane
- $\eta$ – Is an angle to the pixel plane
Test Beam results: comparison with MC

MC simulation: \( \text{Thr.} = 1.5 \text{ el, } \sigma_t = 300 \mu\text{m} \)

Angle \( \phi \)

- \( \sigma = 0.85^\circ \)
- \( \sigma = 0.95^\circ \)

Exp:
- \( \sigma = 0.95^\circ \)
- \( \sigma = 1.6^\circ \)

Reconstructed angle of the track.

Difference between reconstructed space points for two pseudo tracks.

Difference between angle of the track for two pseudo tracks.

Anatoli Romaniouk (ATLAS TRT group)
It is assumed that this detector will occupy the outer radii of the Inner Tracker.

Possible layout:
Two layers interleaved with moderator or dense TR radiator.

Why is that interesting?
A vector tracking!
(TR information might be a complementary feature)

1. Precision space points $X, Y$
2. Vector direction $\phi, \eta$

Anatoli Romaniouk
InGrid Gas Tracker

Test beam studies (5 GeV).

May 2008 test chamber:
- InGrid technology
- Drift distance = 16 mm
- $V_{\text{drift}} = 3800 \text{ V}$
- $E_{\text{drift}} = 2000 \text{ V/cm}$
- $V_{\text{amp}} \sim 470 \text{ V}$
- Gas gain $\sim 800 - 3500$
- Protection layer 30 $\mu$m
- Amplification gap - 50 $\mu$m
- Orientation: 20 degree to the beam and horizontal.

- Gas Mixtures
  - Ar/CO$_2$
  - Xe/CO$_2$
  - He/Isobutane

For the gas mixture 70%Xe+30%CO$_2$
- Total drift time $\sim 300 \text{ ns}$
- Ion signal $\sim 80 \text{ ns}$
- Transverse diffusion $\sigma_T \sim 220 \mu\text{m/cm}^{1/2}$
- Longitudinal diffusion $\sigma_L \sim 120 \mu\text{m/cm}^{1/2}$

Maximum gas gain achieved:
- $\sim 2500$
- Operating threshold $\sim 800 \text{ el.}$

Mesh

Charge

Si prot. layer

Pixels

Effective threshold $> 1600 \text{ el.}$
+ induced charge effect

This corresponds to a primary electron threshold $> 0.7 \text{ el}$

Anatoli Romaniouk
Conclusions

- A huge piece of work lies ahead and there is room and need for motivated participants.
- Although the exact schedule and magnitude of the upgrade is uncertain the need to upgrade will persist as beam intensity evolves over the next few years.

This talk has only covered the Inner Detector at ATLAS. Several additional sub-systems are seriously working on upgrade plans over a more relaxed time frame. In addition to what is discussed here, we are making and planning contributions to the Liquid Argon and MDT upgrade efforts.