High Speed, Low Power
Dual Operational Amplifier
AD826

FEATURES
High Speed:
- 50 MHz Unity Gain Bandwidth
- 350 V/μs Slew Rate
- 70 ns Settling Time to 0.01%
Low Power:
- 7.5 mA Max Power Supply Current Per Amp
Easy to Use:
- Drives Unlimited Capacitive Loads
- 50 mA Min Output Current Per Amplifier
- Specified for ±5 V, ±5 V and ±15 V Operation
- 2.0 V p-p Output Swing into a 150 Ω Load
  (V_S = ±5 V)
Good Video Performance
- Differential Gain & Phase Error of 0.07% & 0.11°
Excellent DC Performance:
- 2.0 mV Max Input Offset Voltage

APPLICATIONS
Unity Gain ADC/DAC Buffer
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video Line Driver
Active Filters

PRODUCT DESCRIPTION
The AD826 is a dual, high speed voltage feedback op amp. It is ideal for use in applications which require unity gain stability and high output drive capability, such as buffering and cable driving. The 50 MHz bandwidth and 350 V/μs slew rate make the AD826 useful in many high speed applications including: video, CATV, copiers, LCDs, image scanners and fax machines. The AD826 features high output current drive capability of 50 mA min per amp, and is able to drive unlimited capacitive loads. With a low power supply current of 15 mA max for both amplifiers, the AD826 is a true general purpose operational amplifier.

The AD826 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD826 can operate from a single +5 V supply, while still achieving 25 MHz of bandwidth. Furthermore the AD826 is fully specified from a single ±5 V to ±15 V power supplies.

The AD826 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 70 ns to 0.01%, with a low input offset voltage of 2 mV max. The AD826 is available in small 8-pin plastic mini-DIP and SO packages.

Driving a Large Capacitive Load

© Analog Devices, Inc., 1995
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700
Fax: 617/326-8703
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>$V_S$</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td>$\pm 5 , V$</td>
<td>30</td>
<td>35</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$\pm 15 , V$</td>
<td>45</td>
<td>50</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>0, $+5 , V$</td>
<td>25</td>
<td>29</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Bandwidth for 0.1 dB Flatness</td>
<td>$\pm 5 , V$</td>
<td>10</td>
<td>20</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>$\pm 15 , V$</td>
<td>25</td>
<td>55</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>0, $+5 , V$</td>
<td>10</td>
<td>20</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Full Power Bandwidth$^1$</td>
<td>$V_{OUT} = 5 , V$</td>
<td>$\pm 5 , V$</td>
<td>15.9</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{LOAD} = 500 , \Omega$</td>
<td>$V_{OUT} = 20 , V$</td>
<td>$\pm 5 , V$</td>
<td>5.6</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>$R_{LOAD} = 1 , k\Omega$</td>
<td>$\pm 5 , V$</td>
<td>200</td>
<td>250</td>
<td>V/$\mu$s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\pm 15 , V$</td>
<td>300</td>
<td>350</td>
<td>V/$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$0, +5 , V$</td>
<td>150</td>
<td>200</td>
<td>V/$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time to 0.1%</td>
<td>$-2.5 , V$ to $+2.5 , V$</td>
<td>$\pm 5 , V$</td>
<td>45</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>0 V to 10 V Step, $A_V = -1$</td>
<td>$\pm 15 , V$</td>
<td>45</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$-2.5 , V$ to $+2.5 , V$</td>
<td>$\pm 5 , V$</td>
<td>70</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>0 V to 10 V Step, $A_V = -1$</td>
<td>$\pm 15 , V$</td>
<td>70</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>NOISE/HARMONIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>$F_C = 1 , MHz$</td>
<td>$\pm 15 , V$</td>
<td>-78</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Noise</td>
<td>$f = 10 , kHz$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>15</td>
<td>nV/$\sqrt{Hz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current Noise</td>
<td>$f = 10 , kHz$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>1.5</td>
<td>pA/$\sqrt{Hz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gain Error (R1 = 150 $\Omega$)</td>
<td>$NTSC$</td>
<td>$\pm 15 , V$</td>
<td>0.07</td>
<td>0.1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$Gain = +2$</td>
<td>$\pm 5 , V$</td>
<td>0.12</td>
<td>0.15</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$0, +5 , V$</td>
<td>0.15</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Differential Phase Error (R1 = 150 $\Omega$)</td>
<td>$NTSC$</td>
<td>$\pm 15 , V$</td>
<td>0.11</td>
<td>0.15</td>
<td>Degrees</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$Gain = +2$</td>
<td>$\pm 5 , V$</td>
<td>0.12</td>
<td>0.15</td>
<td>Degrees</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$0, +5 , V$</td>
<td>0.15</td>
<td></td>
<td></td>
<td>Degrees</td>
<td></td>
</tr>
<tr>
<td><strong>DC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$ to $\pm 15 , V$</td>
<td>0.5</td>
<td>2</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Offset Drift</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>3.3</td>
<td>6.6</td>
<td>µV/$^\circ$C</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>10</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_{MAX}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>10</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>25</td>
<td>200</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_{MAX}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$, $\pm 15 , V$</td>
<td>500</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Offset Current Drift</td>
<td>$V_{OUT} = \pm 2.5 , V$</td>
<td>$\pm 5 , V$</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td>$R_{LOAD} = 500 , \Omega$</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>1.5</td>
<td>3</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{LOAD} = 150 , \Omega$</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>1.5</td>
<td>3</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = \pm 10 , V$</td>
<td>$\pm 15 , V$</td>
<td>3.5</td>
<td>6</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{LOAD} = 1 , k\Omega$</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>2</td>
<td>5</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = \pm 7.5 , V$</td>
<td>$\pm 15 , V$</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{LOAD} = 150 , \Omega$ (50 mA Output)</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>2</td>
<td>4</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>$V_{CM} = \pm 2.5 , V$, $T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$</td>
<td>300</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$V_{CM} = \pm 12 , V$, $T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 5 , V$</td>
<td>80</td>
<td>100</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td>$T_{MIN}$ to $T_{MAX}$</td>
<td>$\pm 15 , V$</td>
<td>86</td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>$\pm 15 , V$</td>
<td>80</td>
<td>100</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Parameter Conditions | $V_s$ | Min | Typ | Max | Units
---|---|---|---|---|---
**OUTPUT CHARACTERISTICS**
Output Voltage Swing | $R_{LOAD} = 500 \Omega$ | ±5 V | 3.3 | 3.8 | ±V
Output Voltage Swing | $R_{LOAD} = 150 \Omega$ | ±5 V | 3.2 | 3.6 | ±V
Output Voltage Swing | $R_{LOAD} = 1 \text{k} \Omega$ | ±15 V | 13.3 | 13.7 | ±V
Output Voltage Swing | $R_{LOAD} = 500 \Omega$ | ±15 V | 12.8 | 13.4 | ±V
Output Voltage Swing | 0, +5 V | +1.5, | +3.5 | V
Output Voltage Swing | ±5 V | 50 | mA
Output Voltage Swing | 0, ±5 V | 50 | mA
Output Voltage Swing | 0, +5 V | 30 | mA
Output Voltage Swing | ±5 V | 90 | mA
Output Voltage Swing | 0, ±5 V | 8 | Ω
Output Current | ±15 V | 50 mA
Output Current | ±5 V | 50 mA
Output Current | 0, +5 V | 30 mA
Output Current | ±15 V | 30 mA
Output Current | 0, ±5 V | 80 mA
Output Current | ±15 V | 100 mA
Output Current | 0, ±5 V | 100 mA
Output Resistance | Open Loop | 0, ±5 V | 1.5 V
Output Resistance | Open Loop | 0, ±5 V | 3.5 V
**MATCHING CHARACTERISTICS**
Dynamic Crosstalk | $f = 5 \text{ MHz}$ | ±15 V | -80 dB
Gain Flatness Match | $G = +1$, $f = 40 \text{ MHz}$ | ±15 V | 0.2 dB
Slew Rate Match | $G = -1$ | ±15 V | 10 V/μs
Input Offset Voltage Match | $T_{MIN} - T_{MAX}$ | ±5 V to ±15 V | 0.5 | 2 | mV
Input Bias Current Match | $T_{MIN} - T_{MAX}$ | ±5 V to ±15 V | 0.06 | 0.8 | μA
Open-Loop Gain Match | $V_o = ±10 \text{ V}$, $R_{LOAD} = 1 \text{k} \Omega$ | ±15 V | 0.15 | 0.01 | mV/V
Common-Mode Rejection Ratio Match | $V_{CM} = ±12 \text{ V}$, $T_{MIN} - T_{MAX}$ | ±15 V | 80 | 100 | dB
Power Supply Rejection Ratio Match | $V_s = ±5 \text{ V}$ to ±15 V, $T_{MIN} - T_{MAX}$ | ±15 V | 80 | 100 | dB
**POWER SUPPLY**
Operating Range | Dual Supply | ±2.5 | ±18 | V
Operating Range | Single Supply | ±5 | +36 | V
Quiescent Current/Amplifier | $T_{MIN} - T_{MAX}$ | ±5 V | 6.6 | 7.5 | mA
Quiescent Current/Amplifier | $T_{MIN} - T_{MAX}$ | ±5 V | 7.5 | mA
Quiescent Current/Amplifier | $T_{MIN} - T_{MAX}$ | ±15 V | 7.5 | mA
Quiescent Current/Amplifier | $T_{MIN} - T_{MAX}$ | ±15 V | 6.8 | 7.5 | mA
Power Supply Rejection Ratio | $V_s = ±5 \text{ V}$ to ±15 V, $T_{MIN} - T_{MAX}$ | 75 | 86 | dB

**NOTES**
1. Full power bandwidth = slew rate/2 $\pi V_{PEAK}$.
2. Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS**
Supply Voltage | ±18 V
Internal Power Dissipation | See Derating Curves
Plastic (N) | See Derating Curves
Small Outline (R) | See Derating Curves
Input Voltage (Common Mode) | ±$V_s$
Differential Input Voltage | ±6 V
Output Short Circuit Duration | See Derating Curves
Storage Temperature Range (N, R) | −65°C to +125°C
Operating Temperature Range | −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) | +300°C

**NOTES**
1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress ranking only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Specification is for device in free air: 8-pin plastic package, $\theta_J = 100$°C/watt; 8-pin SOIC package, $\theta_J = 155$°C/watt.

**ESD SUSCEPTIBILITY**
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD826 features proprietary ESD protection circuits, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

**ORDERING GUIDE**

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD826AN</td>
<td>−40°C to +85°C</td>
<td>8-Pin Plastic DIP</td>
<td>N-8</td>
</tr>
<tr>
<td>AD826AR</td>
<td>−40°C to +85°C</td>
<td>8-Pin Plastic SOIC</td>
<td>R-8</td>
</tr>
<tr>
<td>AD826AR-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Pin Plastic SOIC</td>
<td>R-8</td>
</tr>
</tbody>
</table>

Maximum Power Dissipation vs. Temperature for Different Package Types
AD826 - Typical Characteristics

Figure 1. Common-Mode Voltage Range vs. Supply Voltage

Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

Figure 2. Output Voltage Swing vs. Supply Voltage

Figure 5. Slew Rate vs. Supply Voltage

Figure 3. Output Voltage Swing vs. Load Resistance

Figure 6. Closed-Loop Output Impedance vs. Frequency
Figure 7. Input Bias Current vs. Temperature

Figure 8. Short Circuit Current vs. Temperature

Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

Figure 11. Open-Loop Gain vs. Load Resistance

Figure 12. Power Supply Rejection vs. Frequency
Figure 13. Common-Mode Rejection vs. Frequency

Figure 14. Large Signal Frequency Response

Figure 15. Output Swing and Error vs. Settling Time

Figure 16. Harmonic Distortion vs. Frequency

Figure 17. Input Voltage Noise Spectral Density

Figure 18. Slew Rate vs. Temperature
Figure 19. Closed-Loop Gain vs. Frequency

Figure 20. Differential Gain and Phase vs. Supply Voltage

Figure 21. Crosstalk vs. Frequency

Figure 22. Closed-Loop Gain vs. Frequency, Gain = –1

Figure 23. Gain Flatness Matching vs. Supply, G = +1

Figure 24. Crosstalk Test Circuit
Figure 25. Noninverting Amplifier Configuration

Figure 26. Noninverting Large Signal Pulse Response, \( R_L = 1 \, \text{k}\Omega \)

Figure 27. Noninverting Large Signal Pulse Response, \( R_L = 150 \, \Omega \)

Figure 28. Noninverting Small Signal Pulse Response, \( R_L = 1 \, \text{k}\Omega \)

Figure 29. Noninverting Small Signal Pulse Response, \( R_L = 150 \, \Omega \)
Figure 30. Inverting Amplifier Configuration

Figure 31. Inverting Large Signal Pulse Response, $R_L = 1\, \text{k}\Omega$

Figure 32. Inverting Large Signal Pulse Response, $R_L = 150\, \Omega$

Figure 33. Inverting Small Signal Pulse Response, $R_L = 1\, \text{k}\Omega$

Figure 34. Inverting Small Signal Pulse Response, $R_L = 150\, \Omega$
**THEORY OF OPERATION**

The AD826 is a low cost, wide band, high performance dual operational amplifier which can drive heavy capacitive and resistive loads. It also achieves a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD826 (Figure 35) consists of a degenerated NPN differential pair driving matched PNP s in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

![Figure 35. Simplified Schematic](image)

The capacitor, $C_F$, in the output stage mitigates the effect of capacitive loads. With low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, $C_F$ is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, $C_F$ is incompletely bootstrapped. Effectively, some fraction of $C_F$ contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

**INPUT CONSIDERATIONS**

An input protection resistor ($R_{IN}$ in Figure 25) is required in circuits where the input to the AD826 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a “balancing” resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of $R_{IN}$ and $R_F$ and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

**APPLYING THE AD826**

The AD826 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD826 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive and capacitive loads.

As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

**Circuit Board Layout**

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces inter-amp coupling.

**Choosing Feedback and Gain Resistors**

In order to prevent the stray capacitance present at each amplifier’s summing junction from limiting its performance, the feedback resistors should be $\leq 1$ kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1 pF–5 pF) may be paralleled with $R_F$ to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

**Power Supply Bypassing**

Proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier’s response.

Though two 0.1 µF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.
**SINGLE SUPPLY OPERATION**

An exciting feature of the AD826 is its ability to perform well in a single supply configuration (see Figure 37). The AD826 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: \((R_1 + R_3)/R_2\) combine with \(C_1\) to form a low frequency corner of approximately 30 Hz.

\[ \frac{1}{2\pi R_3 C_2} \]

R3 and C2 reduce the effect of the power supply changes on the output by low-pass filtering with a corner at \(\frac{1}{2\pi R_3 C_2}\).

The values for \(R_L\) and \(C_L\) were chosen to demonstrate the AD826's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, \(C_3\) was inserted in series with \(R_L\).

**PARALLEL AMPS PROVIDE 100 mA TO LOAD**

By taking advantage of the superior matching characteristics of the AD826, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). \(R_1\) and \(R_2\) are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

Figure 36. Single Supply Amplifier Configuration

![Figure 36](image)

Figure 37. Single Supply Pulse Response, \(G = +1\), \(R_L = 150\Omega\), \(C_L = 200\ pF\)

Figure 38. Parallel Amp Configuration

![Figure 38](image)
SINGLE-ENDED TO DIFFERENTIAL LINE DRIVER
Outstanding CMRR (> 80 dB @ 5 MHz), high bandwidth, wide supply voltage range, and the ability to drive heavy loads, make the AD826 an ideal choice for many line driving applications. In this application, the AD830 high speed video difference amp serves as the differential line receiver on the end of a back terminated, 50 ft., twisted-pair transmission line (see Figure 40). The overall system is configured in a gain of +1 and has a -3 dB bandwidth of 14 MHz. Figure 39 is the pulse response with a 2 V p-p, 1 MHz signal input.

Figure 39. Pulse Response

LOW DISTORTION LINE DRIVER
The AD826 can quickly be turned into a powerful, low distortion line driver (see Figure 41). In this arrangement the AD826 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>2nd Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. No Load</td>
<td>-78.5 dBm</td>
</tr>
<tr>
<td>2. 150 Ω R_L Only</td>
<td>-63.8 dBm</td>
</tr>
<tr>
<td>3. 150 Ω R_L 7.5 Ω R_C</td>
<td>-70.4 dBm</td>
</tr>
</tbody>
</table>

In this application one half of the AD826 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD826’s ability to operate from low supply voltages. R_C varies with the load and must be chosen to satisfy the following equation:

\[ R_C = M R_L \]

where \( M \) is defined by \((M + 1) G_S = G_D\) and \( G_D = \) Driver’s Gain, \( G_S = \) System Gain.
HIGH PERFORMANCE ADC BUFFER

Figure 42 is a schematic of a 12-bit high speed analog-to-digital converter. The AD826 dual op amp takes a single ended input and drives the AD872 A/D converter differentially, thus reducing 2nd harmonic distortion. Figure 43 is a FFT of a 1 MHz input, sampled at 10 MHz with a THD of –78 dB. The AD826 can be used to amplify low level signals so that the entire range of the converter is used. The ability of the AD826 to perform on a ±5 volt supply or even with a single 5 volts combined with its rapid settling time and ability to deliver high current to complicated loads make it a very good flash A/D converter buffer as well as a very useful general purpose building block.

Figure 42. A Differential Input Buffer for High Bandwidth ADCs

Figure 43. FFT, Buffered A/D Converter
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

8-Pin Plastic Mini-DIP (N) Package

8-Pin SO (R) Package

All brand or product names mentioned are trademarks or registered trademarks of their respective holders.