Performance of the Electronics for the Sudbury Neutrino Observatory

E.W. Beier, D.F. Cowen, P.T. Keener, J.R. Klein, F.M. Newcomer, D.S. McDonald, M. Neubauer, R. Van Berg, R.G. Van de Water, P. Wittich
Dept. of Physics & Astronomy, University of Pennsylvania, Philadelphia, Pa. 19104

Abstract

The Sudbury Neutrino Observatory (SNO) is a second generation solar neutrino water Cherenkov detector using 1,000 Tonnes of D_2O viewed by almost 10,000 20cm Photomultiplier tubes. The observatory, located 6,800' below ground in INCO Ltd's Creighton mine near Sudbury Ontario, recently began full time operation.

The SNO electronics provides deadtimeless sub-ns time and 0.1 - 1000 photoelectrons (pe) of charge measurement. While the solar neutrino event rate is low, the electronics must handle backgrounds in excess of 1 kHz and bursts in excess of 1 MHz. The integrated trigger system handles multiple independent triggers via 10,000:1 analog sums.

The electronics use three full custom integrated circuits plus standard commercial chips. There are 14 different printed circuit boards mounted in custom crates and racks. The DAQ interface is VME compatible.

I. INTRODUCTION

The signal processing electronics [1] is arranged into nineteen identical "SNO" crates, each processing signals from 512 photomultipiers. The analog processing is implemented in three custom integrated circuits: a bipolar amplifier-shaper, a bipolar discriminator, and a CMOS time measurement and 16 event analog storage chip. The design provides a self triggered, essentially deadtimeless, measurement of time (< 1 ns) and charge (< 0.1 photoelectrons (p.e.) to > 1000 p.e.) with a burst capability above 1 MHz and a sustained low energy event rate better than 1 KHz.

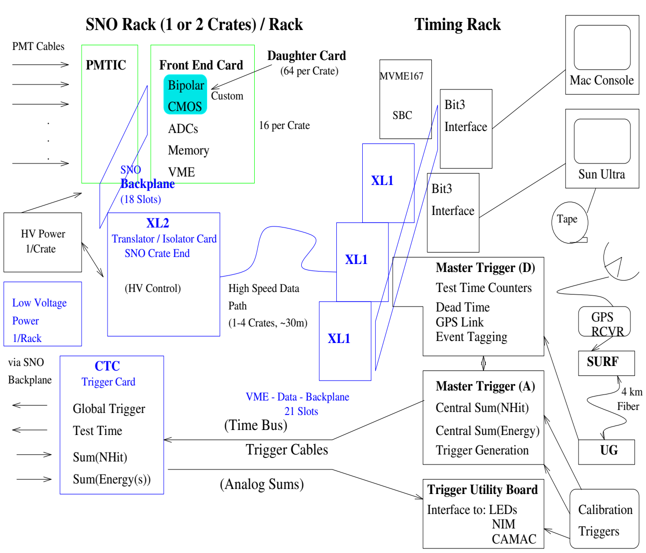

Figure 1 SNO system block diagram showing signal flow from the PMT cables on the left to the event recording computers on the right.

One front end board processes 32 channels, digitizes the signals, and stores the digital results in a 4 MB memory (designed for bursts such as expected from a potential nearby supernova). Sixteen front-end boards, a trigger formation card, and a bus translator card to a VME "interface" crate are in each SNO crate. The 9,546 SNO PMTs are handled in 19 SNO crates in 11 racks spaced around the periphery of the detector *deck* (the mechanical structure which supports the detector itself). Data acquisition is accomplished through the VME interface crate, which polls the 19 SNO crates for data. The VME crate and the central timing and triggering system reside in a centrally located rack. A GPS receiver on the surface delivers a 10MHz clock and requested time code checks through four km of fiber optic cable. The cable length is continuously monitored and corrected for so that individual events are tagged with UMT within the GPS receiver error. A block diagram of the signal processing electronics is shown in Figure 1.

II. FRONT END SIGNAL FLOW

A. *High Voltage and Test Pulsers*

The PMT signal cables are attached in groups of eight to PMT interface cards (PMTIC) that provide HV distribution to the individual channels from a crate level bulk supply. The PMTIC also provides HV monitoring and on/off control (eight tubes at a time) plus a precision charge injection pulser and PMT base current monitor for each channel.

B. *Custom Integrated Circuits*

An AT&T (now Lucent Technologies) analog bipolar process (CBICU-II) was used to implement the designs for a four channel dual range amplifier-shaper-integrator chip (SNOINT) and a four channel discriminator--timer companion chip (SNOD)[2]. These two front end chips are joined by a single channel CMOS device (QUSN7), fabricated in the Northern Telecom CMOS4s process. QUSN7 provides a time to amplitude converter (TAC) and sixteen cells of analog memory for the TAC and three different charge measurements as well as a trigger identification counter, trigger primitive generators, and a totals counter.

C. *Front End Board and Daughter Board*

The initial sixteen fold analog memory in QUSN7 is the first level of buffering in the system. The analog and digital data in this analog memory chip are moved from the

Daughter Board which holds the custom integrated circuits and handles all of the analog signal processing onto the Front End Card for digitization and the digitizations plus trigger ID and flag data are stored in a local 4MB RAM on each front-end card via a simple FPGA implemented state machine. This local memory is then read out over the crate bus into the central VME crate by the DAQ computer. Events are assembled in the computer from the single PMT bundles (12 bytes per hit PMT) plus 24 bytes of trigger and timing information from the MTC/D to make up a complete event packet. The 24 bit Trigger ID is unique for up to 16 million events in order to allow the 1.2GB of front end RAM in the system to buffer high rate events and to allow eventual correlation of PMT bundles with Trigger information.

III. TRIGGER FLOW

The integrated trigger system is implemented as two different NHIT and two different Energy analog sums which gather all 19**x**512 channels into a single central trigger system. Any of the 9,728 discriminators firing produces a current pulse of 20 or 100 ns duration (NHIT20 and NHIT100) and about 600 μA amplitude into the 9,728:1 sum. Each NHIT20 or NHIT100 pulse is width programmable and may be masked out if desired. The energy sums, which directly copy the PMT inputs, are not maskable. A threshold precision of plus or minus a few PMTs is easily maintained in practice as can be seen in Figures 2 and 3. The central trigger system (MTC/Analog and MTC/Digital) provide the final level of analog summing (19:1) and threshold setting plus local and GPS driven clocks to provide time stamps to each event. A wide variety of internal pulsers and external trigger inputs provide for great flexibility in running the detector.

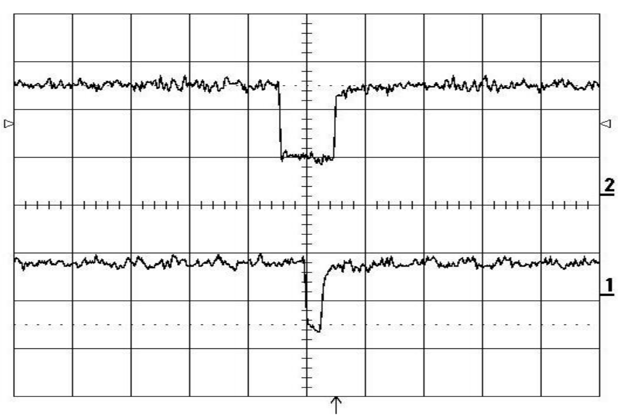

Figure 2: NHIT100 (top) and NHIT20 (bottom) from a single PMT after the 10,000:1 analog summation - 100ns and 20mV per div.

Analog sums passing a preset threshold in an MTC/A or direct digital inputs to the MTC/D, if they are masked in, cause a global trigger (GT) signal to be distributed to all 19 crates. The GT acts as a common stop for any active TACs and increments a Trigger ID counter at each channel. The total trigger formation time is dominated by the 30 m of cable required to transport analog sums from the crates to the Trigger System in the centrally located Timing Rack and then to return the GT signal to the crates. The timing is adjusted so that "late" light from reflections across the 17 m detector can be collected. Each front-end channel has its internal timing set up via DACs on the Front End Card so that the channel stays active for the required time – roughly 400ns from earliest to latest interesting light. The MTC/D can refire a new GT immediately after a preset "lockout" time (nominally 420ns) and will do so either on a new trigger input or if the original trigger input is still over threshold near the end of the previous cycle.

By having multiple thresholds on each MTC/A signal, it is possible to measure the actual trigger efficiency (number of hits recorded vs. number of hits triggered on) at any given number of hits. Figure 3 shows the measured efficiency in units of NHIT for laser data in air at the center of the detector. Trigger efficiencies with water in the detector will be somewhat different given the difference in index of refraction.

Figure 4 shows the NHIT100 trigger in conjunction with an ESUM trigger for an event with a large energy deposition in one PMT and a very small number of additional detected photoelectrons such as one might expect from a radioactive decay in the PMT glass. The ESUM triggers are shaped to be somewhat slower and of significantly lower amplitude than an unprocessed PMT output, but are an especially valuable method of looking at 10,000 PMT outputs at one time.

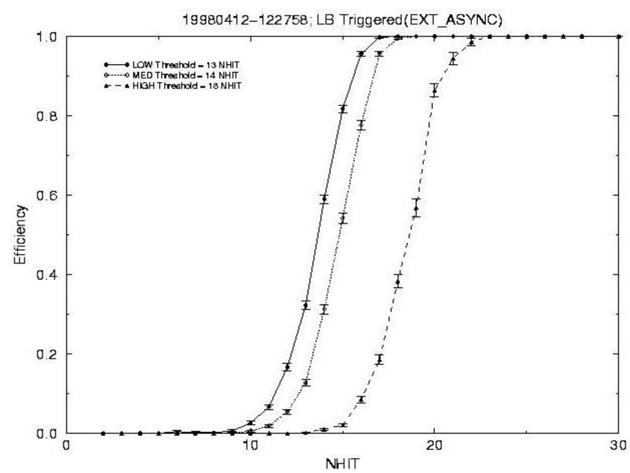

Figure 3: Trigger Efficiency vs. NHIT for various thresholds. Laser source in air at the center of the detector.

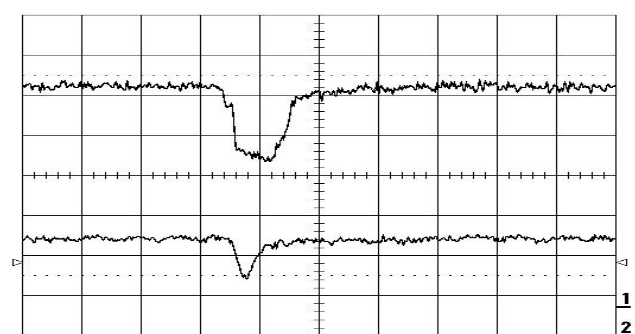

Figure 4: NHIT100, top, ESUM, bottom trace – 100ns/div. The NHIT signal indicates only a few (3-4) tubes have fired while the ESUM indicates a total charge equivalent to many tens of PMTs firing.

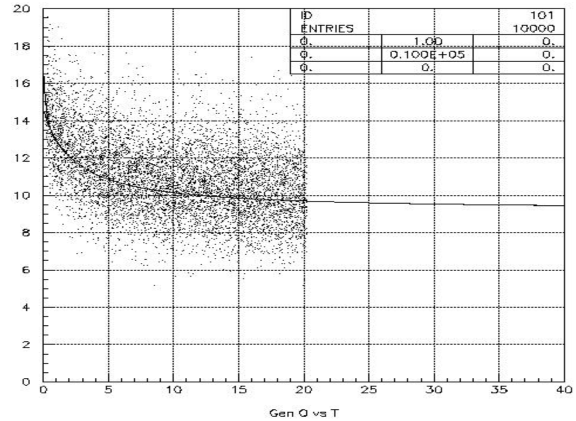

Figure 7: Charge in pe vs. Time in ns measured with a triggered single pe laser source. The fit function is used to correct the time for the measured charge on a tube by tube basis for each event.

V. TIME MEASUREMENTS

The CMOS TAC circuit is started by any PMT discriminator pulse and either runs out of time and resets or is stopped by a Global Trigger (GT) pulse. The MTC/D uses the local 50 MHz precision oscillator to generate test pulses which can then be interpolated using an Analog Devices AD9500 time delay chip to ~ 50ps precision. By using this built in test pulser, the time response of the TACs can be measured precisely and regular runs are made of 10,000 TAC slopes as well as pedestals. Figure 5 shows one such measurement. A global fit is then made to the small imperfections in the TAC response and, as seen in Figure 6, an rms time error of less than 200ps can be achieved for large signals. For small signals there is significant walk or slewing due to the significant risetime of the PMT pulse, the small, but non-zero, discriminator walk, the photostatistics, and the PMT amplifier statistics. These effects are measured using a laser to inject light into the PMTs. The measured time vs. charge curve, shown in Figure 7, is then used as a global correction to time measurements based upon the measured charge.

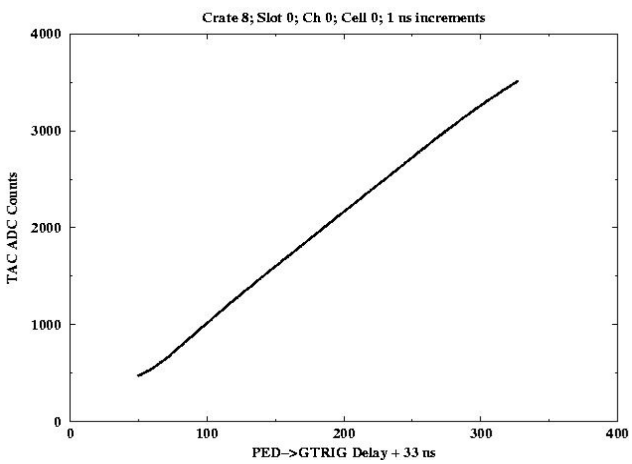

Figure 5: TAC time in counts vs. MTC/D test pulse time in ns for a single channel.

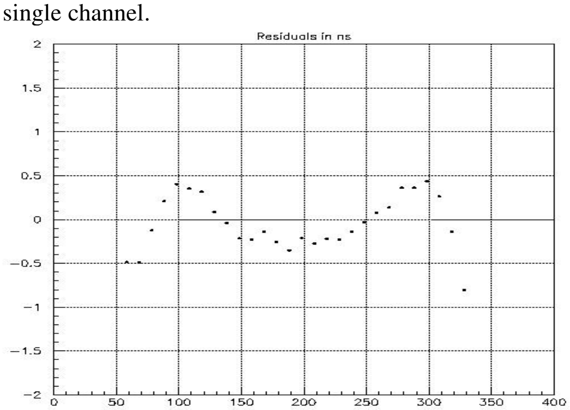

Figure 6: Time fit residuals in ns vs. delay time.

VI. CHARGE MEASUREMENTS

Charge from a PMT pulse is split into two separate integration channels with a relative gain of 16:1 to allow for a larger dynamic range (bi-linear integration). The charge is integrated under the control of the sample time generated in the SNOD chip. There are two separate sample times (*short*, about 70 ns for direct light and *long*, about 400 ns for scattered light). Channel to channel electronic gains are checked via the built in channel charge pulsers and the ADC counts are calibrated in pico Coulombs as shown in Figure 8.

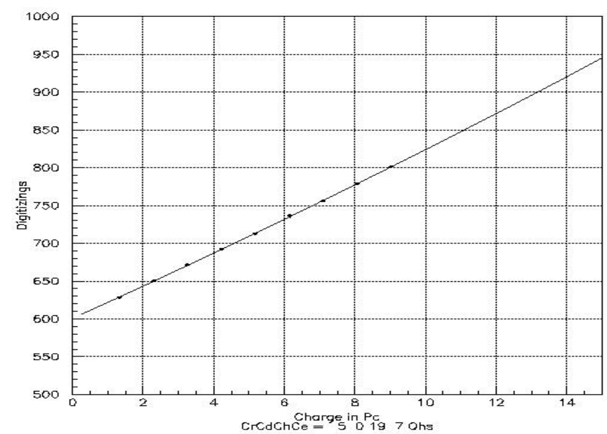

Figure 8: ADC counts vs. injected charge for the high gain short integrate charge measurement (Q_{HS}) – 1 pC ~ 25 ADC counts.

In addition to the charge injection pulser, there is a separate *pedestal* function in each discriminator that forces a channel to go through a zero charge measurement cycle and thus allows a direct measurement of the pedestal for each of the sixteen analog storage locations for each of the three measured charges for that channel. The pedestals have proven to be gratifyingly stable. Figure 9 shows the differences in ADC counts (~ 20 counts per pe) cell by cell, channel by channel between runs on May 14 and August 7, 1998, for 6,900 channels. The gaussian fit is to give a quantitative estimate of the magnitude of the changes. Most of the outliers are due to replacement of a few Daughter Cards.

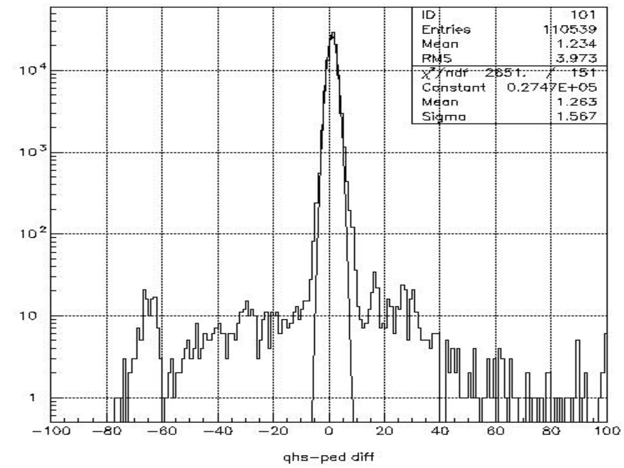

Figure 9: Pedestal changes over an 86 day period (August 7 to May 14) for 6,900 channels times 16 Analog Memory Cells. The average change is 1.2 counts (where a single pe is about 20 counts) and the rms error is about 1.5 counts.

Each PMT has a slightly different gain so that the final calibration must be made with a light source. SNO has both laser and sonoluminescent sources that can be used to make a single photoelectron calibration. Figure 10 shows the response of one channel to a single pe input at various threshold settings. Note that moving the discriminator threshold changes only the low charge side of the distributions. By looking at all 9,546 of these distributions[1] it is possible to calculate the detector efficiency.

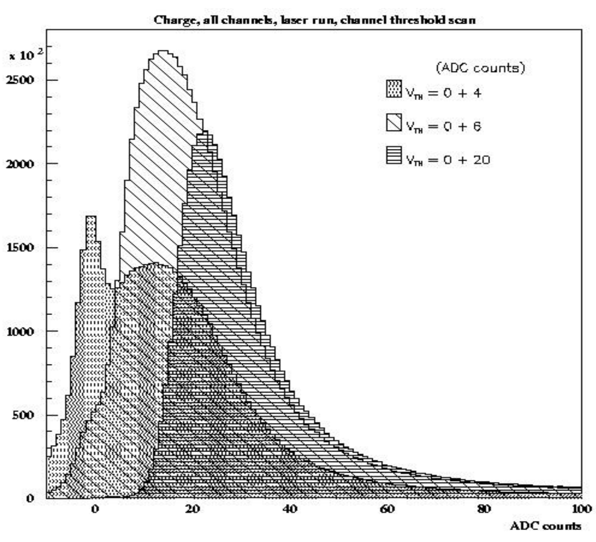

Figure 10: Single channel charge measurement for single photoelectrons vs. different threshold settings. The different thresholds correspond, roughly, to 1/5, 1/3, and 1.2 photoelectron where a single photoelectron is defined as the mean of the low threshold setting distribution.

[1] The SNO detector has 9,546 active PMTs installed. Some of the 9,728 electronics channels not used for ordinary PMTs are used for dynode taps (to extend the dynamic range) and the remainder are used for calibration sources.

VII. Self Testing Capability

As noted in several places above, the system is designed to include most, if not all, of the necessary tools to verify and monitor its integrity and operation. In addition to the 10,000 time and charge adjustable pulsers, each Front End Card incorporates an ADC to measure DC power voltages, an embedded temperature transducer, and the PMT base current resistors on the PMT Interface Card. Each analog set point (thresholds, timing widths, TAC slopes, etc.) in the system is individually controlled by a digital to analog converter (DAC) – nearly 60,000 set points in all. The trigger system also includes voltage measuring capability so that thresholds and offsets can be monitored and controlled.

The net effect of all of these controls is that most of the setup routines for the system can be completely automated. For instance, the integrator sample time for both short and long sample times and the total time of interest for the TAC can all be measured and adjusted, channel by channel in a few minutes using the built in pulsers. Many tasks like pedestal measurement and trigger and discriminator zeros can be measured in a non-intrusive fashion during actual data taking.

VIII. Acknowledgments

The authors gratefully acknowledge R. Ford, A. Hallin, and A. Hamer of Queen's University, Kingston Ontario who provided the laser system for some of these measurements, W. Frati of Penn who provided several of the analyses and R. Hanson and J. Karn of the University of Guelph, Guelph Ontario who connected the detector and collected much of the data shown here, and, of course, the entire SNO collaboration which made the whole enterprise possible.

IX. References

[1] T. Ekenberg, F.M. Newcomer and R. Van Berg, A Biman, R.L. Stevenson, "The Sudbury Neutrino Electronics Chain," *Transactions on Nuclear Science*, vol. 042 N4, pp.925-932, August 1995.

2] F.M. Newcomer and R. Van Berg, "A Wide Dynamic Range Integrator-Discriminator-Timer Chip Set for PMT Applications," *Transactions on Nuclear Science*, vol. 042 N4, pp.1068-1076, August 1995.