FEC32M Table of Contents

page number	description
1	root
2 a,b	daughter board connectors
3	ADC subroot with unity gain buffers
4	ADC unit with opamp, adc
5 a,b,c	backplane connectors and interface logic
6 a,b	serial DACs and calibration DAC
7	FIFO memory: memory controller, simm, and FIFO controller
8 a,b,c,d	register address decoding and register subpages. LEDs.
9	board id register
10	adc register
11	CALIBRATION DAC SETTING REGISTER
12 a,b	CMOS readput and programming register.
13	DAC programming register
14	general control/status register
15	pedestal enable register
16	voltage monitor select and adc readout register
17	high voltage control/status register
19	sequencer
20 A,B,C	VOLTAGE REFERENCES AND MONITORS. TEMPERATURE MONITOR. BYPASS CAPS.
21	trigger component, mother board.
22	HV BACKPLANE CONNECTORS
23	DAUGHTER BOARD CONNECTORS

offset indicates sublevel of hierarchy.

DRAWING

UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE: CONTENTS ABBREV=CNTNTS

LAST_MODIFIED=Mon Jan 29 13:14:24 1996

DATE:

ENGINEER:

PAGE: 0