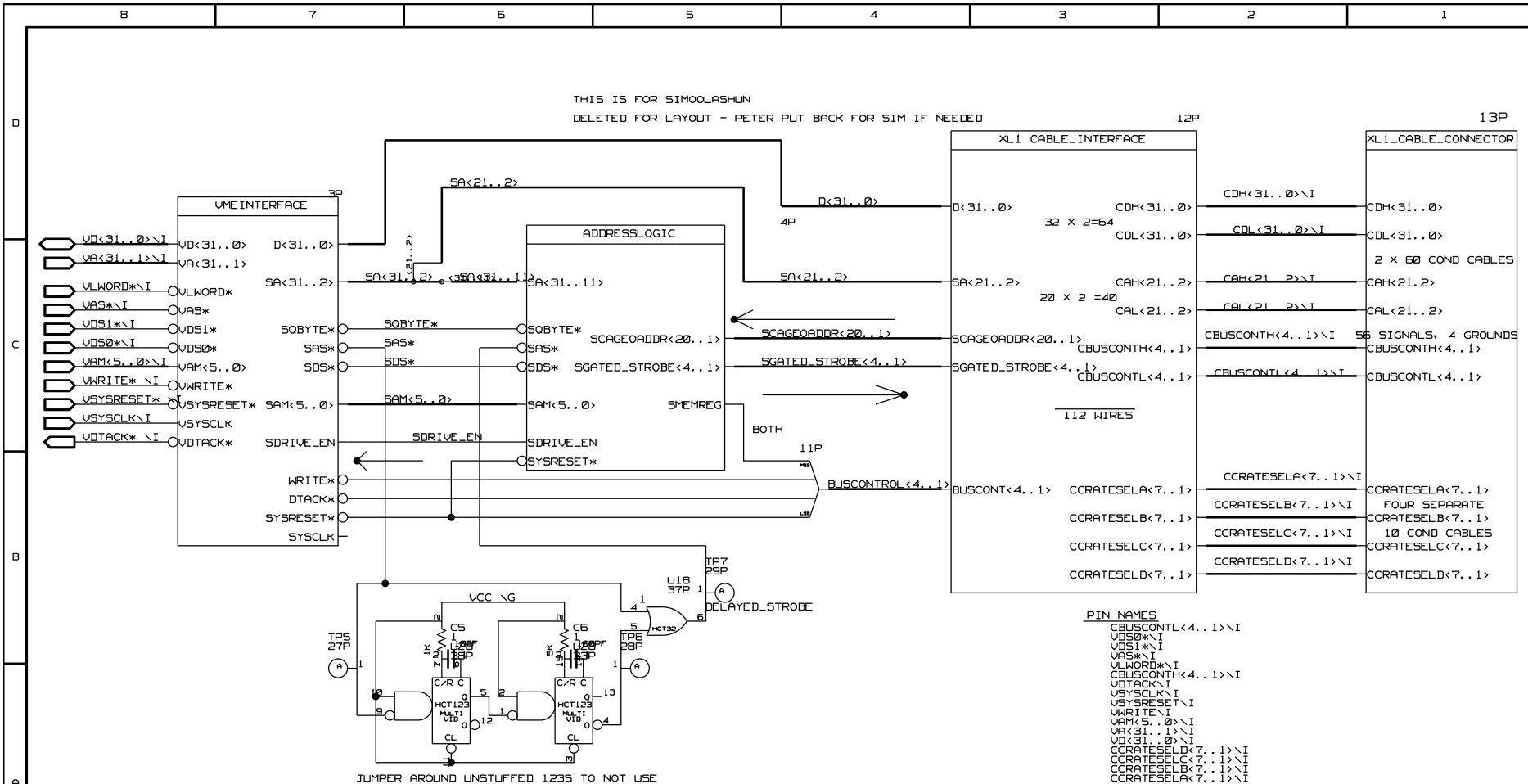
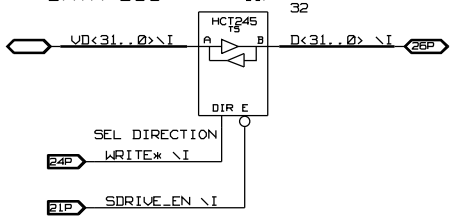
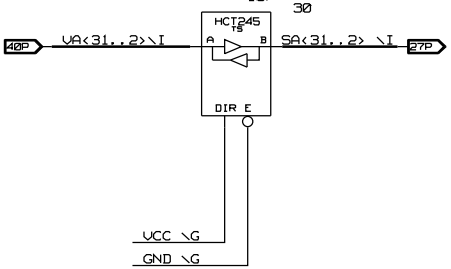

THIS IS FOR SIMOOLASHUN
DELETED FOR LAYOUT - PETER PUT BACK FOR SIM IF NEEDED
12P
13P
VMEINTERFACE
3P
ADDRESSLOGIC
XL1 CABLE_INTERFACE
XL1_CABLE_CONNECTOR
VD<31..0>\I
VA<31..1>\I
VLWORD*\I
VAS*\I
VDS1*\I
VDS0*\I
VAM<5..0>\I
VWRITE* \I
VSYSRESET*
VSYSCLK\I
VDTACK* \I
D<31..0>
SA<31..2>
SQBYTE*
SAS*
SDS*
SAM<5..0>
SDRIVE_EN
WRITE*
DTACK*
SYSRESET*
SYSCLK
SA<21..2>
SA<31..11>
SCAGEOADDR<20..1>
SGATED_STROBE<4..1>
SMEMREG
SYSRESET*
4P
32 X 2=64
20 X 2 =40
CDH<31..0>
CDL<31..0>
CAH<21..2>
CAL<21..2>
CBUSCONTH<4..1>
CBUSCONTL<4..1>
112 WIRES
56 SIGNALS, 4 GROUNDS
2 X 60 COND CABLES
BOTH
11P
BUSCONTROL<4..1>
BUSCONT<4..1>
CCRATESELA<7..1>
CCRATESELB<7..1>
CCRATESELC<7..1>
CCRATESELD<7..1>
FOUR SEPARATE
10 COND CABLES
TP7
29P
U18
37P
DELAYED_STROBE
VCC \G
C5
C6
1K
5K
100PF
33P
TP5
27P
TP6
28P
C/R C
HCT123
MULTI
VIB
CL
HCT32
JUMPER AROUND UNSTUFFED 1235 TO NOT USE
PIN NAMES
CBUSCONTL<4..1>\I
VDS0*\I
VDS1*\I
VAS*\I
VLWORD*\I
CBUSCONTH<4..1>\I
VDTACK\I
VSYSCLK\I
VSYSRESET\I
VWRITE\I
VAM<5..0>\I
VA<31..1>\I
VD<31..0>\I
CCRATESELD<7..1>\I
CCRATESELC<7..1>\I
CCRATESELB<7..1>\I
CCRATESELA<7..1>\I
CDH<31..0>\I
CDL<31..0>\I
CAH<21..2>\I
CAL<21..2>\I
DRAWING
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE:
XL1
VME EXTENDER SYSTEM
ABBREV=XL1
LAST_MODIFIED=Tue Feb 20 16:01:34 1996
DATE:
ENGINEER:
RVB
PAGE:
1 OF ?

VME INTERFACE

DATA BUS



ADDRESS BUS

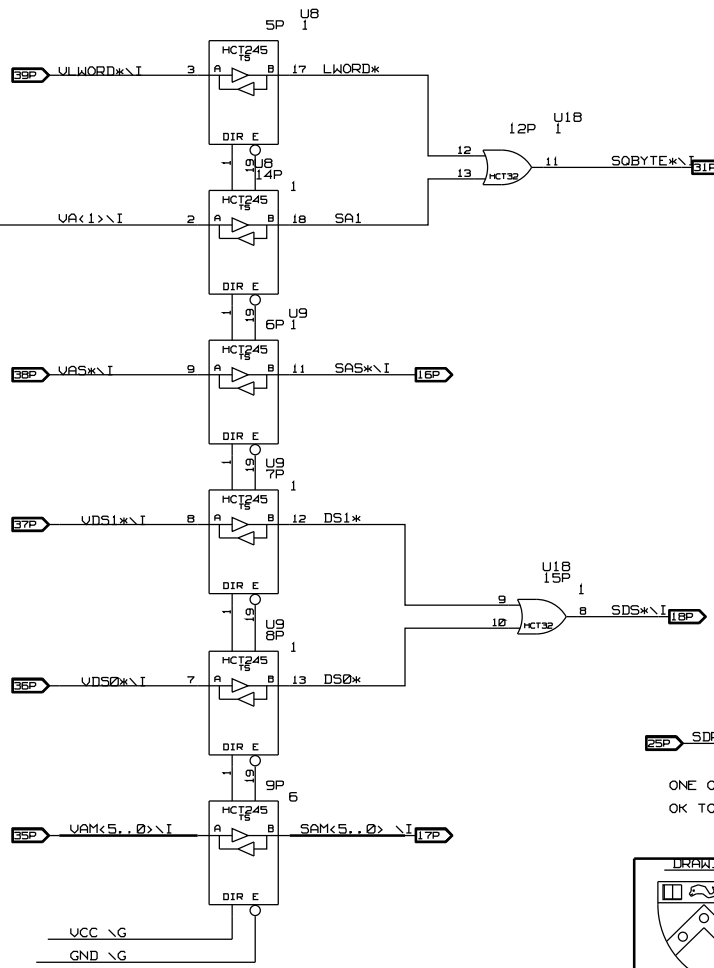


FOR X245, WHEN DIR = LOW, GOES FROM B TO A

PIN NAMES

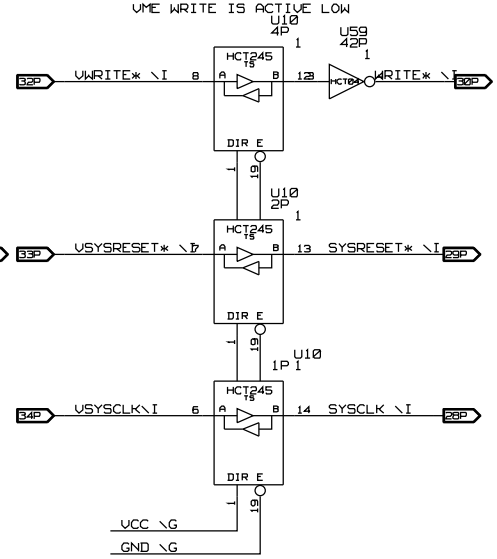
VSYSRESET*\I
DTACK*\I
WRITE*\I
VWRITE*\I
VDTACK*\I
SYSRESET*\I
SA<31..2>\I
SAM<5..0>\I
SDRIVE_EN\I
SDS*\I
SAS*\I
SQBYTE*\I
VD50*\I
VD51*\I
VAS*\I
VLWORD*\I
VD<31..0>\I
VA<31..1>\I
VAM<5..0>\I
VSYSCLK\I
SYSCLK\I
D<31..0>\I

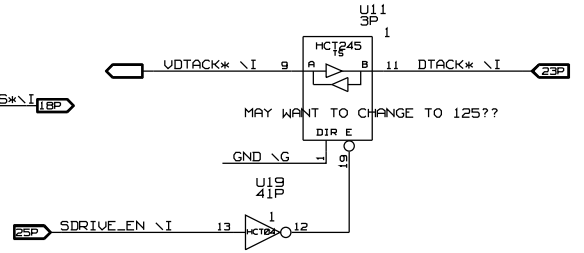
STROBES AND DATA MODIFIERS



CONTROL SIGNALS

VME WRITE IS ACTIVE LOW





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HIGH ENERGY PHYSICS

TITLE: VMEINTERFACE
VMEINT

DATE:

LAST MODIFIED=Tue Feb 20 16:01:44 1996

ENGINEER: RVB, PW

PAGE: 1 OF 1

VME INTERFACE CONNECTORS

J1 - TOP CONNECTOR

J2
2P

EUROCONN

	A	B	C	
VD<00>\I	A1	B1	C1	VD<08>\I
VD<01>\I	A2	B2	C2	VD<09>\I
VD<02>\I	A3	B3	C3	VD<10>\I
VD<03>\I	A4	B4	C4	VD<11>\I
VD<04>\I	A5	B5	C5	VD<12>\I
VD<05>\I	A6	B6	C6	VD<13>\I
VD<06>\I	A7	B7	C7	VD<14>\I
VD<07>\I	A8	B8	C8	VD<15>\I
GND \G	A9	B9	C9	GND \G
VSYSCLK\I	A10	B10	C10	
GND \G	A11	B11	C11	
VDS1*\I	A12	B12	C12	VSYSRESET* \I
VDS0*\I	A13	B13	C13	VLWORD*\I
VWRITE* \I	A14	B14	C14	VAM<5>\I
GND \G	A15	B15	C15	VA<23>\I
VDTACK* \I	A16	B16	C16	VA<22>\I
GND \G	A17	B17	C17	VA<21>\I
VAS*\I	A18	B18	C18	VA<20>\I
GND \G	A19	B19	C19	VA<19>\I
	A20	B20	C20	VA<18>\I
	A21	B21	C21	VA<17>\I
	A22	B22	C22	VA<16>\I
VAM<4>\I	A23	B23	C23	VA<15>\I
VA<07>\I	A24	B24	C24	VA<14>\I
VA<06>\I	A25	B25	C25	VA<13>\I
VA<05>\I	A26	B26	C26	VA<12>\I
VA<04>\I	A27	B27	C27	VA<11>\I
VA<03>\I	A28	B28	C28	VA<10>\I
VA<02>\I	A29	B29	C29	VA<09>\I
VA<01>\I	A30	B30	C30	VA<08>\I
	A31	B31	C31	
VMEP5V	A32	B32	C32	VMEP5V

	B
B1	33 VBBSY
B2	34 VBCLR
B3	35 VACFAIL
B4	36
B5	37
B6	38
B7	39
B8	40
B9	41
B10	42
B11	43
B12	44
B13	45
B14	46
B15	47
B16	48 VAM<0>\I
B17	49 VAM<1>\I
B18	50 VAM<2>\I
B19	51 VAM<3>\I
B20	52 GND \G
B21	53
B22	54
B23	55 GND \G
B24	56
B25	57
B26	58
B27	59
B28	60
B29	61
B30	62
B31	63
B32	64 VMEP5V

J2 BOTTOM CONNECTOR

J1
1P

EUROCONN

	A	B	C	
1	A1	B1	C1	65
2	A2	B2	C2	66
3	A3	B3	C3	67
4	A4	B4	C4	68
5	A5	B5	C5	69
6	A6	B6	C6	70
7	A7	B7	C7	71
8	A8	B8	C8	72
9	A9	B9	C9	73
10	A10	B10	C10	74
11	A11	B11	C11	75
12	A12	B12	C12	76
13	A13	B13	C13	77
14	A14	B14	C14	78
15	A15	B15	C15	79
16	A16	B16	C16	80
17	A17	B17	C17	81
18	A18	B18	C18	82
19	A19	B19	C19	83
20	A20	B20	C20	84
21	A21	B21	C21	85
22	A22	B22	C22	86
23	A23	B23	C23	87
24	A24	B24	C24	88
25	A25	B25	C25	89
26	A26	B26	C26	90
27	A27	B27	C27	91
28	A28	B28	C28	92
29	A29	B29	C29	93
30	A30	B30	C30	94
31	A31	B31	C31	95
32	A32	B32	C32	96

	B	C
B1	33 VMEP5V	
B2	34 GND \G	
B3	35	
B4	36 VA<24>\I	
B5	37 VA<25>\I	
B6	38 VA<26>\I	
B7	39 VA<27>\I	
B8	40 VA<28>\I	
B9	41 VA<29>\I	
B10	42 VA<30>\I	
B11	43 VA<31>\I	
B12	44 GND \G	
B13	45 VMEP5V	
B14	46 VD<16>\I	
B15	47 VD<17>\I	
B16	48 VD<18>\I	
B17	49 VD<19>\I	
B18	50 VD<20>\I	
B19	51 VD<21>\I	
B20	52 VD<22>\I	
B21	53 VD<23>\I	
B22	54 GND \G	
B23	55 VD<24>\I	
B24	56 VD<25>\I	
B25	57 VD<26>\I	
B26	58 VD<27>\I	
B27	59 VD<28>\I	
B28	60 VD<29>\I	
B29	61 VD<30>\I	
B30	62 VD<31>\I	
B31	63 GND \G	
B32	64 VMEP5V	

3P

POWER_IN

VMEP5V — VMEP5V

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UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE: VMEINTERFACE VMEINT	DATE:
ENGINEER: RVB	PAGE: 2 OF 2

LAST MODIFIED=Tue Feb 20 16:01:47 1996

CRATE ADDRESS RECOGNIZE

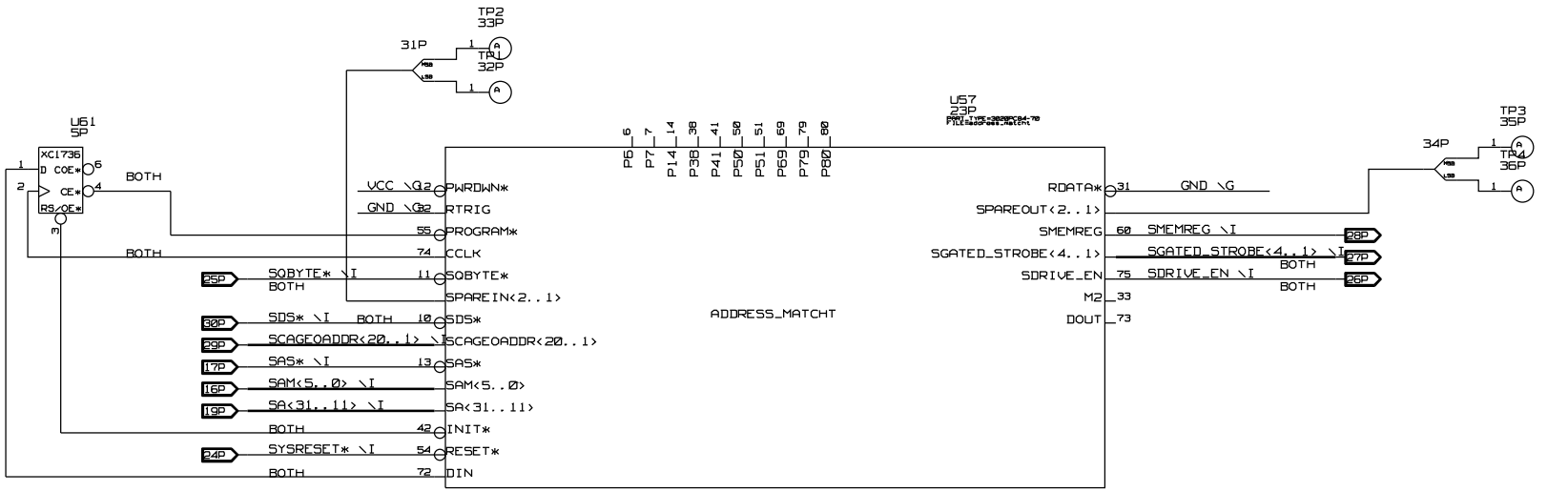
FOR THE 5 RELEVANT BITS, COMPARE WITH THESE CRATES

LONGWORD AND VA<1> BOTH LOW=LOW QBYTE (CAGEOADDR<XXXXX>) - MAKE GATED STROBE IF VALID

STROBE IFF LONGWORD, DS0, DS1, AND AS ASSERTED

ADDRESS VALIDATION

THIS WIRING ASSUMES THAT CRATE ADDRESS IS IN BITS 26..22
IF SOME OTHER 5 BITS IN RANGE 31..22 ARE USED THEN TOP 'OR'
SHOULD BE REWIRED WITH NEW 'IDENTICALLY ZERO' BITS
FOR REGISTER SPACE, ALL BITS 31..16 MUST = ZERO



DRAWING

UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE: ADDRESSLOGIC
ADDRESSLOGICLAST_MODIFIED=Tue Feb 20 16:01:55 1996

DATE:

ENGINEER: RVB

PAGE: 1 OF 1

CRATE ADDRESS RECOGNIZE

LONGWORD AND VA<1> BOTH LOW=LOW QBYTE

FOR THE 5 RELEVANT BITS, COMPARE WITH THESE CRATES
(CAGEOADDR<XXXXX>) - MAKE GATED STROBE IF VALID

STROBE IFF LONGWORD, DS0, DS1, AND AS ASSERTED

BOTH DS<0> AND DS<1> LOW

CORRECTED TO BIT3 LIMITATIONS
REQUIRES BIT 15 HIGH FOR REG
REQUIRES BIT 26 LOW FOR MEM

BITS NOT USED IN MEMORY MAP

USED IN MEMORY MAP, NOT REGISTER

ALWAYS NOT USED IN REGISTER

ADDRESS MODIFY DECODE

EXTENDED NON PRIV ACCESS (MEM)

SHORT NON PRIV ACCESS (REG)

ADDRESS VALIDATION

THIS WIRING ASSUMES THAT CRATE ADDRESS IS IN BITS 26..22
IF SOME OTHER 5 BITS IN RANGE 31..22 ARE USED THEN TOP 'OR'
SHOULD BE REWIRED WITH NEW 'IDENTICALLY ZERO' BITS
FOR REGISTER SPACE, ALL BITS 31..16 MUST = ZERO

GATED STROBE ONLY IF LONGWORD TRANSFER, RECOGNIZED MEMORY OR
REGISTER ADDRESS, AND RECOGNIZED CRATE

ONE OF THESE 4 CRATES IS ACTIVE
OK TO DRIVE VME BUS (DATA AND DTACK)

3020PCB4-70

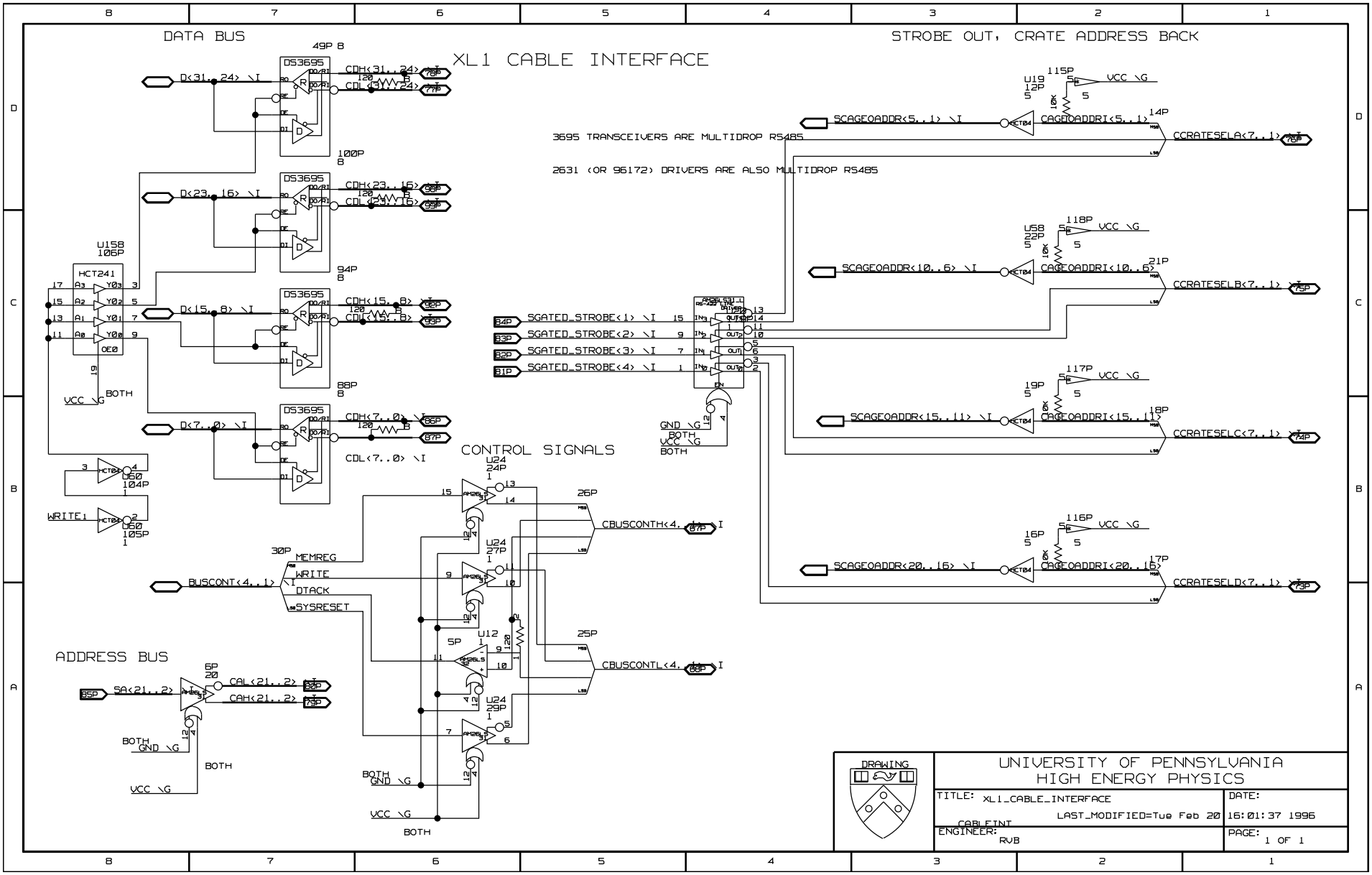
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS

TITLE: ADDRESS_MATCH ADDRMTCH
LAST_MODIFIED=Wed Jan 31 17:47:34 1996

DATE:

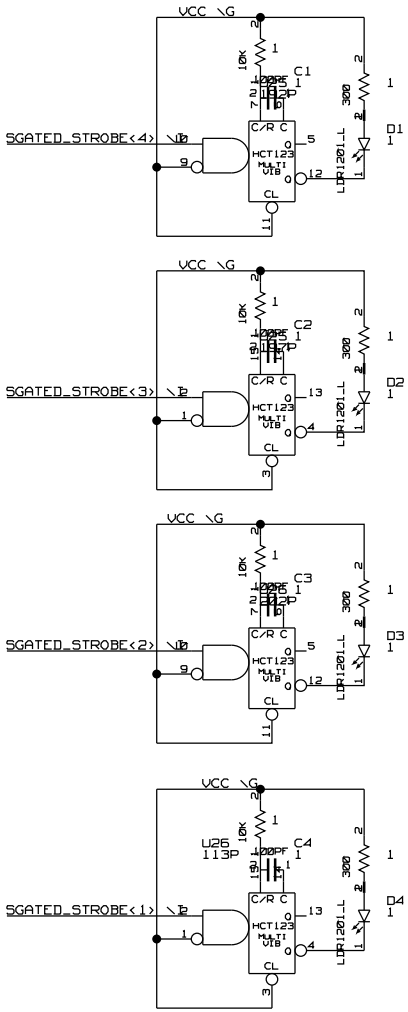
ENGINEER: RVB

PAGE: 1 OF 1

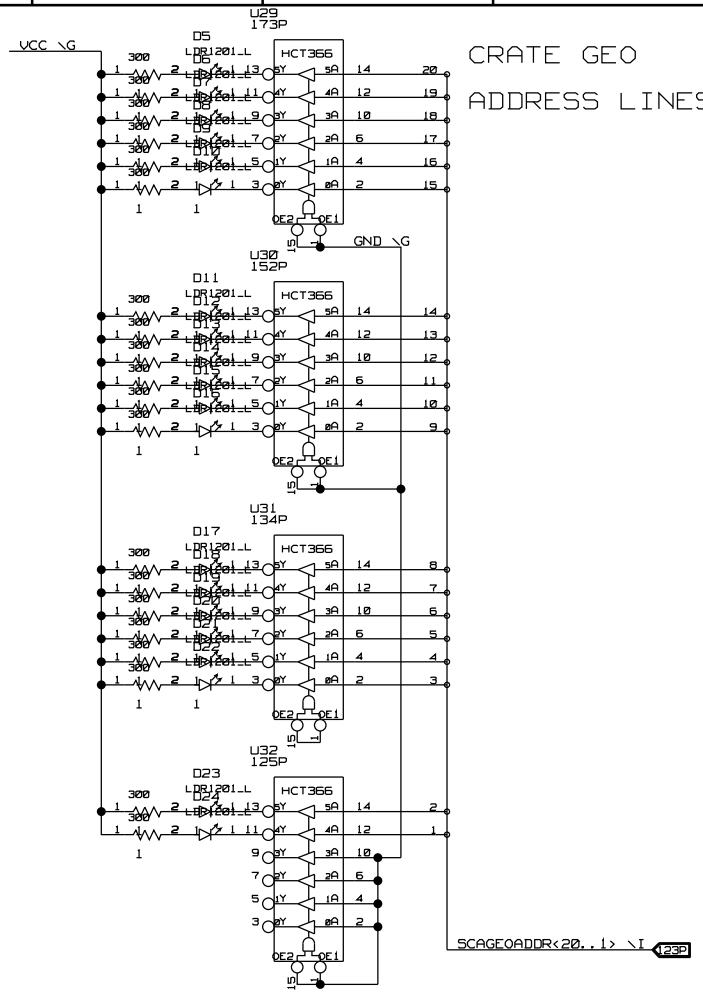

DATA BUS
XL1 CABLE INTERFACE
STROBE OUT, CRATE ADDRESS BACK
3695 TRANSCEIVERS ARE MULTIDROP RS485
2631 (OR 96172) DRIVERS ARE ALSO MULTIDROP RS485
CONTROL SIGNALS
ADDRESS BUS
DS3695
HCT241
U158
106P
D<31..24> \I
D<23..16> \I
D<15..8> \I
D<7..0> \I
CDH<31..24>
CDL<31..24>
CDH<23..16>
CDL<23..16>
CDH<15..8>
CDL<15..8>
CDH<7..0> \I
CDL<7..0> \I
SGATED_STROBE<1> \I
SGATED_STROBE<2> \I
SGATED_STROBE<3> \I
SGATED_STROBE<4> \I
SCAGEOADDR<5..1> \I
SCAGEOADDR<10..6> \I
SCAGEOADDR<15..11> \I
SCAGEOADDR<20..16> \I
CAGEOADDRI<5..1>
CAGEOADDRI<10..6>
CAGEOADDRI<15..11>
CAGEOADDRI<20..16>
CCRATESELA<7..1>
CCRATESELB<7..1>
CCRATESELC<7..1>
CCRATESELD<7..1>
CBUSCONTH<4..1>
CBUSCONTL<4..1>
BUSCONT<4..1>
MEMREG
WRITE
DTACK
SYSRESET
SA<21..2>
CAL<21..2>
CAH<21..2>
WRITE1
VCC \G
GND \G
BOTH
DRAWING
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE: XL1_CABLE_INTERFACE
LAST_MODIFIED=Tue Feb 20
CABLEINT
DATE: 16:01:37 1996
ENGINEER: RVB
PAGE: 1 OF 1

XL1 LED INDICATORS

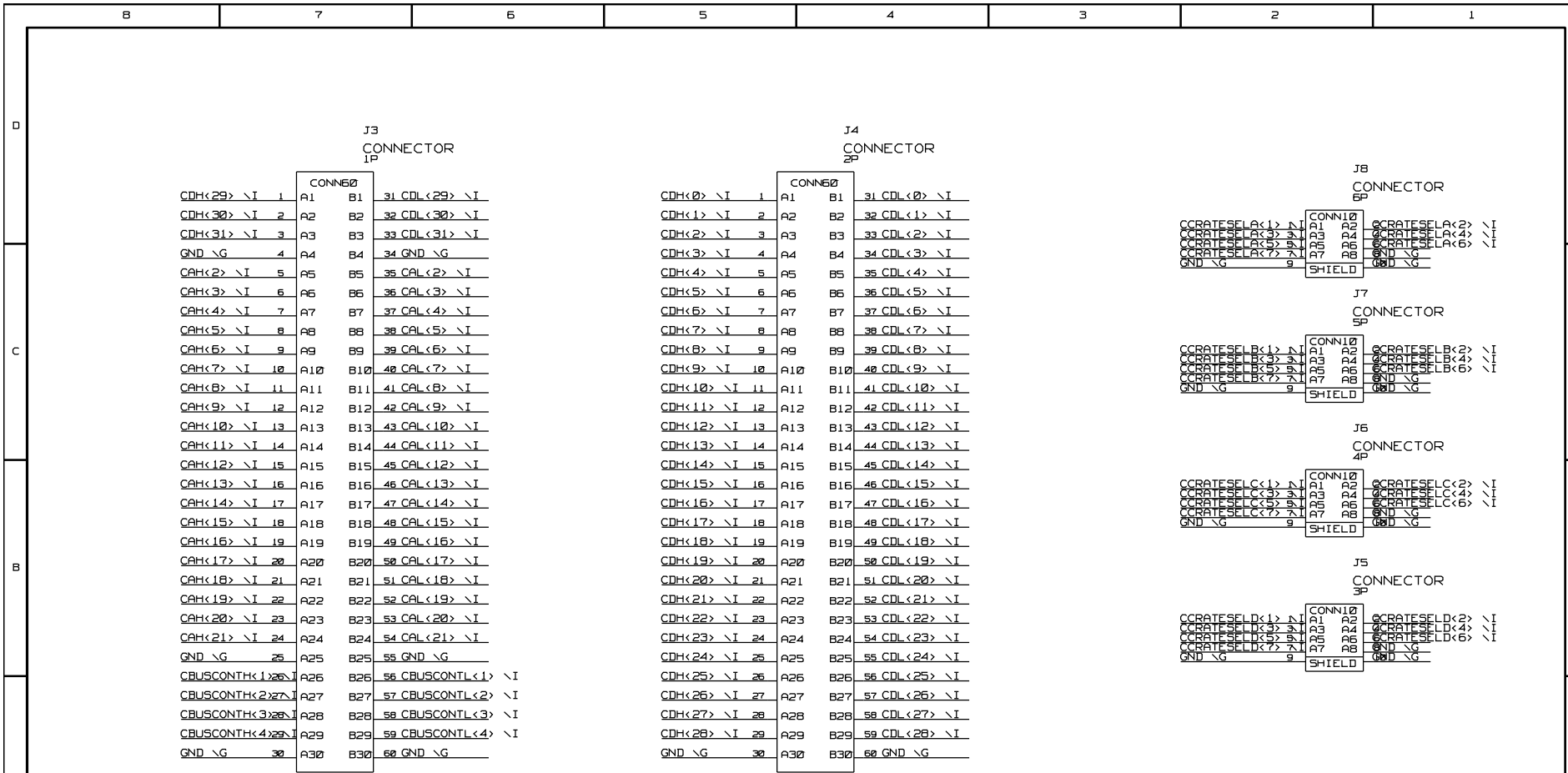
GATED STROBE LEDS



CRATE GEO ADDRESS LINES



DRAWING	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
	TITLE: XL1_CABLE_INTERFACE LAST_MODIFIED=Tue Feb 20 16:01:41 1996 CABLEINT	DATE:
	ENGINEER: RVB	PAGE: 2 OF 2

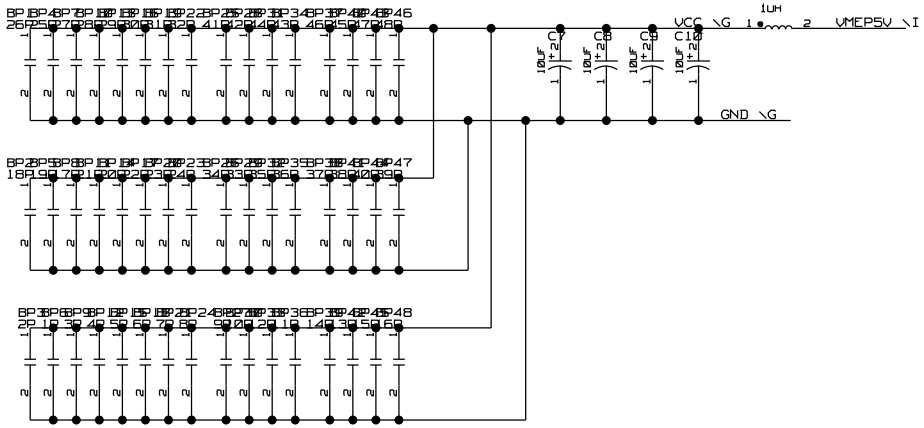

J3
CONNECTOR
1P
CONN60
CDH<29> \I 1 A1 B1 31 CDL<29> \I
CDH<30> \I 2 A2 B2 32 CDL<30> \I
CDH<31> \I 3 A3 B3 33 CDL<31> \I
GND \G 4 A4 B4 34 GND \G
CAH<2> \I 5 A5 B5 35 CAL<2> \I
CAH<3> \I 6 A6 B6 36 CAL<3> \I
CAH<4> \I 7 A7 B7 37 CAL<4> \I
CAH<5> \I 8 A8 B8 38 CAL<5> \I
CAH<6> \I 9 A9 B9 39 CAL<6> \I
CAH<7> \I 10 A10 B10 40 CAL<7> \I
CAH<8> \I 11 A11 B11 41 CAL<8> \I
CAH<9> \I 12 A12 B12 42 CAL<9> \I
CAH<10> \I 13 A13 B13 43 CAL<10> \I
CAH<11> \I 14 A14 B14 44 CAL<11> \I
CAH<12> \I 15 A15 B15 45 CAL<12> \I
CAH<13> \I 16 A16 B16 46 CAL<13> \I
CAH<14> \I 17 A17 B17 47 CAL<14> \I
CAH<15> \I 18 A18 B18 48 CAL<15> \I
CAH<16> \I 19 A19 B19 49 CAL<16> \I
CAH<17> \I 20 A20 B20 50 CAL<17> \I
CAH<18> \I 21 A21 B21 51 CAL<18> \I
CAH<19> \I 22 A22 B22 52 CAL<19> \I
CAH<20> \I 23 A23 B23 53 CAL<20> \I
CAH<21> \I 24 A24 B24 54 CAL<21> \I
GND \G 25 A25 B25 55 GND \G
CBUSCONTH<1> \I 26 A26 B26 56 CBUSCONTL<1> \I
CBUSCONTH<2> \I 27 A27 B27 57 CBUSCONTL<2> \I
CBUSCONTH<3> \I 28 A28 B28 58 CBUSCONTL<3> \I
CBUSCONTH<4> \I 29 A29 B29 59 CBUSCONTL<4> \I
GND \G 30 A30 B30 60 GND \G
J4
CONNECTOR
2P
CONN60
CDH<0> \I 1 A1 B1 31 CDL<0> \I
CDH<1> \I 2 A2 B2 32 CDL<1> \I
CDH<2> \I 3 A3 B3 33 CDL<2> \I
CDH<3> \I 4 A4 B4 34 CDL<3> \I
CDH<4> \I 5 A5 B5 35 CDL<4> \I
CDH<5> \I 6 A6 B6 36 CDL<5> \I
CDH<6> \I 7 A7 B7 37 CDL<6> \I
CDH<7> \I 8 A8 B8 38 CDL<7> \I
CDH<8> \I 9 A9 B9 39 CDL<8> \I
CDH<9> \I 10 A10 B10 40 CDL<9> \I
CDH<10> \I 11 A11 B11 41 CDL<10> \I
CDH<11> \I 12 A12 B12 42 CDL<11> \I
CDH<12> \I 13 A13 B13 43 CDL<12> \I
CDH<13> \I 14 A14 B14 44 CDL<13> \I
CDH<14> \I 15 A15 B15 45 CDL<14> \I
CDH<15> \I 16 A16 B16 46 CDL<15> \I
CDH<16> \I 17 A17 B17 47 CDL<16> \I
CDH<17> \I 18 A18 B18 48 CDL<17> \I
CDH<18> \I 19 A19 B19 49 CDL<18> \I
CDH<19> \I 20 A20 B20 50 CDL<19> \I
CDH<20> \I 21 A21 B21 51 CDL<20> \I
CDH<21> \I 22 A22 B22 52 CDL<21> \I
CDH<22> \I 23 A23 B23 53 CDL<22> \I
CDH<23> \I 24 A24 B24 54 CDL<23> \I
CDH<24> \I 25 A25 B25 55 CDL<24> \I
CDH<25> \I 26 A26 B26 56 CDL<25> \I
CDH<26> \I 27 A27 B27 57 CDL<26> \I
CDH<27> \I 28 A28 B28 58 CDL<27> \I
CDH<28> \I 29 A29 B29 59 CDL<28> \I
GND \G 30 A30 B30 60 GND \G
J8
CONNECTOR
6P
CONN10
CCRATESELA<1> \I A1 A2 CCRATESELA<2> \I
CCRATESELA<3> \I A3 A4 CCRATESELA<4> \I
CCRATESELA<5> \I A5 A6 CCRATESELA<6> \I
CCRATESELA<7> \I A7 A8 GND \G
GND \G 9 SHIELD GND \G
J7
CONNECTOR
5P
CONN10
CCRATESELB<1> \I A1 A2 CCRATESELB<2> \I
CCRATESELB<3> \I A3 A4 CCRATESELB<4> \I
CCRATESELB<5> \I A5 A6 CCRATESELB<6> \I
CCRATESELB<7> \I A7 A8 GND \G
GND \G 9 SHIELD GND \G
J6
CONNECTOR
4P
CONN10
CCRATESELC<1> \I A1 A2 CCRATESELC<2> \I
CCRATESELC<3> \I A3 A4 CCRATESELC<4> \I
CCRATESELC<5> \I A5 A6 CCRATESELC<6> \I
CCRATESELC<7> \I A7 A8 GND \G
GND \G 9 SHIELD GND \G
J5
CONNECTOR
3P
CONN10
CCRATESELD<1> \I A1 A2 CCRATESELD<2> \I
CCRATESELD<3> \I A3 A4 CCRATESELD<4> \I
CCRATESELD<5> \I A5 A6 CCRATESELD<6> \I
CCRATESELD<7> \I A7 A8 GND \G
GND \G 9 SHIELD GND \G
DRAWING
XL1CABCONN
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
TITLE: XL1_CABLE_CONNECTOR
LAST_MODIFIED=Tue Feb 20 16:01:52 1996
DATE:
ENGINEER: RVB
PAGE: 1 OF 1

FIVE VOLT POWER TREATMENT

BYPASS CAPACITORS - ABOUT 1 PER IC

INPUT INDUCTOR/FUSE

TANTALUM 10UF



DRAWING	UNIVERSITY OF PENNSYLVANIA HIGH ENERGY PHYSICS	
POWER	TITLE: POWER_IN LAST_MODIFIED=Tue Feb 20 16:01:50 1996	DATE:
	ENGINEER: RVB	PAGE: 9 OF 9