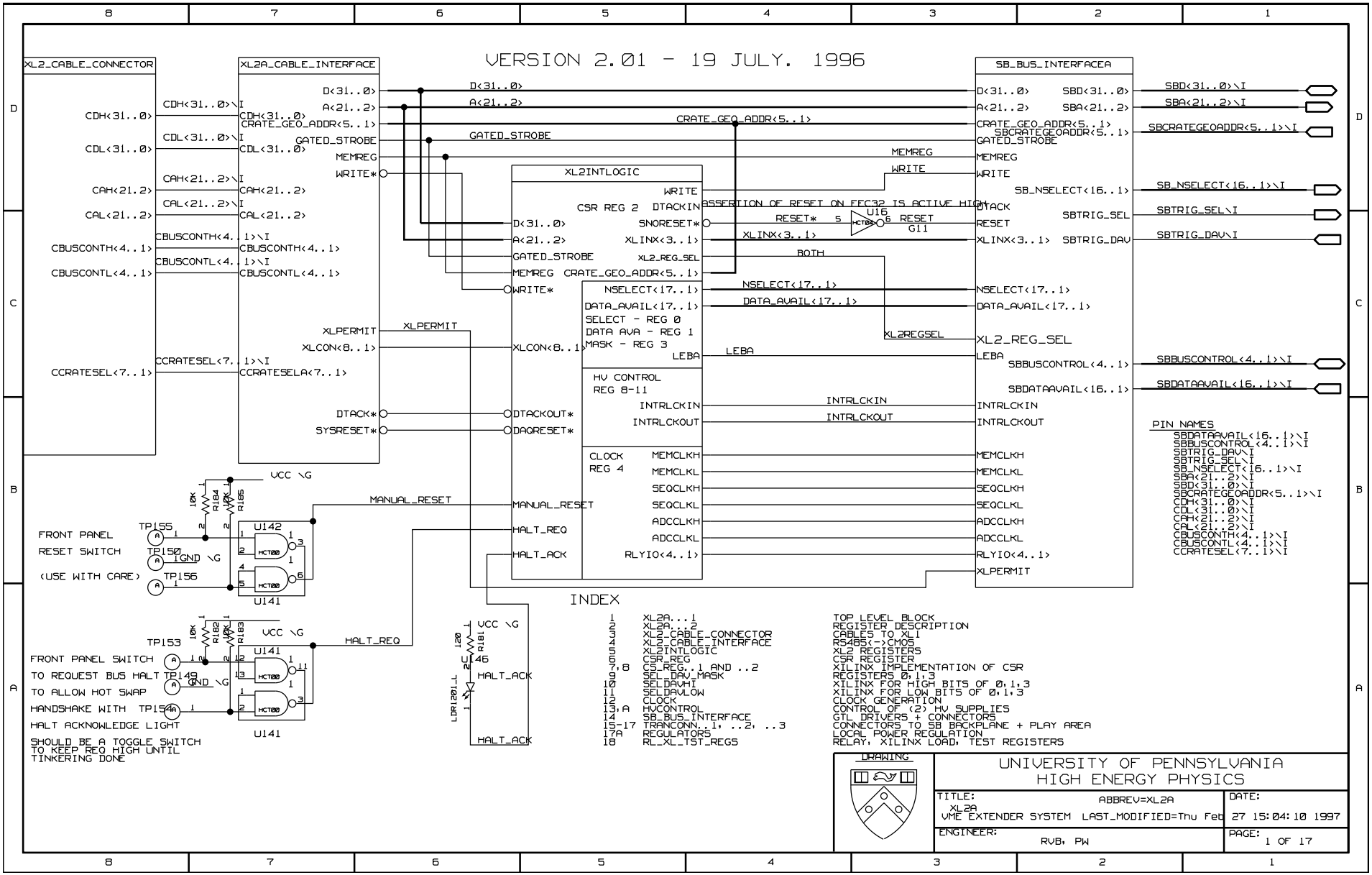
XL2 BOARD BLOCK VIEW



TRANSLATOR 2 (XL2) REGISTER DEFINITIONS

FIRST REGISTER GROUP - CRATE CONTROL

ALWAYS ENABLED - IRREGARDLESS OF STATE OF REG 0

REG 0 - SELECT REGISTER
- BITS 0..15 SELECT ANY (OR ALL) FECS 0..15
- BIT 16 SELECT TRIGGER CARD
- BIT 17 SELECT XL2 CARD

REG 1 - DATA AVAILABLE
- BITS 0..15 DATA AVAILABLE IN FEC 0..15
- BIT 16 DATA AVAILABLE IN TRIGGER CARD
- BIT 17 DATA AVAILABLE IN XL2 CARD
- BIT 30 REQUEST TO HALT BACKPLANE TRAFFIC
- BIT 31 REQUEST FLAG - OR OF BITS 0..17, 30

REG 2 - XL2 CSR
- BITS 0..4 GEOGRAPHIC CRATE ADDRESS, READ ONLY
- BIT 6 LIGHT 'HALT ACK' LIGHT
- BIT 7 CRATE RESET (OR'ED WITH SYSRESET)
- BITS 8..11 XLINX CONTROL AND LOADS
  - 8 = DONE_PROG* (R/W) (CF XILINX ACTIVE)
  - 9 = DATA IN (TO FEC XILINX) (R/W)
  - 10 = CONFIGURATION CLOCK (TO FEC XILINX) (R/W)
  - 11 = XILINX ACTIVE FLAG - HOLDS SELECT REGISTER STEADY (R/W)
- BITS 26..30 ERRORS, FROM XL2 LOGIC (TBD)
- BIT 31 ERROR FLAG

REG 3 - MASKS
- BITS 0..15 - MASK OFF DATA AVAILABLE FROM FECS 0..15

SECOND REGISTER GROUP - CLOCK, HVRELAYS, TEST

SECOND GROUP AND BEYOND REQUIRE CORRECT LOADING OF SELECT REGISTER (REG 0)

REG 4 - CLOCK CSR
- BIT 0 = SHIFT CLOCK IN FOR MEMORY CLOCK
- BIT 1 = DATA IN FOR MEMORY CLOCK
- BIT 2 = OUTPUT ENABLE FOR MEMORY CLOCK
- BIT 3 = SOFTWARE MEMORY CLOCK
- BIT 4 = SHIFT CLOCK IN FOR SEQUENCER CLOCK
- BIT 5 = DATA IN FOR SEQUENCER CLOCK
- BIT 6 = OUTPUT ENABLE FOR SEQUENCER CLOCK
- BIT 7 = SOFTWARE SEQUENCER CLOCK
- BIT 8 = SHIFT CLOCK IN FOR ADC CLOCK
- BIT 9 = DATA IN FOR ADC CLOCK
- BIT 10 = OUTPUT ENABLE FOR ADC CLOCK
- BIT 11 = SOFTWARE ADC CLOCK
- BIT 12 = SPARE
- BIT 13 = SPARE
- BIT 14 = SPARE
- BIT 15 = MASTER CLOCK ENABLE

REG 5 - HV RELAY CONTROL
- BIT 0 - RELAY CLOCK
- BIT 1 - RELAY DATA
- BIT 2 - RELAY RESET
- BIT 3 - RELAY DATA OUT
- BIT 4 - RELAY LOAD

REG 6 - XILINX UBER CONTROL AND CHECK
- BITS<8..5> - CONTROL - ENABLE XILINX LOAD IF = 0101
- BITS<4..1> - ADDRESS LINE MODIFIERS (A<21..18>)
  - A<21> = 1 AND A<20> = 0 FORCES XILINX LOAD MODE ON MB

REG 7 - GENERAL READ/WRITE/DISPLAY TEST REGISTER
- BITS<31..0> - DATA

THIRD REGISTER GROUP - HV CONTROL REGISTERS 8-11

REG 8 - HV CSR

R/W	BIT 0 SET HV SUPPLY A AC POWER ON
R	BIT 1 SPARE 1, SHOULD = 0
R	BIT 2 HV INTERLOCK (BACKPLANE) STATUS (1 = ALL BOARDS IN)
R	BITS 3..5 HV A ERROR CONDITIONS, TO BE DETERMINED
R/W	BITS 6..7 HV A CONTROL BITS, TO BE DETERMINED
R/W	BIT 16 SET HV SUPPLY B AC POWER ON
R	BIT 17 SPARE 17, SHOULD = 0
R	BITS 19..21 HV B ERROR CONDITIONS, TO BE DETERMINED
R/W	BITS 22..23 HV B CONTROL BITS, TO BE DETERMINED
R	BIT 31 ERROR FLAG

REG 9 - HV SETPOINTS
- BITS 0..11 HV A SET POINT (LSB = 1/4096TH OF FSR)
- BITS 16..27 HV B SET POINT (LSB = 1/4096TH OF FSR)

REG 10 - HV VOLTAGE READBACK
- BITS 0..11 HV A VOLTAGE (LSB = 1/4096 OF FSR)
- BITS 16..27 HV B VOLTAGE

REG 11 - HV CURRENT READBACK
- BITS 0..11 HV A CURRENT (LSB = 1/4096 OF FSR)
- BITS 16..27 HV B CURRENT

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TITLE: XL2A VME EXTENDER SYSTEM	ABBREV=XL2A LAST_MODIFIED=Wed Sep 11 17:32:45 1996
ENGINEER: RVB	PAGE: 2 OF 17
DATE:	

XL2 CABLE AND TERMINATION CONNECTORS

INPUTS

ADDRESS LINES J8 CONNECTOR

CDH<29> \I	1	A1	B1	31	CDL<29> \I
CDH<30> \I	2	A2	B2	32	CDL<30> \I
CDH<31> \I	3	A3	B3	33	CDL<31> \I
GND \G	4	A4	B4	34	GND \G
CAH<2> \I	5	A5	B5	35	CAL<2> \I
CAH<3> \I	6	A6	B6	36	CAL<3> \I
CAH<4> \I	7	A7	B7	37	CAL<4> \I
CAH<5> \I	8	A8	B8	38	CAL<5> \I
CAH<6> \I	9	A9	B9	39	CAL<6> \I
CAH<7> \I	10	A10	B10	40	CAL<7> \I
CAH<8> \I	11	A11	B11	41	CAL<8> \I
CAH<9> \I	12	A12	B12	42	CAL<9> \I
CAH<10> \I	13	A13	B13	43	CAL<10> \I
CAH<11> \I	14	A14	B14	44	CAL<11> \I
CAH<12> \I	15	A15	B15	45	CAL<12> \I
CAH<13> \I	16	A16	B16	46	CAL<13> \I
CAH<14> \I	17	A17	B17	47	CAL<14> \I
CAH<15> \I	18	A18	B18	48	CAL<15> \I
CAH<16> \I	19	A19	B19	49	CAL<16> \I
CAH<17> \I	20	A20	B20	50	CAL<17> \I
CAH<18> \I	21	A21	B21	51	CAL<18> \I
CAH<19> \I	22	A22	B22	52	CAL<19> \I
CAH<20> \I	23	A23	B23	53	CAL<20> \I
CAH<21> \I	24	A24	B24	54	CAL<21> \I
GND \G	25	A25	B25	55	GND \G
CBUSCONTH<1> \I	26	A26	B26	56	CBUSCONTL<1> \I
CBUSCONTH<2> \I	27	A27	B27	57	CBUSCONTL<2> \I
CBUSCONTH<3> \I	28	A28	B28	58	CBUSCONTL<3> \I
CBUSCONTH<4> \I	29	A29	B29	59	CBUSCONTL<4> \I
GND \G	30	A30	B30	60	GND \G

DATA LINES J4 CONNECTOR

CDH<0> \I	1	A1	B1	31	CDL<0> \I
CDH<1> \I	2	A2	B2	32	CDL<1> \I
CDH<2> \I	3	A3	B3	33	CDL<2> \I
CDH<3> \I	4	A4	B4	34	CDL<3> \I
CDH<4> \I	5	A5	B5	35	CDL<4> \I
CDH<5> \I	6	A6	B6	36	CDL<5> \I
CDH<6> \I	7	A7	B7	37	CDL<6> \I
CDH<7> \I	8	A8	B8	38	CDL<7> \I
CDH<8> \I	9	A9	B9	39	CDL<8> \I
CDH<9> \I	10	A10	B10	40	CDL<9> \I
CDH<10> \I	11	A11	B11	41	CDL<10> \I
CDH<11> \I	12	A12	B12	42	CDL<11> \I
CDH<12> \I	13	A13	B13	43	CDL<12> \I
CDH<13> \I	14	A14	B14	44	CDL<13> \I
CDH<14> \I	15	A15	B15	45	CDL<14> \I
CDH<15> \I	16	A16	B16	46	CDL<15> \I
CDH<16> \I	17	A17	B17	47	CDL<16> \I
CDH<17> \I	18	A18	B18	48	CDL<17> \I
CDH<18> \I	19	A19	B19	49	CDL<18> \I
CDH<19> \I	20	A20	B20	50	CDL<19> \I
CDH<20> \I	21	A21	B21	51	CDL<20> \I
CDH<21> \I	22	A22	B22	52	CDL<21> \I
CDH<22> \I	23	A23	B23	53	CDL<22> \I
CDH<23> \I	24	A24	B24	54	CDL<23> \I
CDH<24> \I	25	A25	B25	55	CDL<24> \I
CDH<25> \I	26	A26	B26	56	CDL<25> \I
CDH<26> \I	27	A27	B27	57	CDL<26> \I
CDH<27> \I	28	A28	B28	58	CDL<27> \I
CDH<28> \I	29	A29	B29	59	CDL<28> \I
GND \G	30	A30	B30	60	GND \G

TERMINATIONS

ADDRESS LINES J7 CONNECTOR

CDH<29> \I	1	A1	B1	31	CDL<29> \I
CDH<30> \I	2	A2	B2	32	CDL<30> \I
CDH<31> \I	3	A3	B3	33	CDL<31> \I
GND \G	4	A4	B4	34	GND \G
CAH<2> \I	5	A5	B5	35	CAL<2> \I
CAH<3> \I	6	A6	B6	36	CAL<3> \I
CAH<4> \I	7	A7	B7	37	CAL<4> \I
CAH<5> \I	8	A8	B8	38	CAL<5> \I
CAH<6> \I	9	A9	B9	39	CAL<6> \I
CAH<7> \I	10	A10	B10	40	CAL<7> \I
CAH<8> \I	11	A11	B11	41	CAL<8> \I
CAH<9> \I	12	A12	B12	42	CAL<9> \I
CAH<10> \I	13	A13	B13	43	CAL<10> \I
CAH<11> \I	14	A14	B14	44	CAL<11> \I
CAH<12> \I	15	A15	B15	45	CAL<12> \I
CAH<13> \I	16	A16	B16	46	CAL<13> \I
CAH<14> \I	17	A17	B17	47	CAL<14> \I
CAH<15> \I	18	A18	B18	48	CAL<15> \I
CAH<16> \I	19	A19	B19	49	CAL<16> \I
CAH<17> \I	20	A20	B20	50	CAL<17> \I
CAH<18> \I	21	A21	B21	51	CAL<18> \I
CAH<19> \I	22	A22	B22	52	CAL<19> \I
CAH<20> \I	23	A23	B23	53	CAL<20> \I
CAH<21> \I	24	A24	B24	54	CAL<21> \I
GND \G	25	A25	B25	55	GND \G
CBUSCONTH<1> \I	26	A26	B26	56	CBUSCONTL<1> \I
CBUSCONTH<2> \I	27	A27	B27	57	CBUSCONTL<2> \I
CBUSCONTH<3> \I	28	A28	B28	58	CBUSCONTL<3> \I
CBUSCONTH<4> \I	29	A29	B29	59	CBUSCONTL<4> \I
VCC \G	1	300 R155 2	A30	B30	60 ||63

ATERM
ADDRESS TERM INSTALLED
LDR1201-L
GND \G

DATA LINES J5 CONNECTOR

CDH<0> \I	1	A1	B1	31	CDL<0> \I
CDH<1> \I	2	A2	B2	32	CDL<1> \I
CDH<2> \I	3	A3	B3	33	CDL<2> \I
CDH<3> \I	4	A4	B4	34	CDL<3> \I
CDH<4> \I	5	A5	B5	35	CDL<4> \I
CDH<5> \I	6	A6	B6	36	CDL<5> \I
CDH<6> \I	7	A7	B7	37	CDL<6> \I
CDH<7> \I	8	A8	B8	38	CDL<7> \I
CDH<8> \I	9	A9	B9	39	CDL<8> \I
CDH<9> \I	10	A10	B10	40	CDL<9> \I
CDH<10> \I	11	A11	B11	41	CDL<10> \I
CDH<11> \I	12	A12	B12	42	CDL<11> \I
CDH<12> \I	13	A13	B13	43	CDL<12> \I
CDH<13> \I	14	A14	B14	44	CDL<13> \I
CDH<14> \I	15	A15	B15	45	CDL<14> \I
CDH<15> \I	16	A16	B16	46	CDL<15> \I
CDH<16> \I	17	A17	B17	47	CDL<16> \I
CDH<17> \I	18	A18	B18	48	CDL<17> \I
CDH<18> \I	19	A19	B19	49	CDL<18> \I
CDH<19> \I	20	A20	B20	50	CDL<19> \I
CDH<20> \I	21	A21	B21	51	CDL<20> \I
CDH<21> \I	22	A22	B22	52	CDL<21> \I
CDH<22> \I	23	A23	B23	53	CDL<22> \I
CDH<23> \I	24	A24	B24	54	CDL<23> \I
CDH<24> \I	25	A25	B25	55	CDL<24> \I
CDH<25> \I	26	A26	B26	56	CDL<25> \I
CDH<26> \I	27	A27	B27	57	CDL<26> \I
CDH<27> \I	28	A28	B28	58	CDL<27> \I
CDH<28> \I	29	A29	B29	59	CDL<28> \I
VCC \G	1	300 R124 2	A30	B30	60 ||62

DTERM
GND \G
LDR1201-L

DATA TERM INSTALLED

CRATE ADDRESS AND GATED STROBE J9

CCRATESEL<1> \I	1	P1	P2	2	CCRATESEL<2> \I
CCRATESEL<3> \I	3	P3	P4	4	CCRATESEL<4> \I
CCRATESEL<5> \I	5	P5	P6	6	CCRATESEL<6> \I
CCRATESEL<7> \I	7	P7	P8	8	GND \G
GND \G	9	P9	P10	10	GND \G

CONN10
SHIELD

DRAWING
XL1CABCONN

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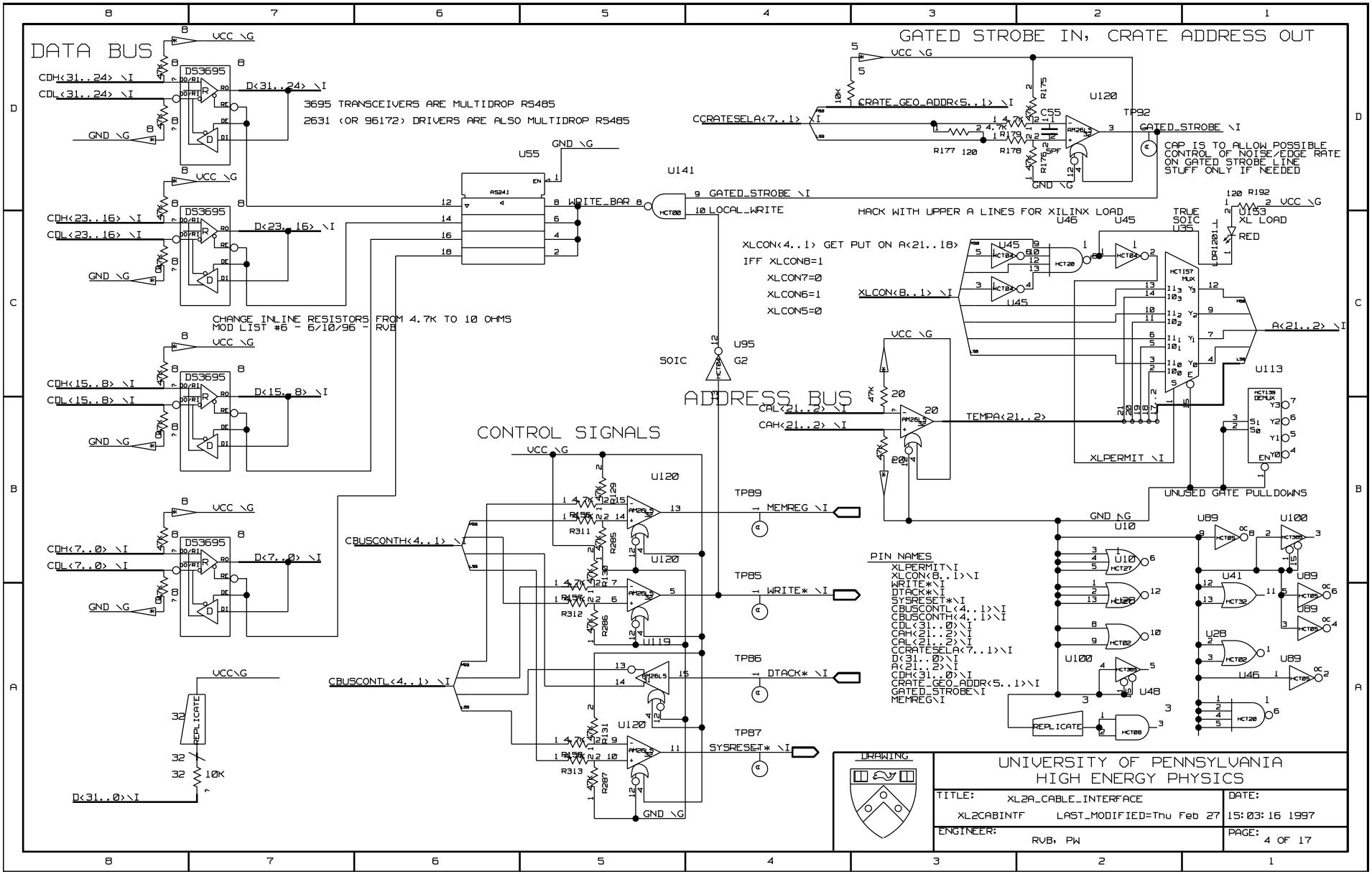
TITLE: XL2_CABLE_CONNECTOR
LAST_MODIFIED=Thu Feb 27 15:03:11 1997

DATE:

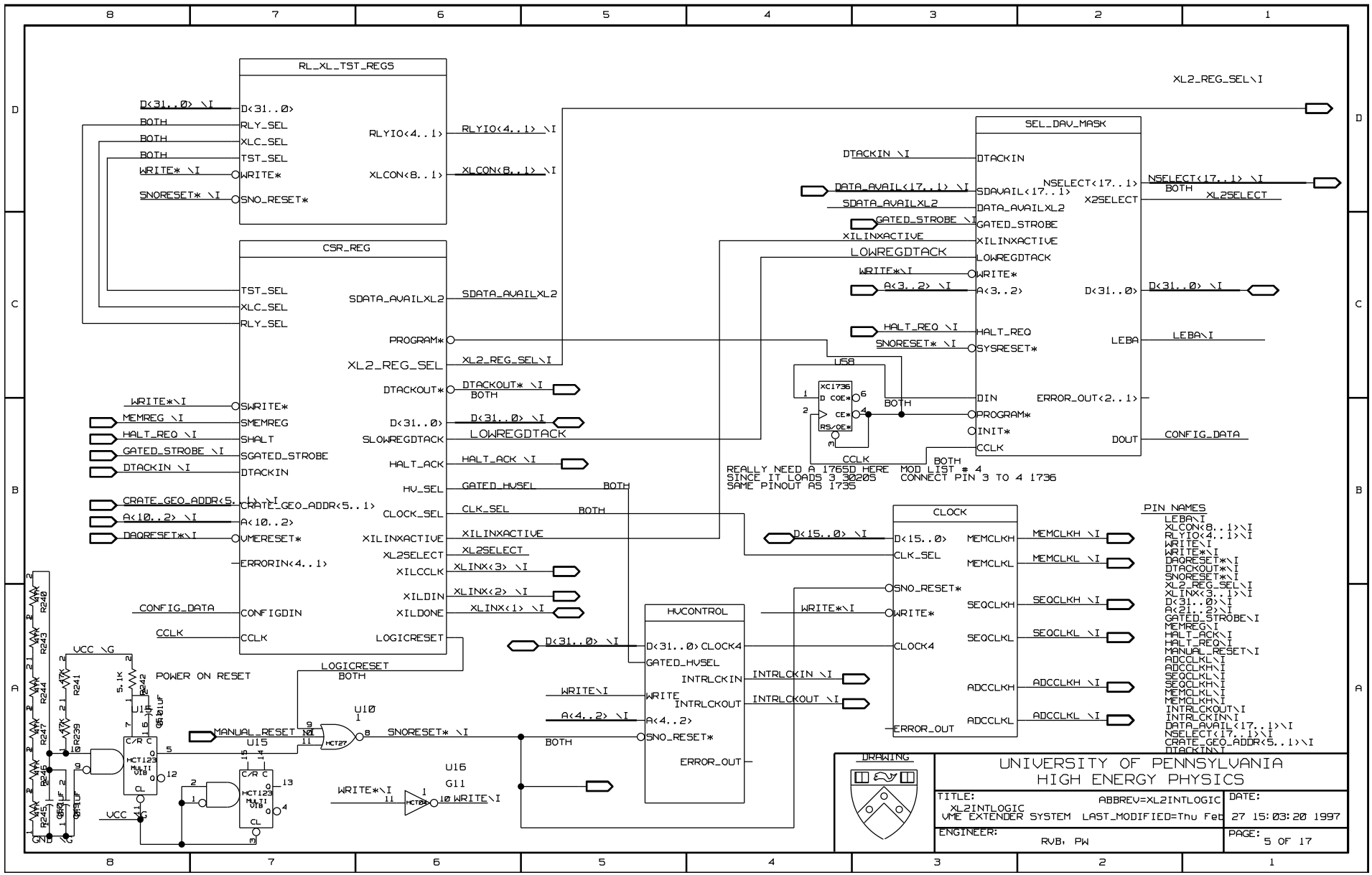
ENGINEER: RVB

PAGE: 3 OF 17

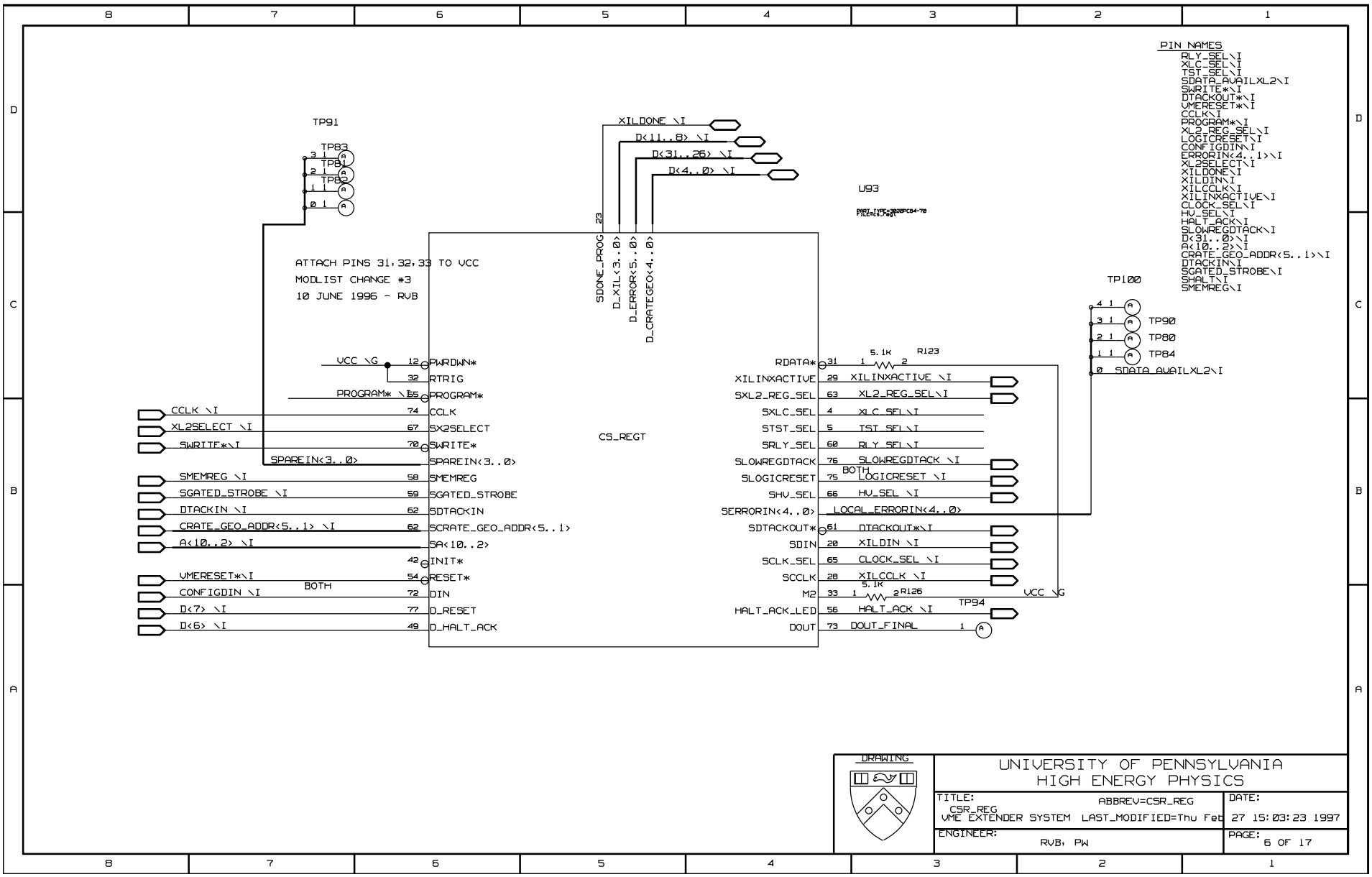
XL2 CABLE INTERFACE



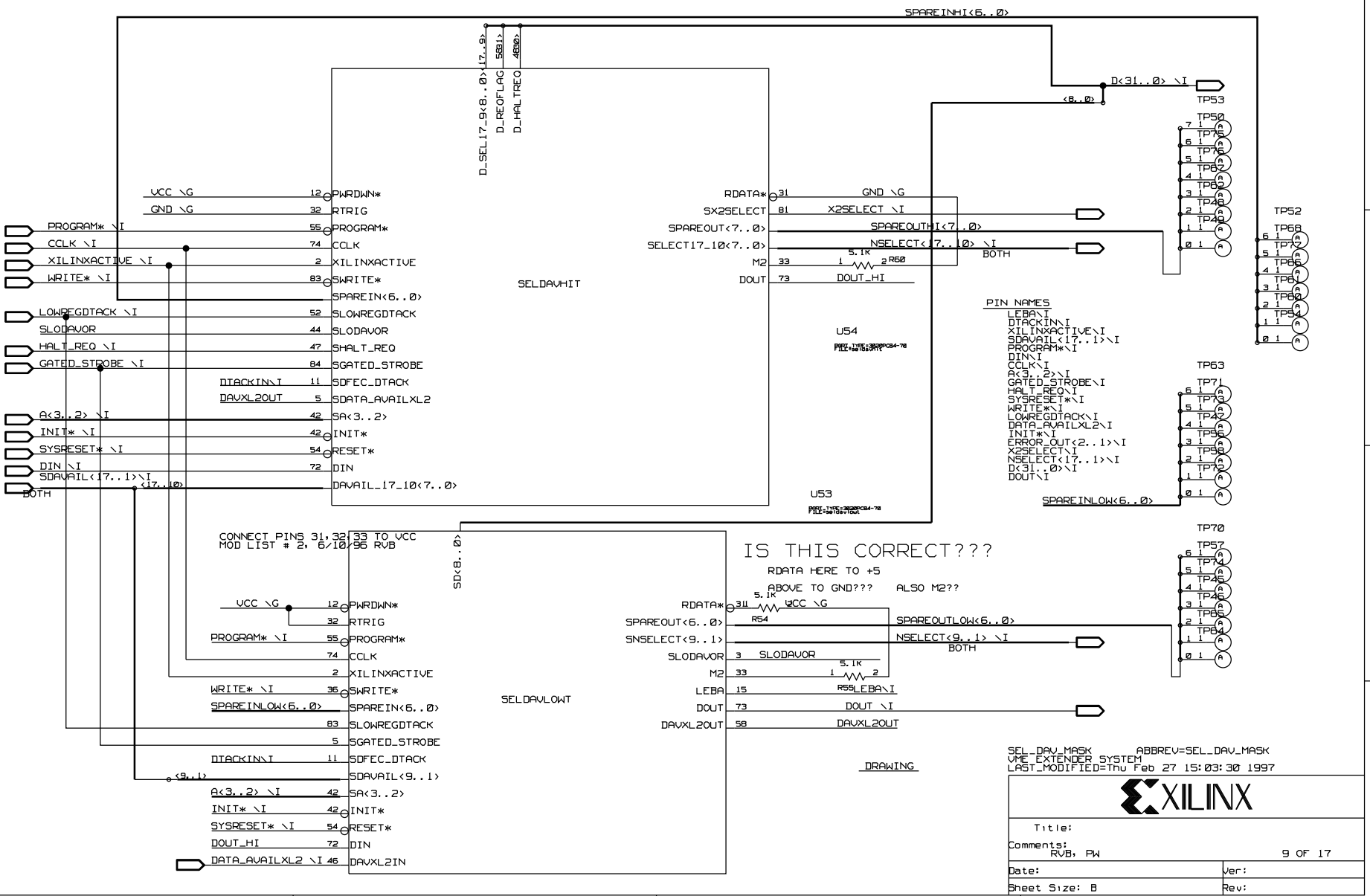
XL2 INTERNAL LOGIC



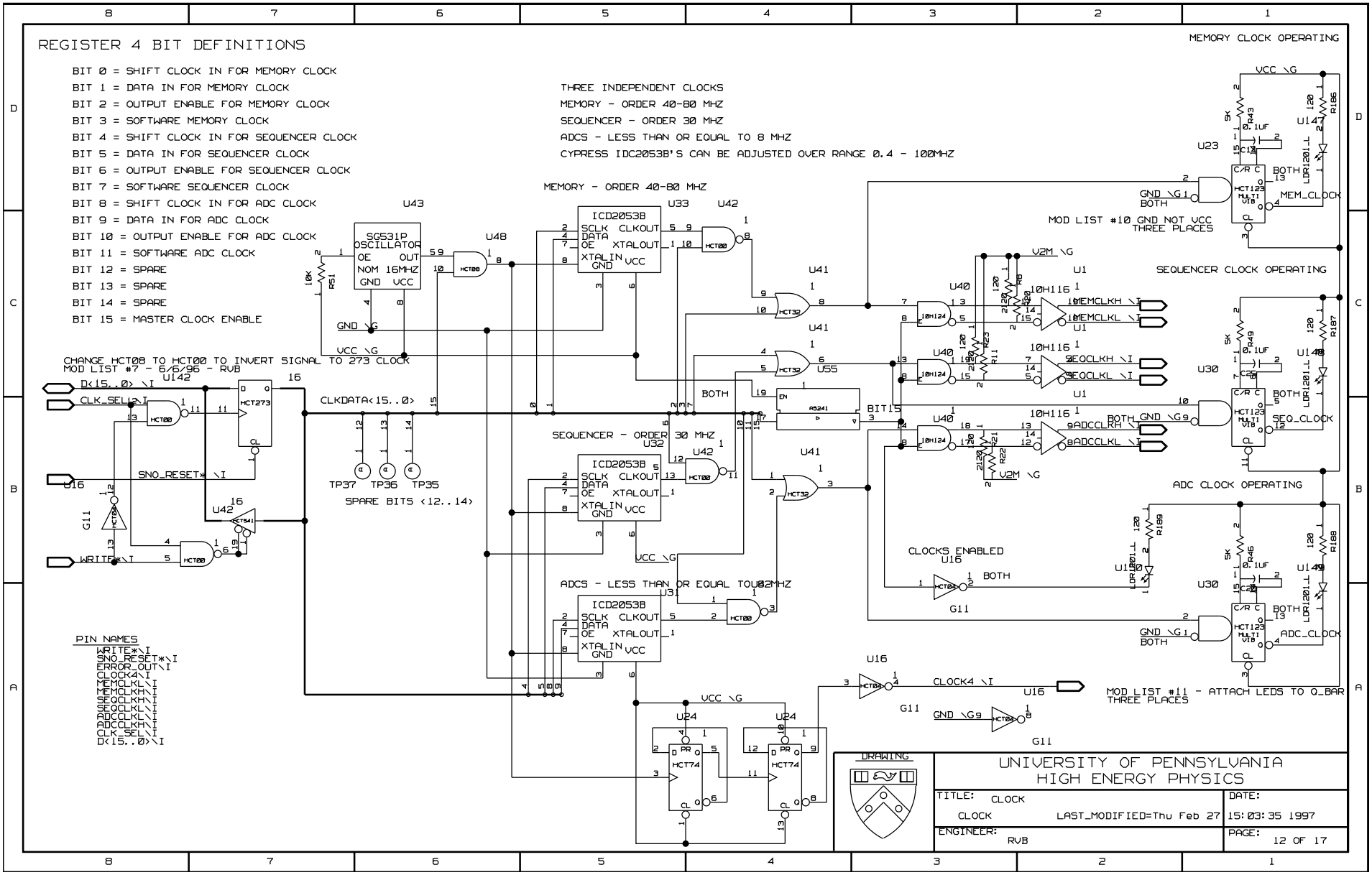
CONTROL AND STATUS REGISTER



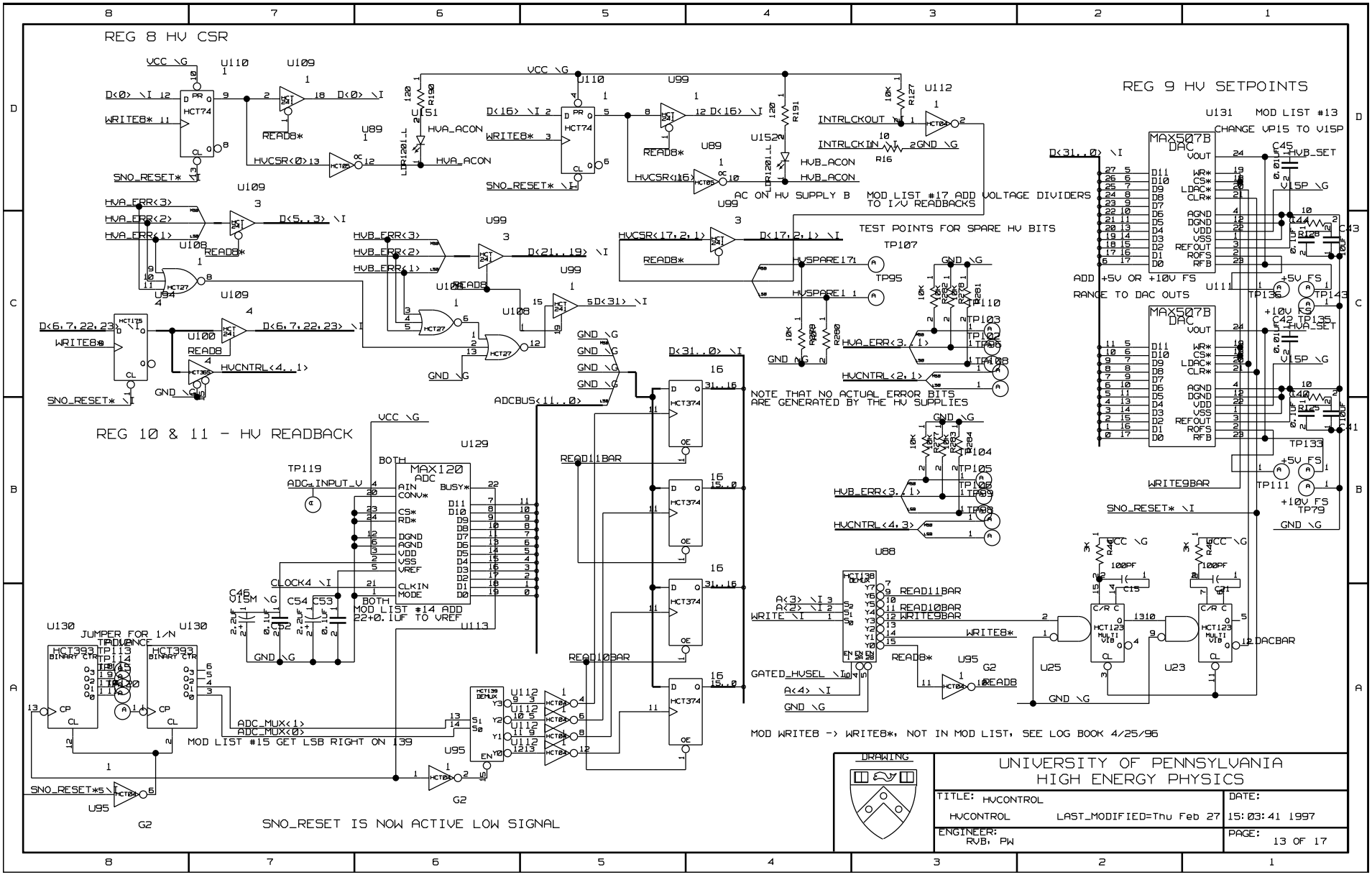
SELECT, DATA AVAILABLE AND MASK REGISTERS



REGISTER 4 - CLOCK



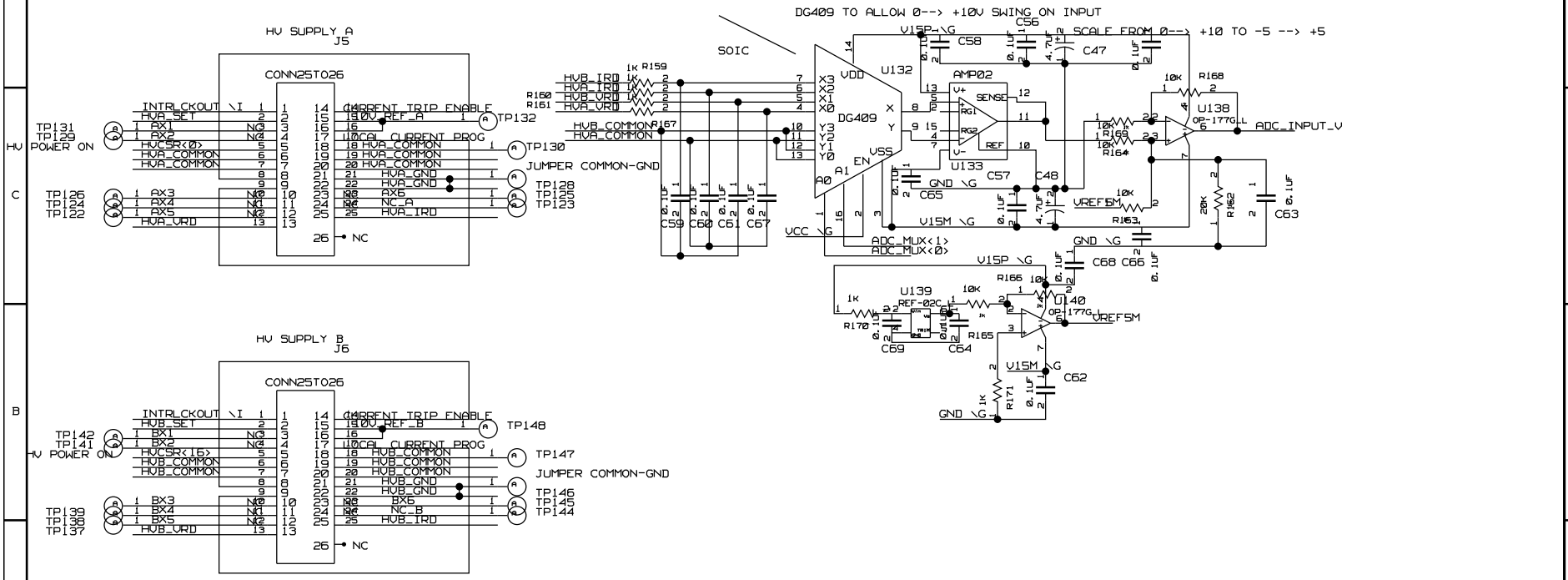
HV CONTROL AND READBACK - MODS TO V2.0



HV CONTROL AND READBACK - MODS TO V2.0

GLASSMAN MODEL MR CONNECTIONS AND SCALING C70

CAREFUL OF THIS PART - CHECK PHYSICAL AND LOGICAL DESCRIPTION
VS. DATA BOOK - ALSO NEED TO FIND AVAILABILITY...



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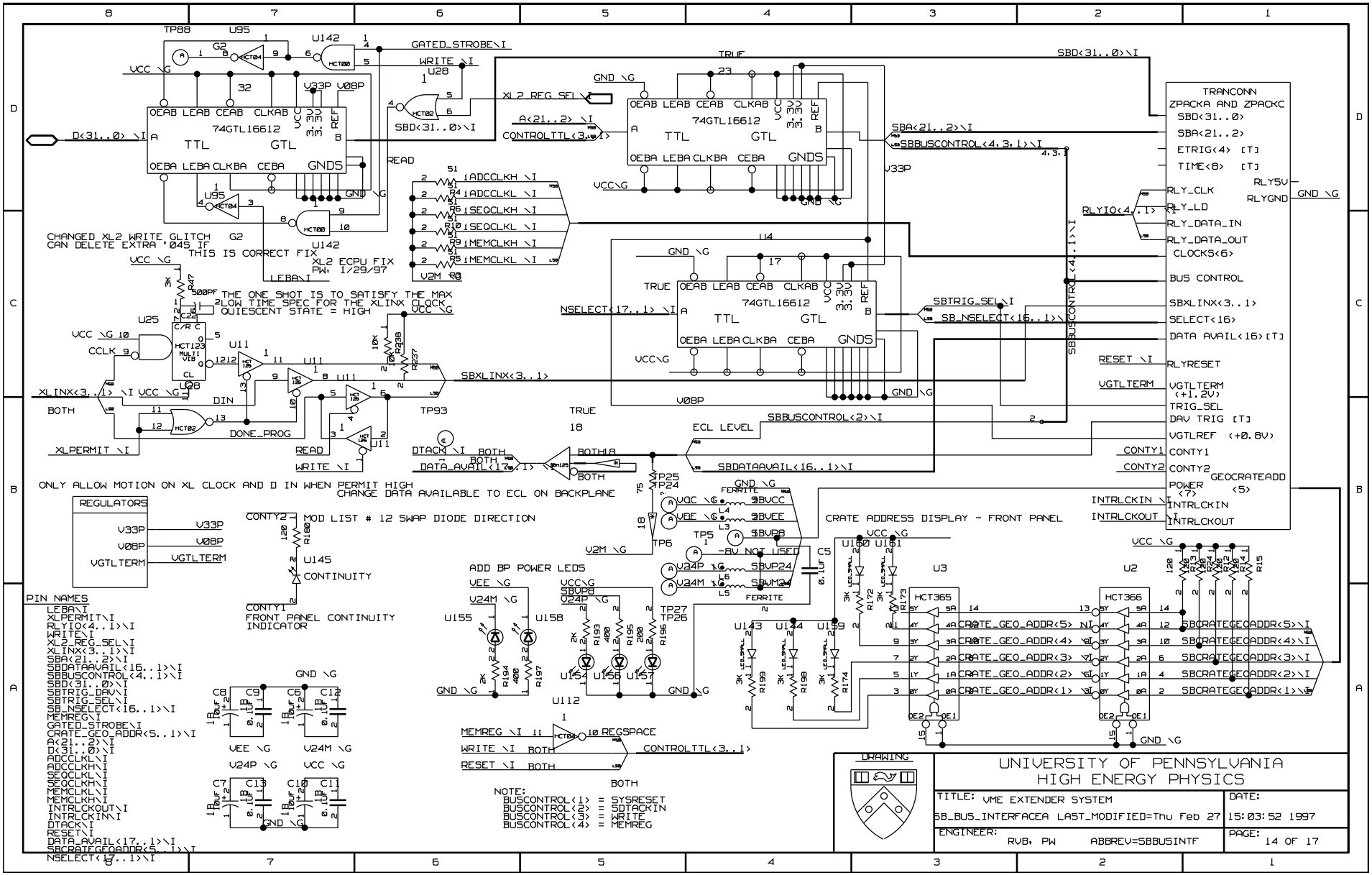
TITLE: HVCONTROL HVCONTROL LAST_MODIFIED=Thu Feb 27	DATE: 15:03:46 1997
ENGINEER: RVB, PW	PAGE: 13B OF 17

SB BUS INTERFACEA



TRANCONN PAGE 1

SNOBUS PIN ARRANGEMENT - TRANSLATOR STATION

REVISED VERSION WITH:
NO MORE THAN 4 BUS LINES PER ROW
VM8 ON C4, C5 PINS
SEPARATE ROWS FOR VP24, VM24
ADJUSTED TO ALLOW FOR PADDLE CARD ORIENTATION
CORRECTED VP8 PIN IN C ROW

TRANSLATOR VIEW
TRANSLATOR TERMINATES THE TRIGGER AND TIMING BUSSES
TRANSLATOR DOES HAVE 17 SELECT LINES
NAMING: TOP SIGNALS END IN T, BOTTOM IN B
SB PREFIX = SNOBUS - BACKPLANE SIGNALS

HIGH/LOW TRUE FINAL OR PENULTIMATE H OR L

CONN165

A		B		C		D		E	
A1	1 SBGEOCA<1> \I	B1	34 SBGEOCA<2> \I	C1	67 SBGEOCA<3> \I	D1	100 SBGEOCA<4> \I	E1	133 CONTY1 \I
A2	2 SBESUMLB	B2	35 GND \G	C2	68 SBESUMHB	D2	101 SBGEOCA<5> \I	E2	134 GND \G
A3	3 GND \G	B3	36 GND \G	C3	69 GND \G	D3	102 GND \G	E3	135 GND \G
A4	4 SBGLTRH	B4	37 SBGLTRL	C4	70 VM8	D4	103 SBTESTTH	E4	136 SBTESTTL
A5	5 SBSYNCLRH	B5	38 SBSYNCLRL	C5	71 VM8	D5	104 SBSYNCLR24H	E5	137 SBSYNCLR24L
A6	6 GND \G	B6	39 GND \G	C6	72 GND \G	D6	105 GND \G	E6	138 GND \G
A7	7 GND \G	B7	40 SBA<2> \I	C7	73 SBA<3> \I	D7	106 SBA<4> \I	E7	139 SBA<5> \I
A8	8 SBA<6> \I	B8	41 GND \G	C8	74 SBA<7> \I	D8	107 SBA<8> \I	E8	140 SBA<9> \I
A9	9 SBA<10> \I	B9	42 SBA<11> \I	C9	75 GND \G	D9	108 SBA<12> \I	E9	141 SBA<13> \I
A10	10 SBA<14> \I	B10	43 SBA<15> \I	C10	76 SBA<16> \I	D10	109 GND \G	E10	142 SBA<17> \I
A11	11 SBA<18> \I	B11	44 SBA<19> \I	C11	77 SBA<20> \I	D11	110 SBA<21> \I	E11	143 GND \G
A12	12 GND \G	B12	45 SBD<0> \I	C12	78 SBD<1> \I	D12	111 SBD<2> \I	E12	144 SBD<3> \I
A13	13 SBD<4> \I	B13	46 SBD<5> \I	C13	79 SBD<6> \I	D13	112 GND \G	E13	145 SBD<7> \I
A14	14 SBD<8> \I	B14	47 SBD<9> \I	C14	80 GND \G	D14	113 SBD<10> \I	E14	146 SBD<11> \I
A15	15 SBD<12> \I	B15	48 GND \G	C15	81 SBD<13> \I	D15	114 SBD<14> \I	E15	147 SBD<15> \I
A16	16 GND \G	B16	49 SBD<16> \I	C16	82 SBD<17> \I	D16	115 SBD<18> \I	E16	148 SBD<19> \I
A17	17 SBD<20> \I	B17	50 SBD<21> \I	C17	83 SBD<22> \I	D17	116 SBD<23> \I	E17	149 GND \G
A18	18 SBD<24> \I	B18	51 SBD<25> \I	C18	84 SBD<26> \I	D18	117 GND \G	E18	150 SBD<27> \I
A19	19 SBD<28> \I	B19	52 SBD<29> \I	C19	85 GND \G	D19	118 SBD<30> \I	E19	151 SBD<31> \I
A20	20 SBREGSPACE	B20	53 GND \G	C20	86 VM24	D20	119 VM24	E20	152 SBRESET
A21	21 GND \G	B21	54 SBDTACK	C21	87 SBWRITE	D21	120 VGTLREF \I	E21	153 GND \G
A22	22 VP24	B22	55 VP24	C22	88 GND \G	D22	121 GND \G	E22	154 SBDONE_PROGXL
A23	23 SBDINXL	B23	56 GND \G	C23	89 SBCLKXL	D23	122 GND \G	E23	155 GND \G
A24	24 VP8	B24	57 VP8	C24	90 VP8	D24	123 VP8	E24	156 VP8
A25	25 GND \G	B25	58 GND \G	C25	91 GND \G	D25	124 GND \G	E25	157 GND \G
A26	26 VP5	B26	59 VP5	C26	92 VP5	D26	125 VP5	E26	158 VP5
A27	27 VP5	B27	60 VP5	C27	93 VP5	D27	126 VP5	E27	159 VP5
A28	28 SBCLKADH	B28	61 SBCLKADL	C28	94 GND \G	D28	127 SBCLKMEMH	E28	160 SBCLKMEML
A29	29 SBCLKSQH	B29	62 SBCLKSQL	C29	95 GND \G	D29	128 GND \G	E29	161 GND \G
A30	30 VM5	B30	63 VM5	C30	96 VM5	D30	129 VM5	E30	162 VM5
A31	31 VM5	B31	64 VM5	C31	97 VM5	D31	130 VM5	E31	163 VM5
A32	32 SBESUMLT	B32	65 GND \G	C32	98 SBESUMHT	D32	131 GND \G	E32	164 GND \G
A33	33 GND \G	B33	66 GND \G	C33	99 GND \G	D33	132 GND \G	E33	165 CONTY2 \I

J2

TOP TRIGGER	SBREGSPACE SBWRITE SBDTACK SBRESET	SBBUSCONTROL<4..1> \I
GND LINE		
TIMING		
GEOGRAPHIC ADDRESS	SBSYNCLRH SBSYNCLRL SBGLTRH SBGLTRL SBTESTTH SBTESTTL SBSYNCLR24H SBSYNCLR24L	SBTIMEBUS<8..1> \I
BUS ADDRESS		
BUS DATA	SBCLKXL SBDINXL SBDONE_PROGXL	SBXLINX<3..1> \I
BUS CONTROL	GND \G VP5 VM5 VP8 VM8 VP24 VM24	POWER<7..1> \I
XILINX LOAD PINS		
MAIN POWER DIST		
CLOCK	SBCLKADH SBCLKADL SBCLKSQH SBCLKSQL SBCLKMEMH SBCLKMEML	SBCLOCKS<6..1> \I
GND LINE	SBESUMLT SBESUMHT SBESUMLB SBESUMHB	SBETRIG<4..1> \I
BOTTOM TRIGGER		

THREE CLOCK VERSION -
SBCLKAD FOR ADCS
SBCKLSQ FOR SEQUENCER
SBCLKMEM FOR MEMORY

CONTY1 AND CONTY2 ARE CONNECTOR CONTINUITY TEST PINS

POWER IS:
+24V, -24V - ADCS, SOME OP AMPS/DACS, REFERENCES, TRIGGER
+8 FOR BIPOLAR, DACS, -8 FOR DACS
+5 FOR CMOS AND GENERAL LOGIC
-5.2 FOR ECL AND BIPOLAR

REFERENCES ARE:
VTRIGREF FOR CURRENT SUM BASE REFERENCES
VGTLREF FOR GTL TRANSCEIVER TERMINATIONS

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TITLE: TRANCONN
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ABBREV=TRANCONN
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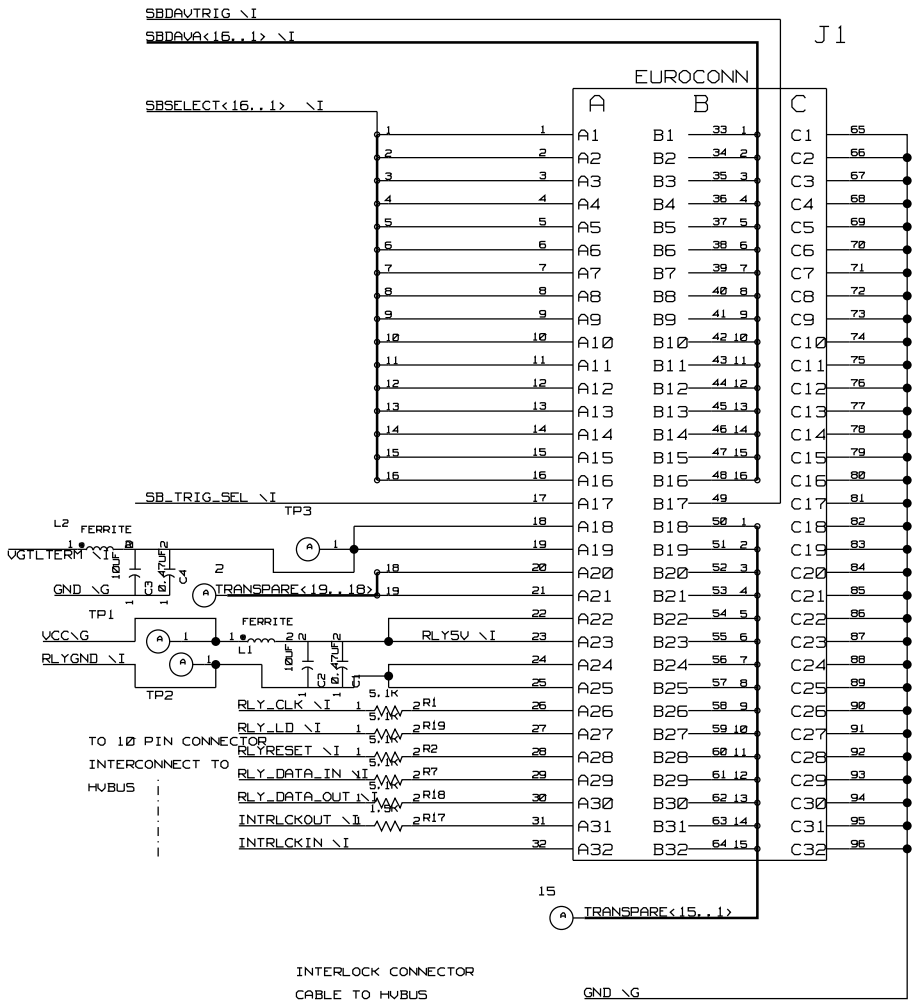
TRANSLATOR J3 CONNECTOR



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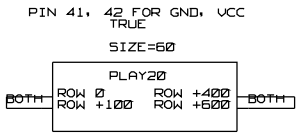
ENGINEER: RVB	TRANCONN	PAGE: 16 OF 17

PLAY AREA

ROOM FOR UP TO SIX 20 PIN DIPS.



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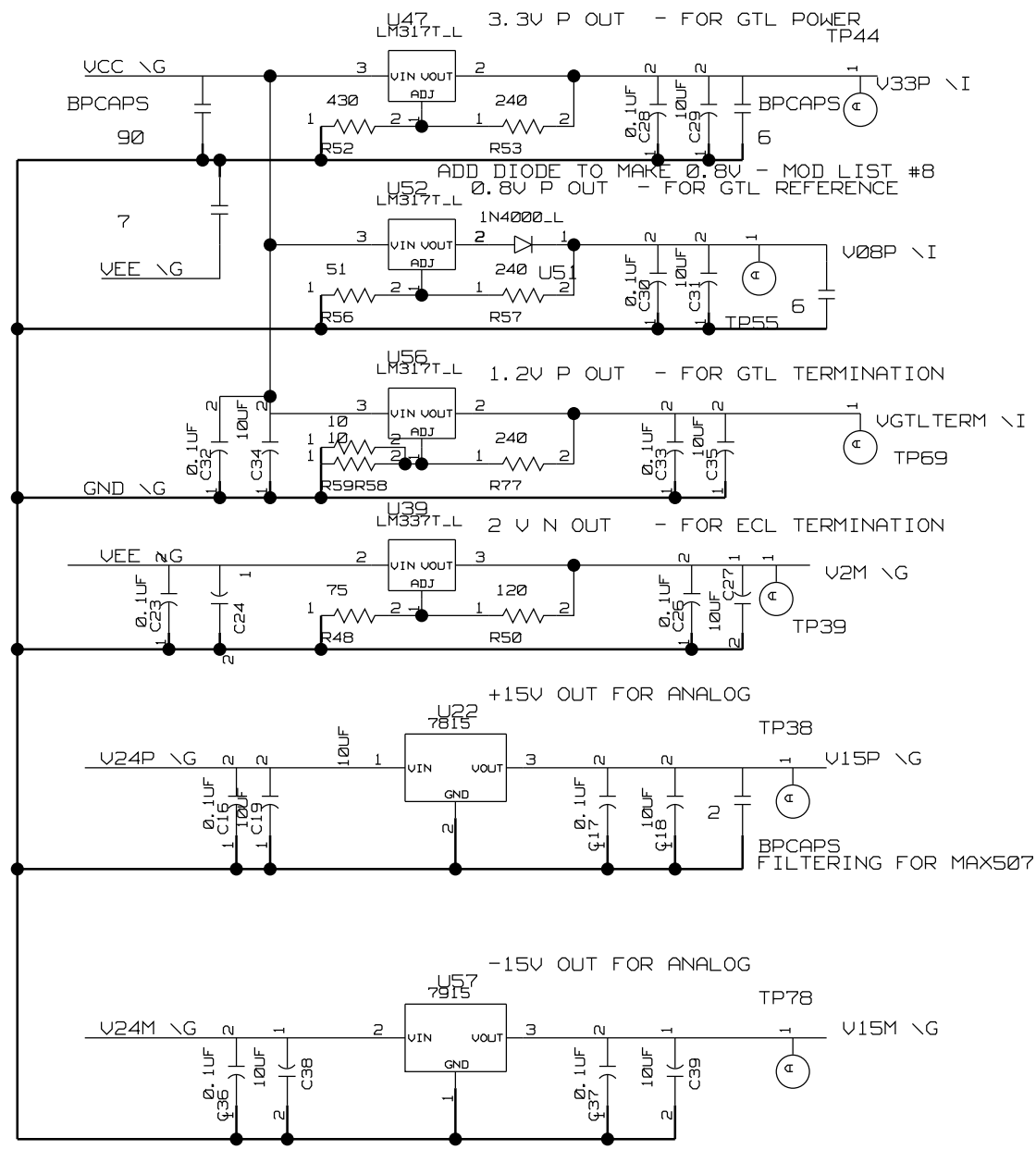
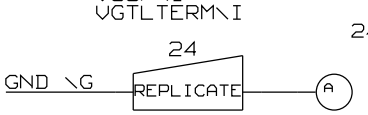
TITLE: TRANCONN LAST_MODIFIED=Thu Feb 27	DATE: 15:04:03 1997
ENGINEER: RVB TRANCONN	PAGE: 17 OF 17

REGULATORS



PIN NAMES
V08P\I
V33P\I
VGTLTERM\I



FOUR OF THESE TESTPOINTS ARE 109 VME ASSEMBLY HOLES

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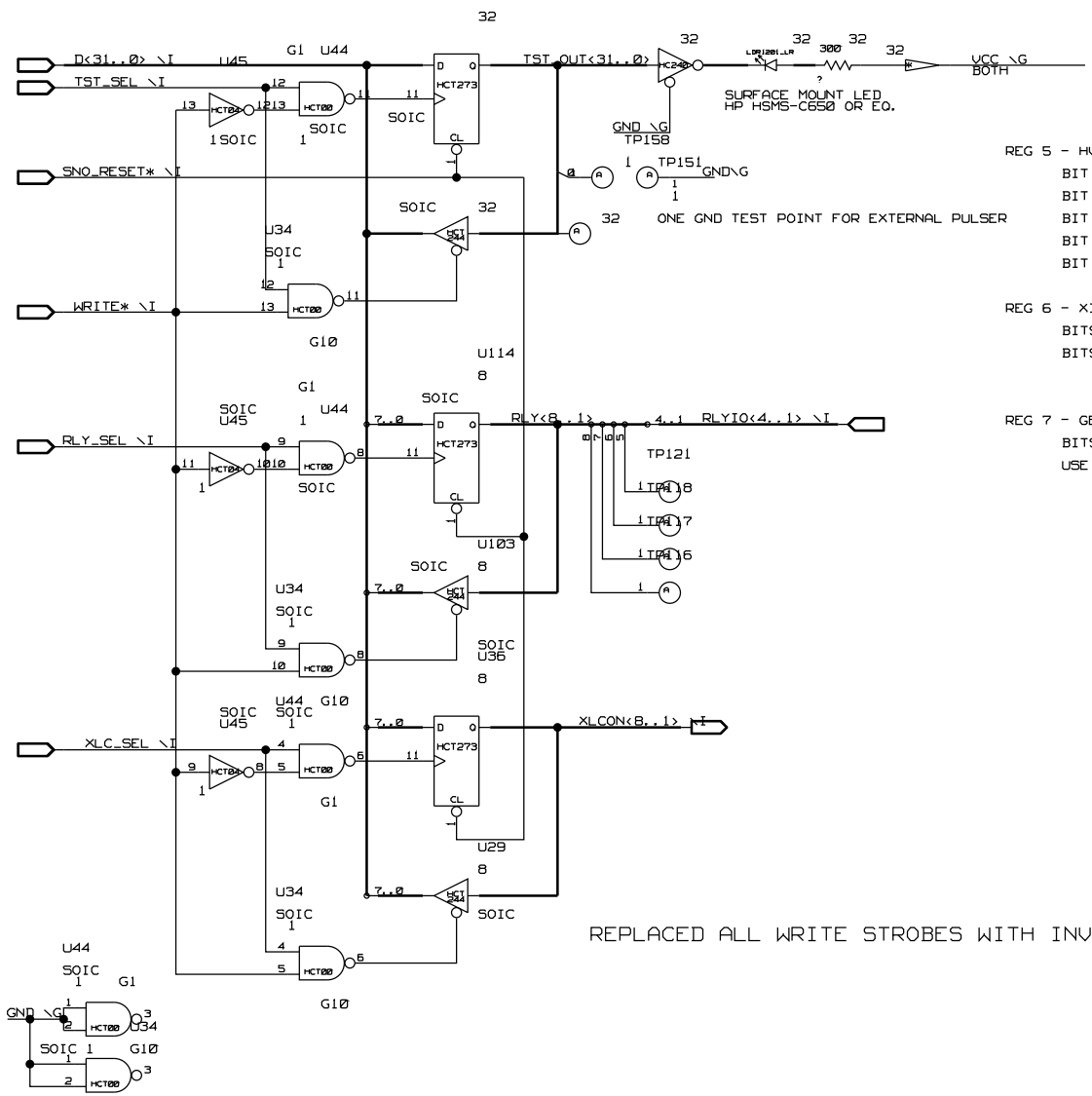
HIGH ENERGY PHYSICS

TITLE: REGULATORS REGULATORS	DATE:
ENGINEER: RVB, PW	PAGE: 17A OF 17

RELAY XILINX‹LOAD› TEST REGISTERS



REG 5 - HV RELAY CONTROL
- BIT 0 - RELAY CLOCK
- BIT 1 - RELAY DATA
- BIT 2 - RELAY RESET
- BIT 3 - RELAY DATA OUT
- BIT 4 - RELAY LOAD

REG 6 - XILINX UBER CONTROL AND CHECK
- BITS‹8..5› - CONTROL - ENABLE XILINX LOAD IF = 0101
- BITS‹4..1› - ADDRESS LINE MODIFIERS ‹A‹21..18››
  - A‹21› = 1 AND A‹20› = 0 FORCES XILINX LOAD MODE ON MB

REG 7 - GENERAL READ/WRITE/DISPLAY TEST REGISTER
- BITS‹31..0› - DATA
- USE ONE BIT FOR EXTERNAL PULSER.

PIN NAMES
- XLCON‹8..1›\I
- XLC_SEL\I
- TST_SEL\I
- RLY_SEL\I
- RLYIO‹4..1›\I
- SNO_RESET*\I
- WRITE*\I
- D‹31..0›\I

REPLACED ALL WRITE STROBES WITH INVERTED TO MATCH CLOCK REG STROBE ASSERTION

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TITLE: RL_XL_TST_REGS	DATE:
RLXLTSTREG LAST_MODIFIED=Thu Feb 27 15:04:08 1997	
ENGINEER: RVB	PAGE: 1