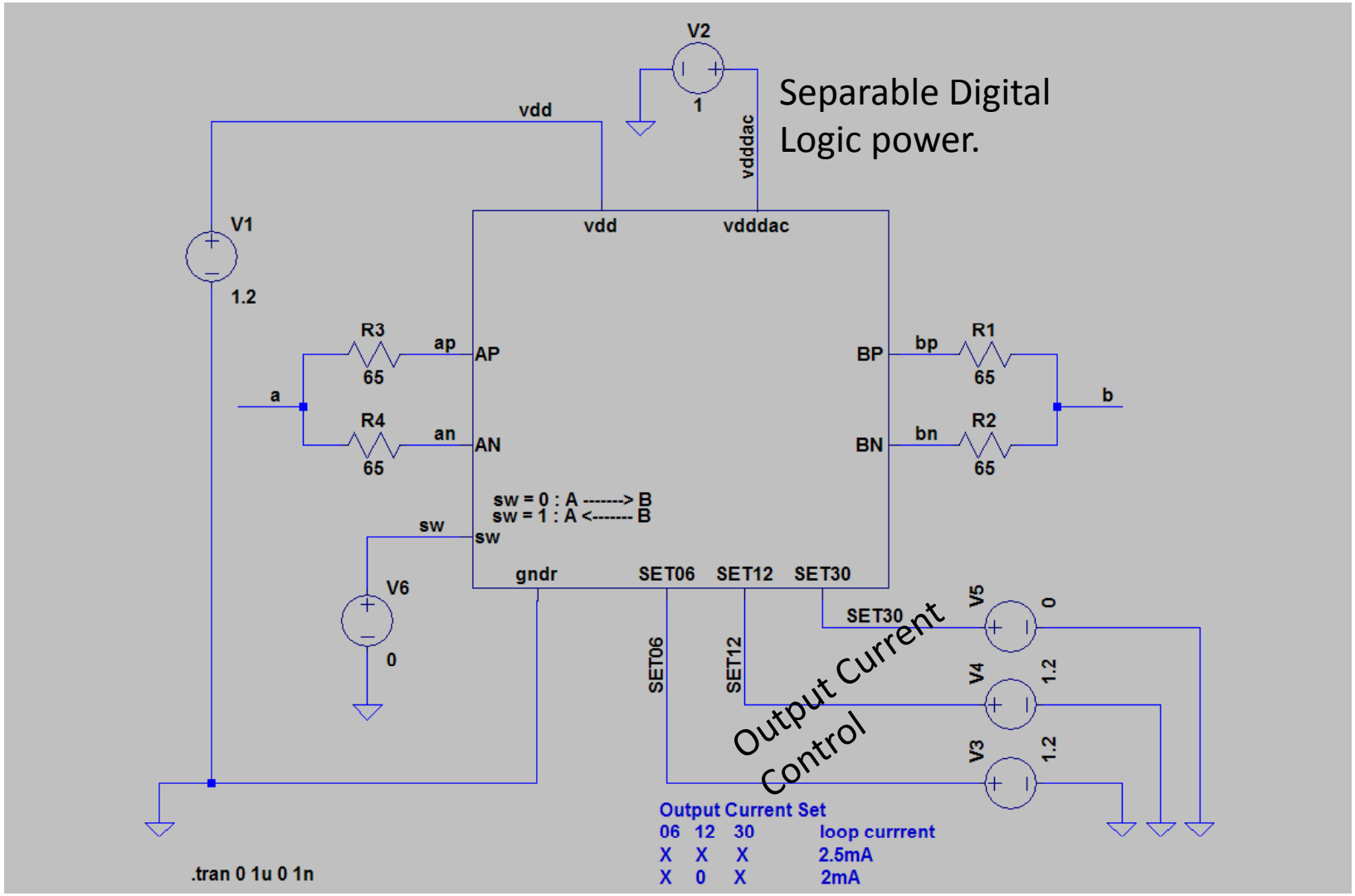
ABCn Driver Receiver and Shunt Blocks a Preliminary Look

Nandor Dressnandt
Mitch Newcomer
Devyn Schafer

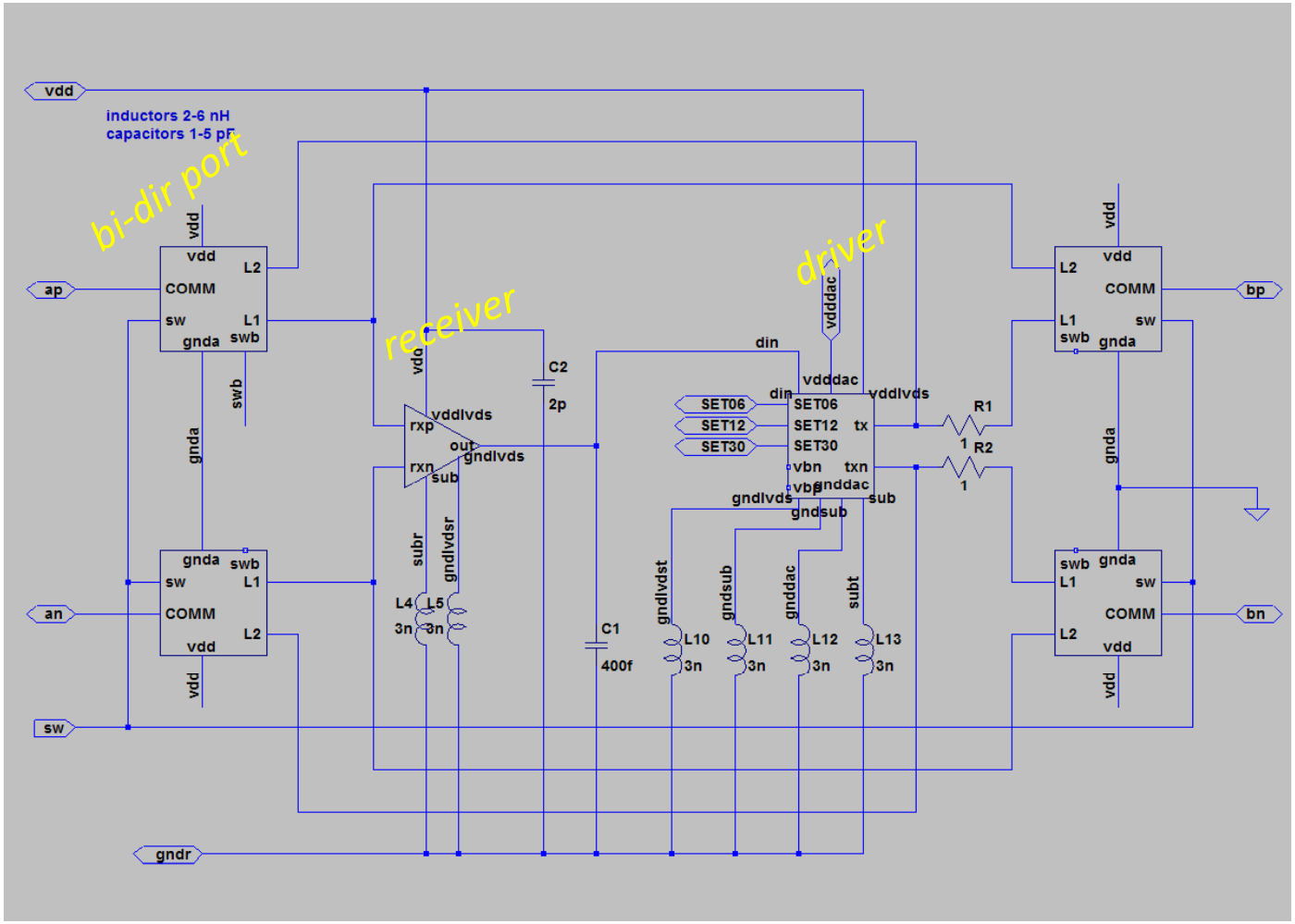
130nm Transceiver



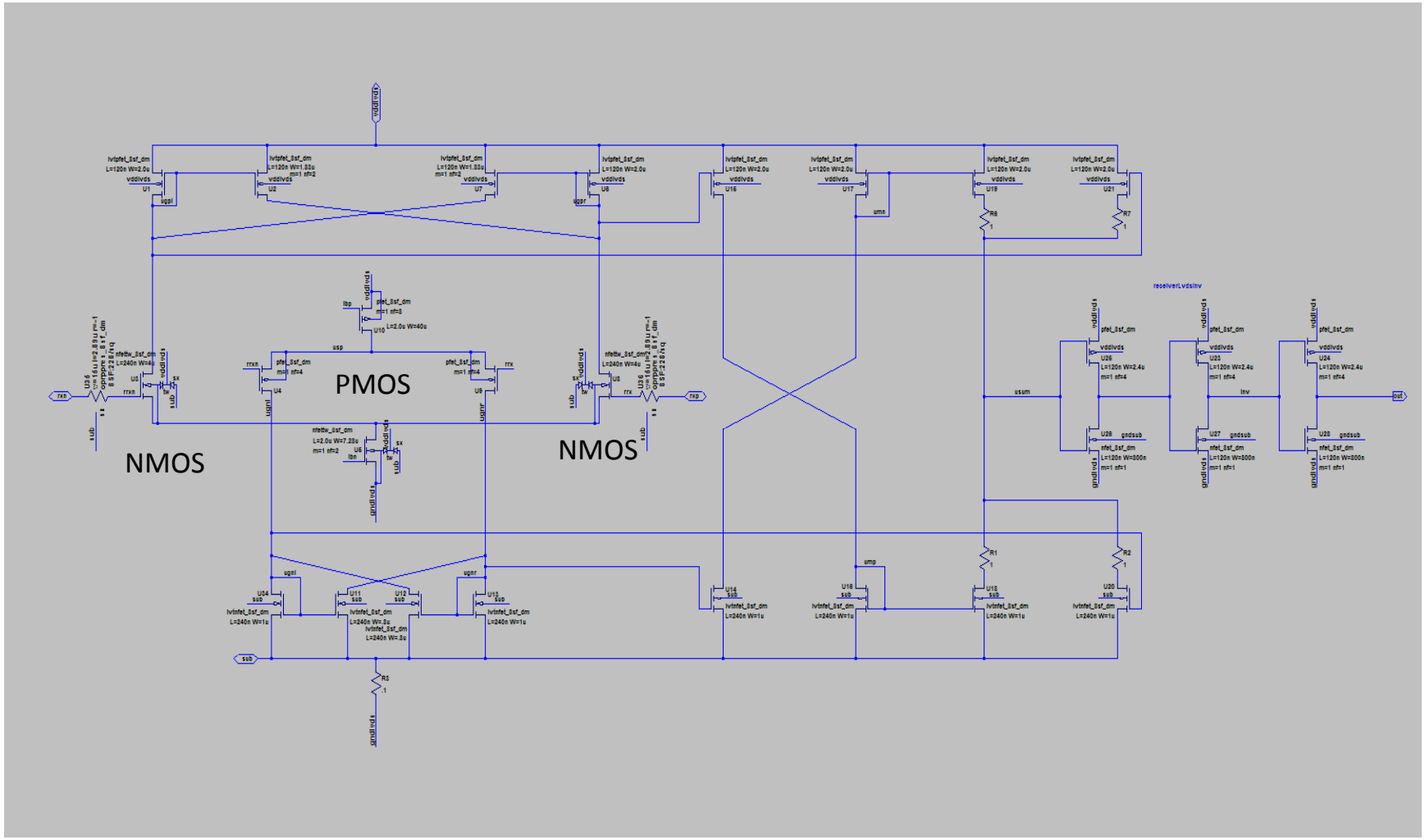
Major Transceiver Sub-Blocks

* < 20 Ω port res.
0-3mA driver
Rcvr 0-1.2V CM

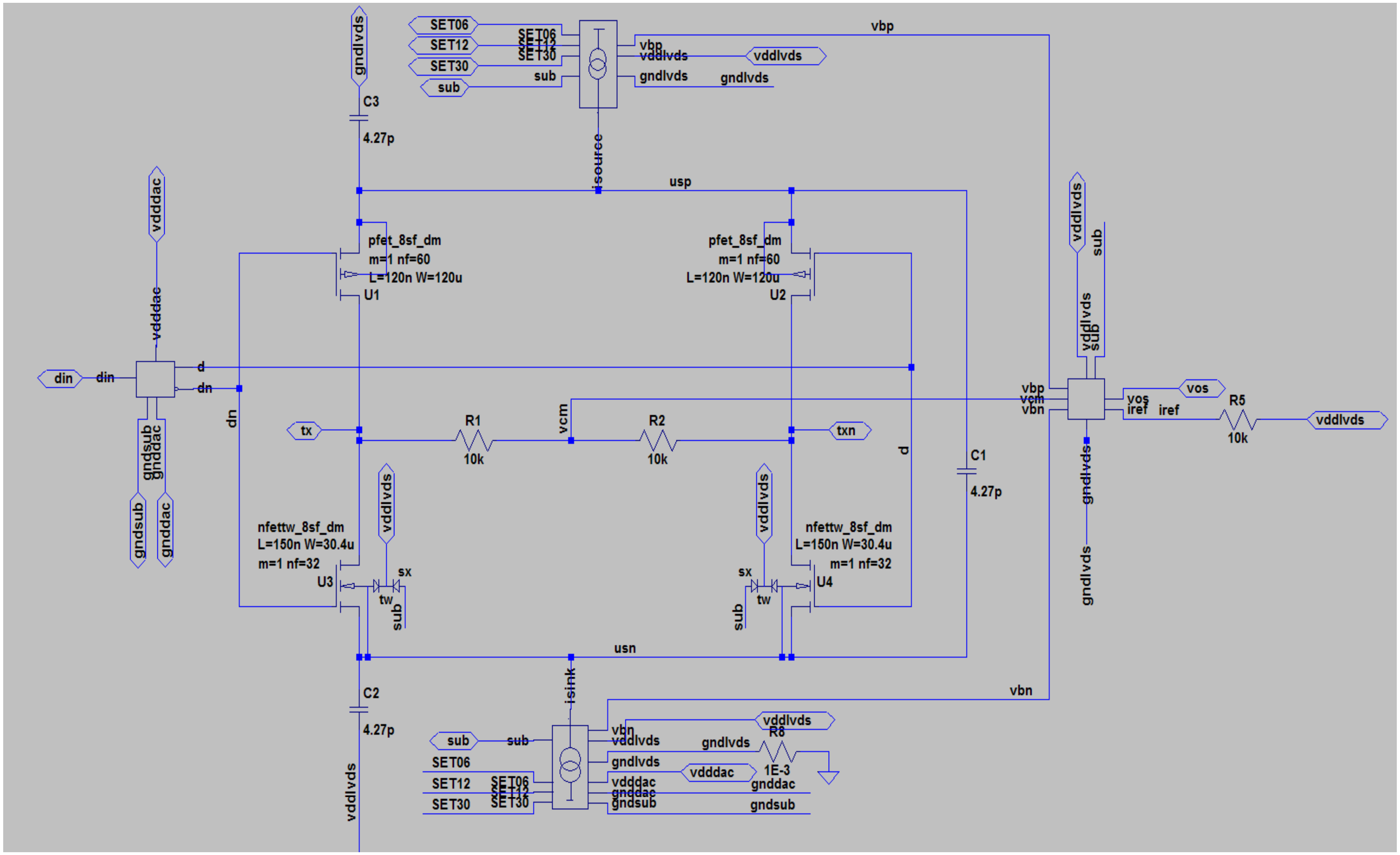
P O W E R
RCVR 330uW
Driver 1.5mW +
drive current pwr



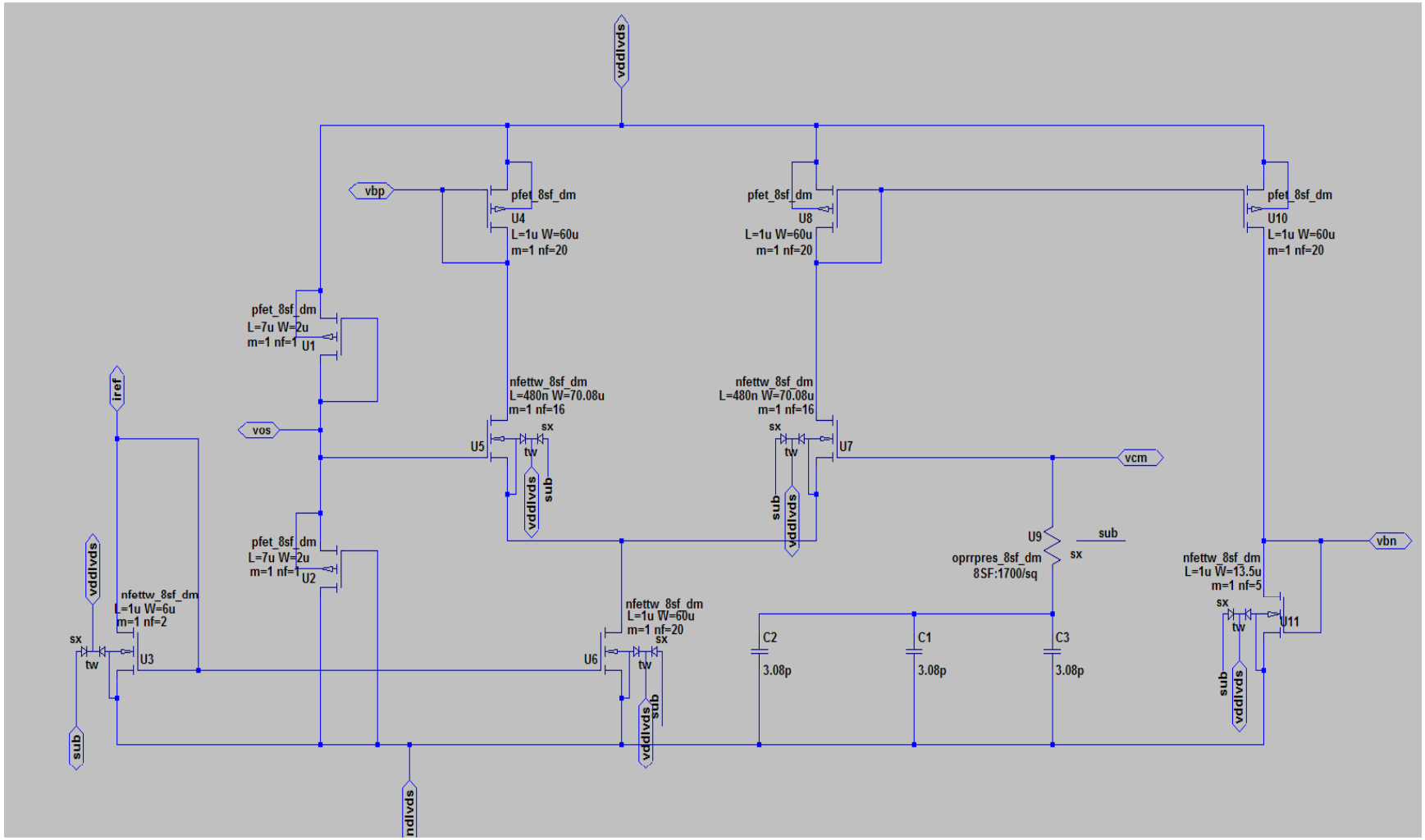
Rail to Rail Receiver



Driver

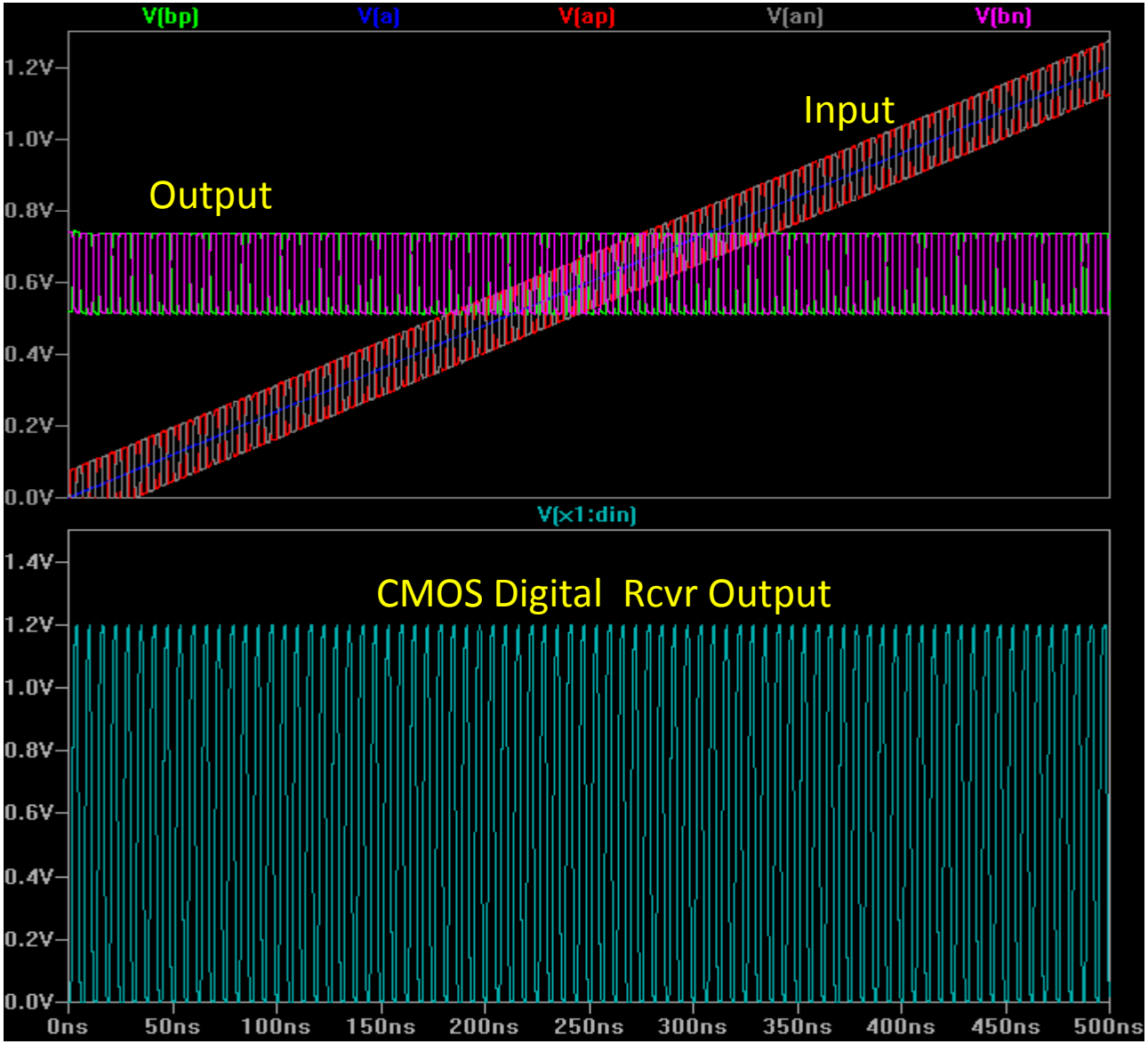

SET06
SET12
SET30
sub
vbp
vddlvds
gndlvds
isource
usp
gndlvds
C3
4.27p
vdddac
din
d
dn
gndsub
gnddac
pfet_8sf_dm
m=1 nf=60
L=120n W=120u
U1
U2
tx
txn
R1
10k
R2
10k
vcm
nfettw_8sf_dm
L=150n W=30.4u
m=1 nf=32
U3
U4
sx
tw
usn
isink
C2
4.27p
C1
4.27p
vbn
vos
iref
R5
10k
R8
1E-3
vdddac
gnddac
gndsub

Driver Common Mode Adjust



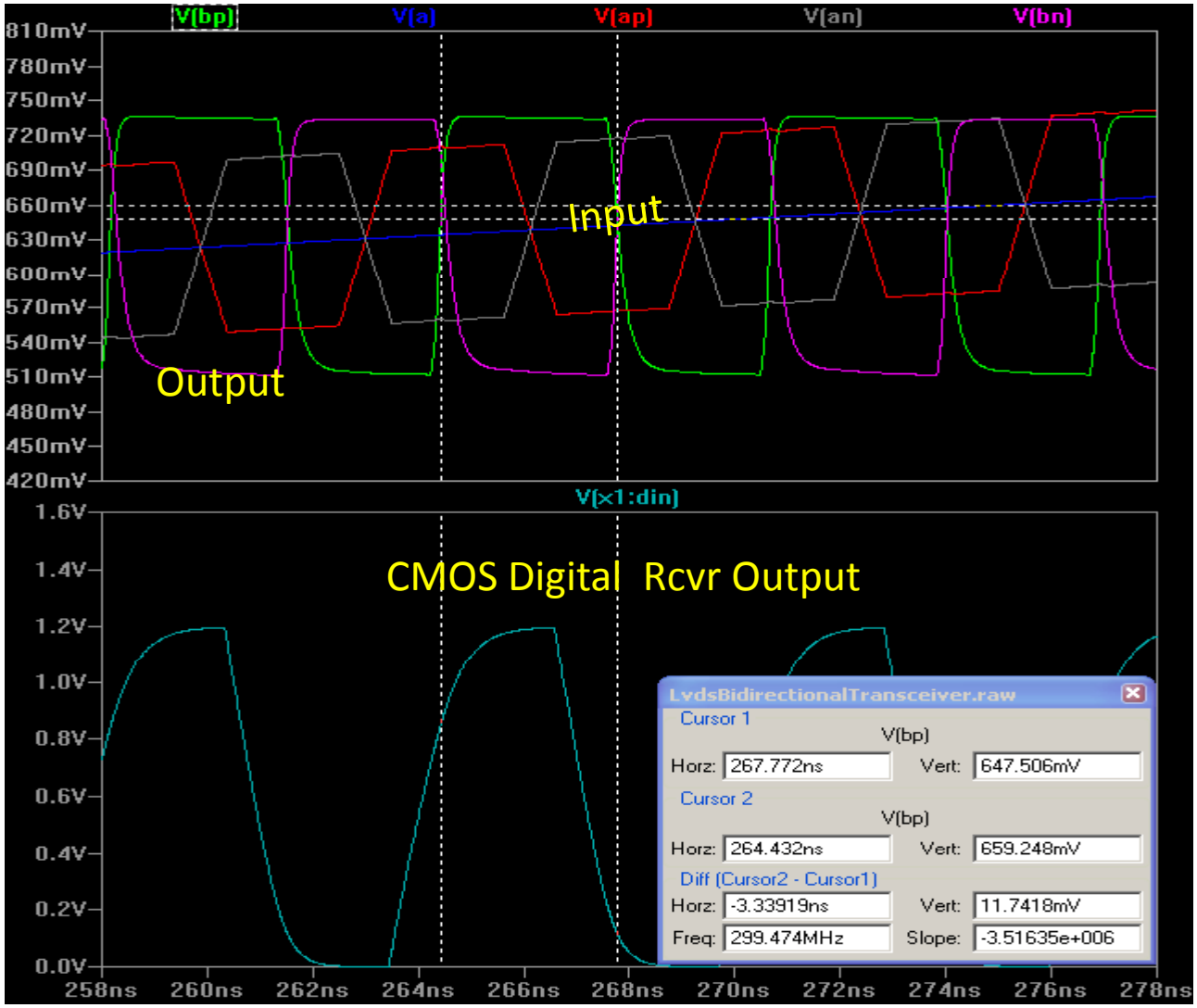
Common Mode Range @160MHz Vdd=1.2V

Input Hi Z
± 75mV
Common Mode
Input 0 – 1.2V
Output OK over
full CM Range



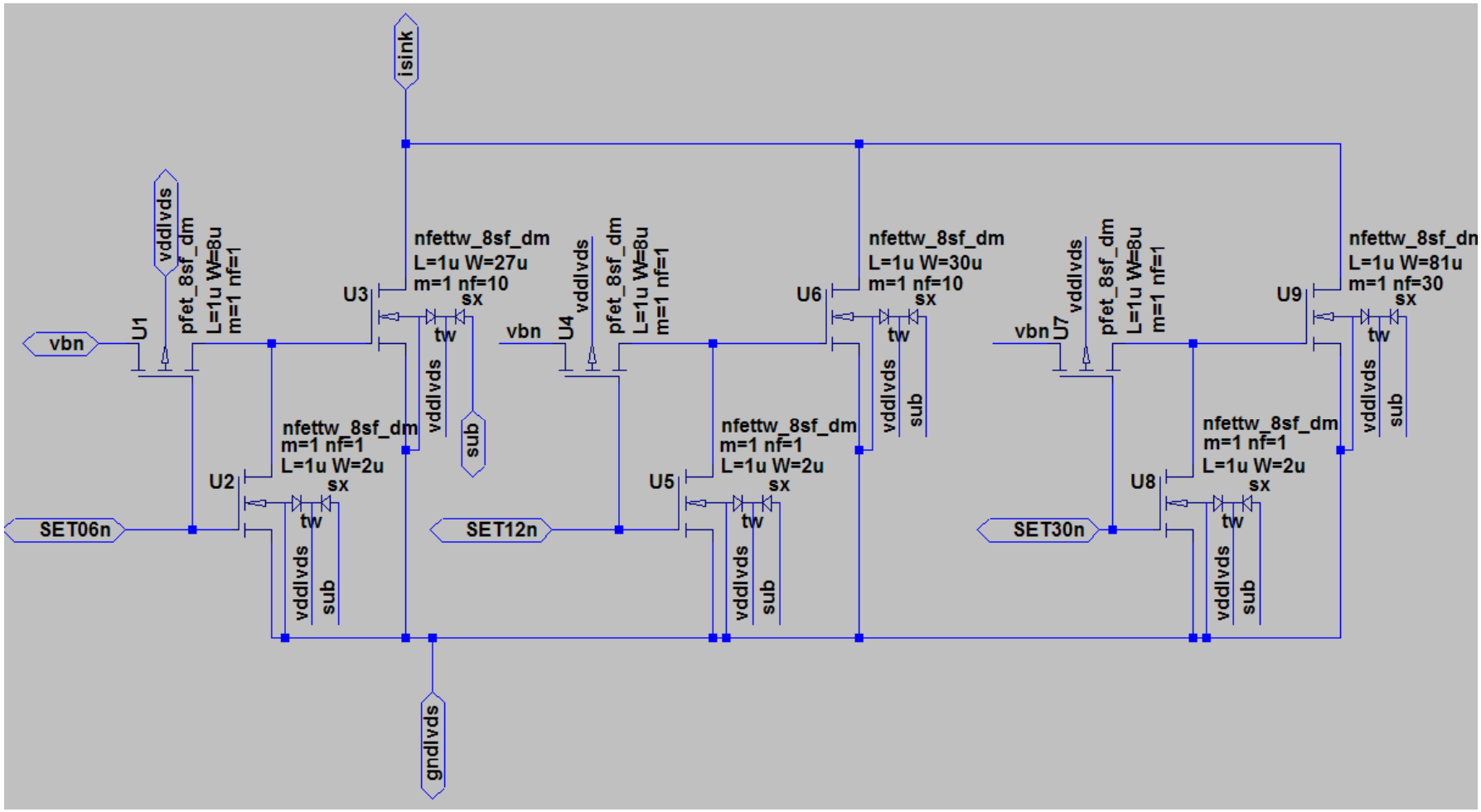
Internal Receiver
OK over Full
CM Range

Expanded View@160MHz Vdd=1.2V



Mixed TW and Standard Transistor

What is the appropriate Convention for T3 / TW ?



Status

- Cadence Schematic entered
  - Finish error checking
  - Recheck process variation/temp
  - Need to run local variation Monte Carlo

- Layout ??
  - Shape preference?
  - With Pads, without??