Implementation of Multiple Power Loops using the SPP ASIC on Stave09

Mitch Newcomer

Motivations for Multi-Loop Serial Powering

- **Lower Total Voltage**
  - One loop of 24 * 2.4V ~ 60V
  - Two Loops of 12 ~30V
- **Lower stored energy in signal coupling capacitors**
  - 4X smaller with 2 loops
- **Lower Power Dissipation for fixed voltage protection circuitry.**
  - SPP consumes ~6mA adding SPP shunt regulator current reserve would need ~ 8mA total
  - Global SPP voltage should exceed maximum loop voltage by ~ 5V.

    G SPP V Dropping resistor *~¼ Watt (max) for one loop*

    ~½ Watt (max) for two loops

- **Smaller aggregate effects with supply interactions**
- **Easy to test larger single loop by simply re arranging jumper fields.**

Overhead to add 2 Loop capability

Physical requirement to go from 1 loop to 2 loops

- **One jumper field is required on the stave bus.** Breaks current path. Allows a second supply to be jumpered in.
- **One Jumper field on BNL or Stave bus card.** Breaks SPP global data / voltage line. Allows second supply to be jumpered in.

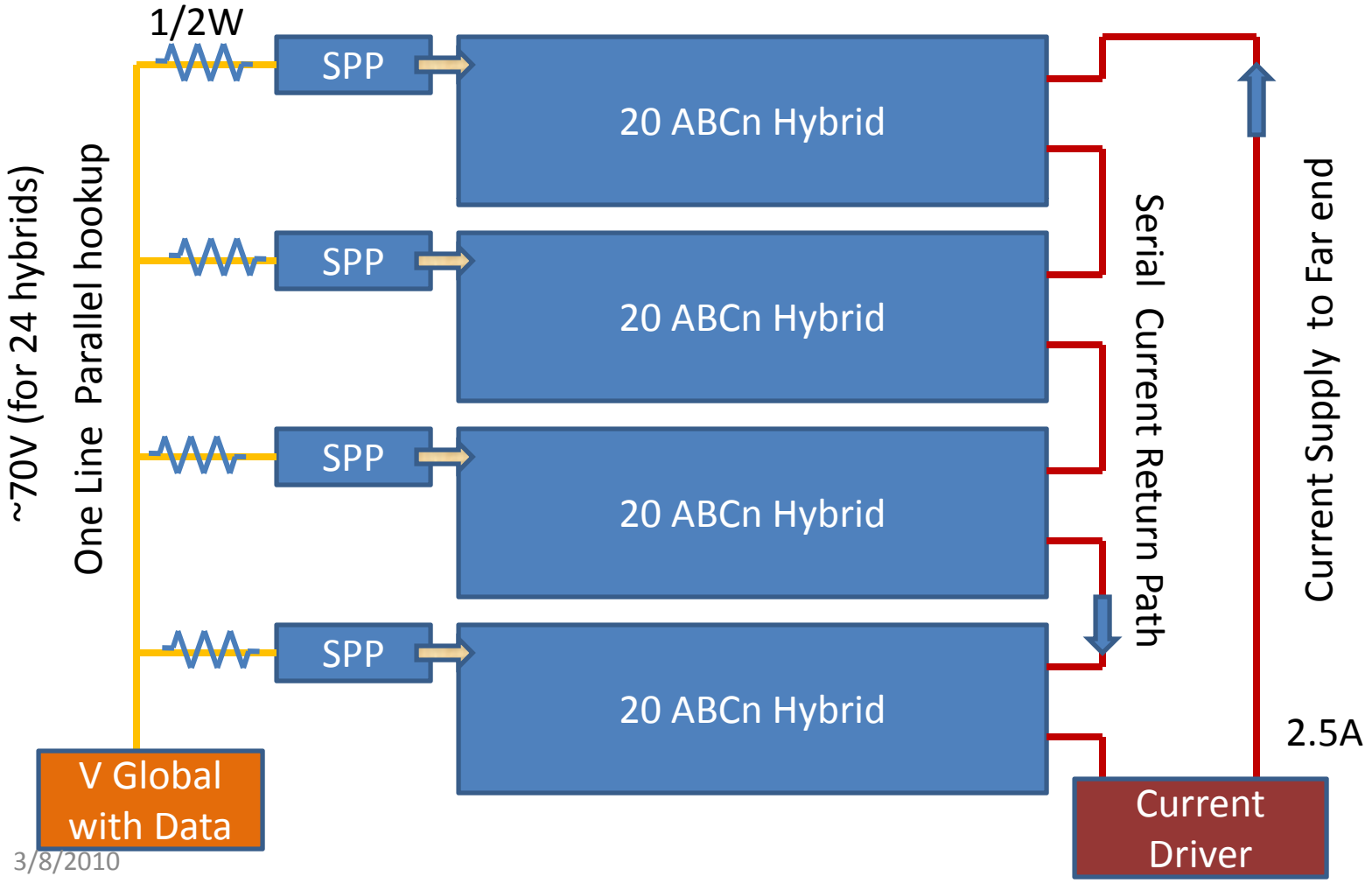
One extra feed line for the second Hybrid Current supply.

One extra feed line for the second SPP power supply.

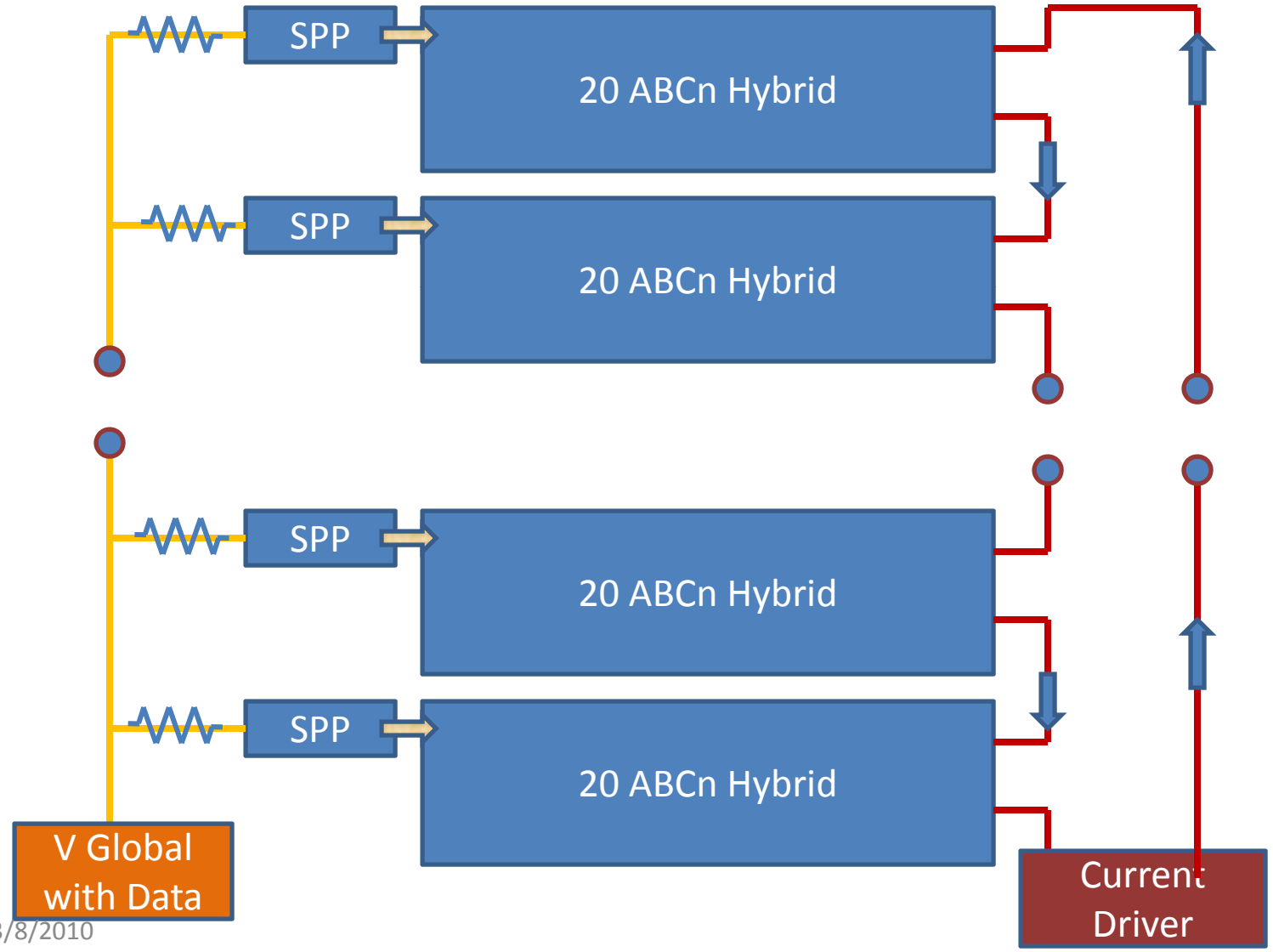
Extra supply lines might be patch wired into jumper field or added to Stave bus.

4 hybrid SPP controlled Single Loop.

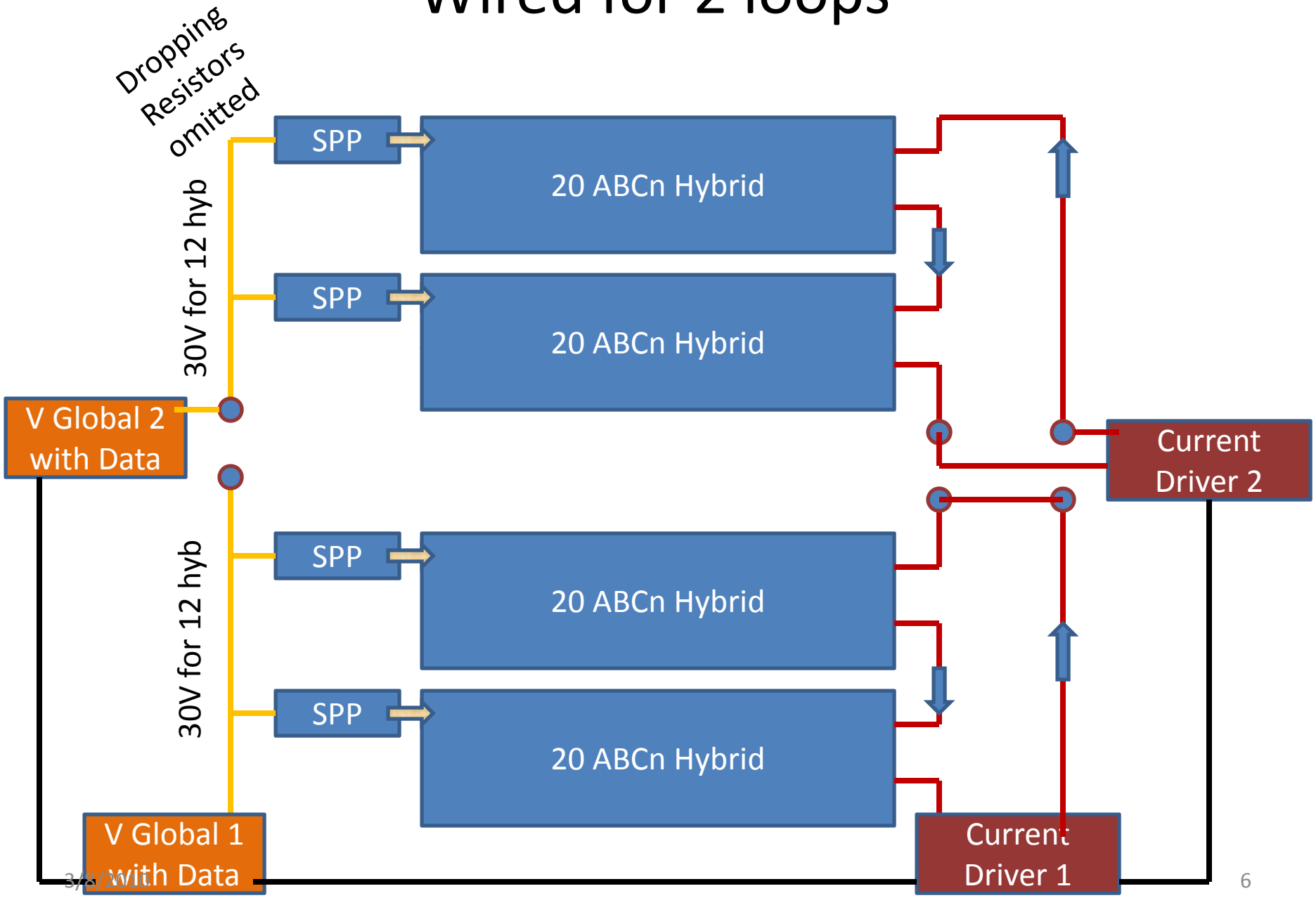
The SPP ASIC is planned to plug into the BNL protection Board it Controls Hybrid voltage and utilizes the BNL FET to short hybrid when reqd. Data may be superimposed on V global or send on a separate line.



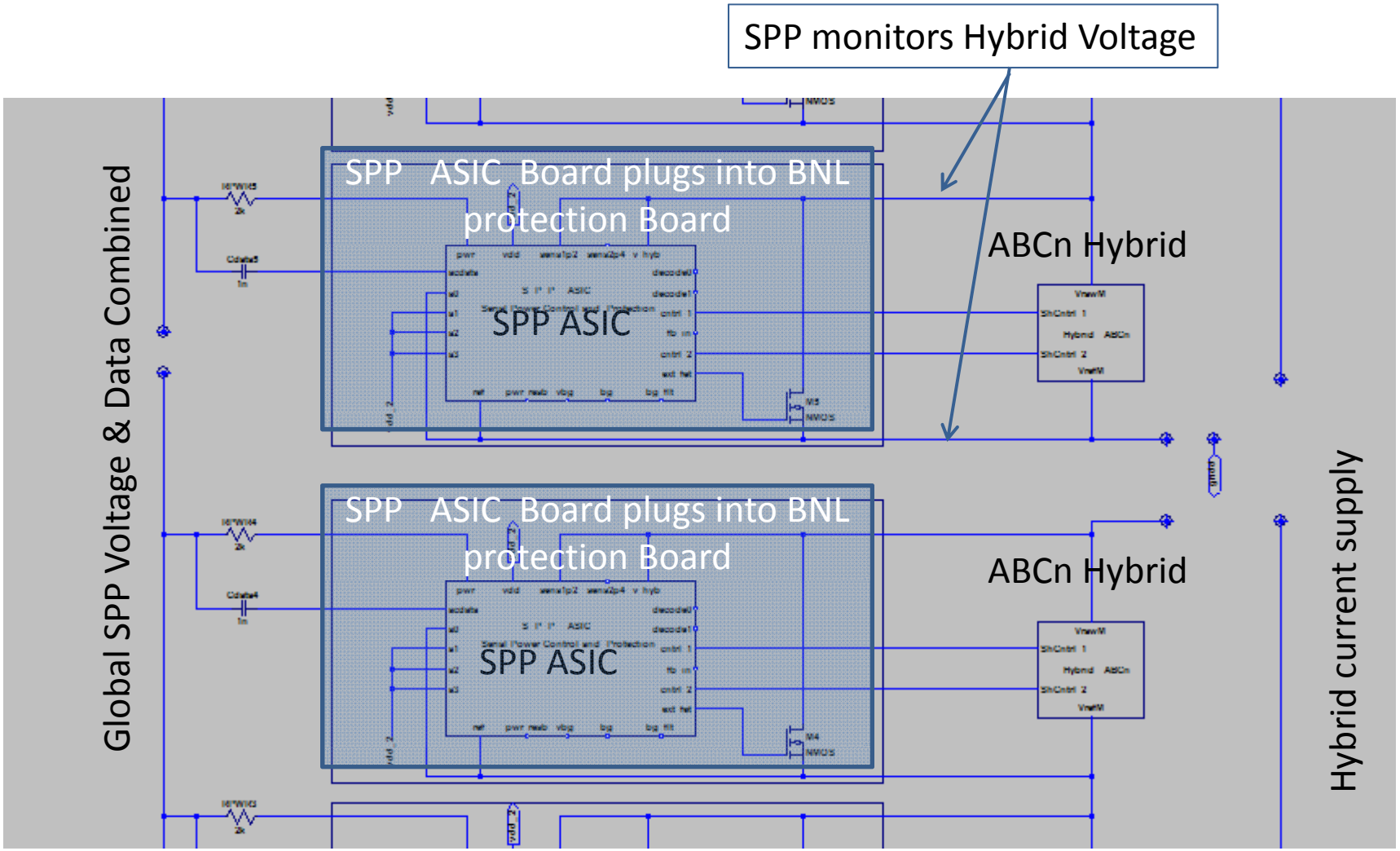
Jumper Fields Required to make 2 loops



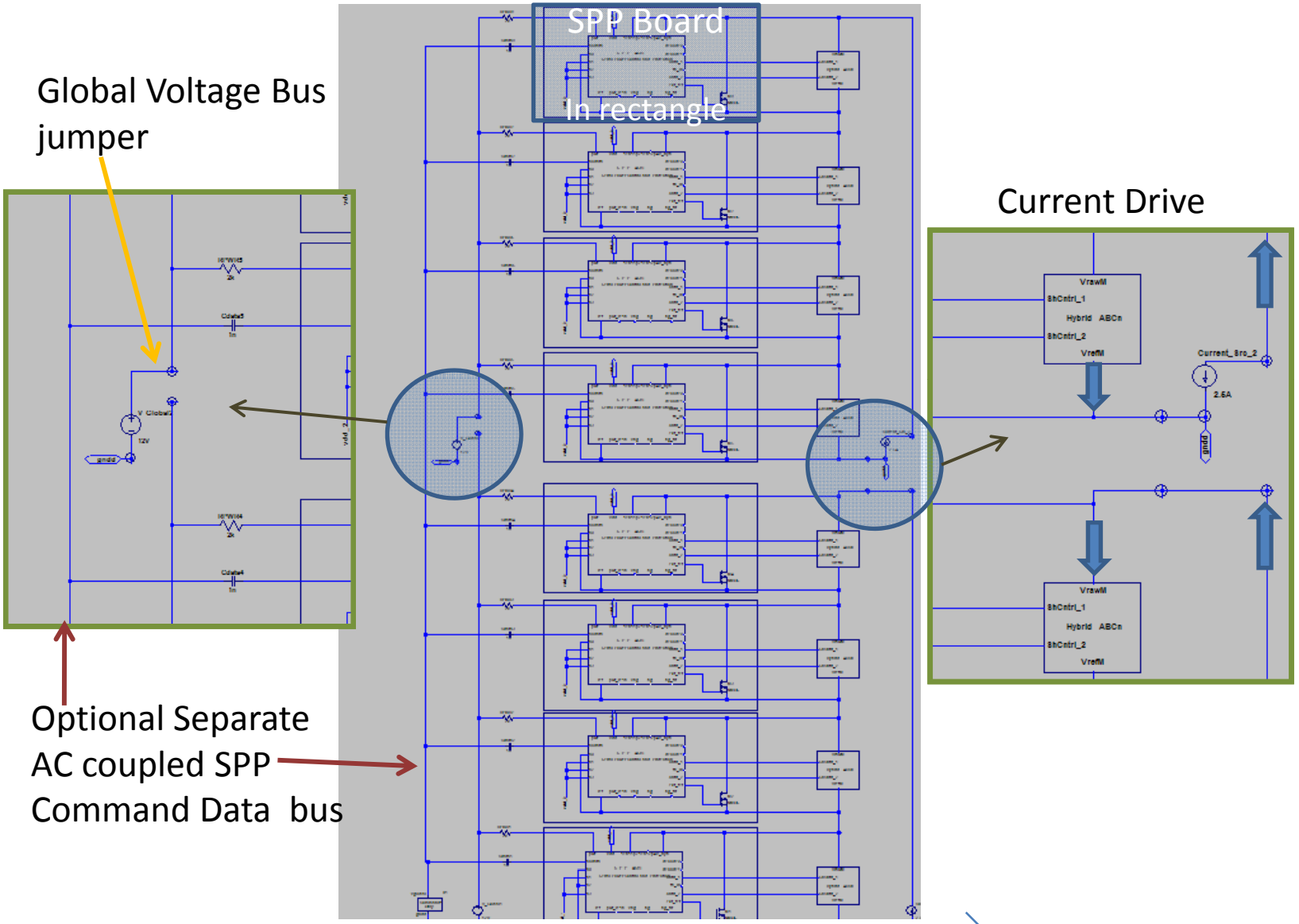
Wired for 2 loops



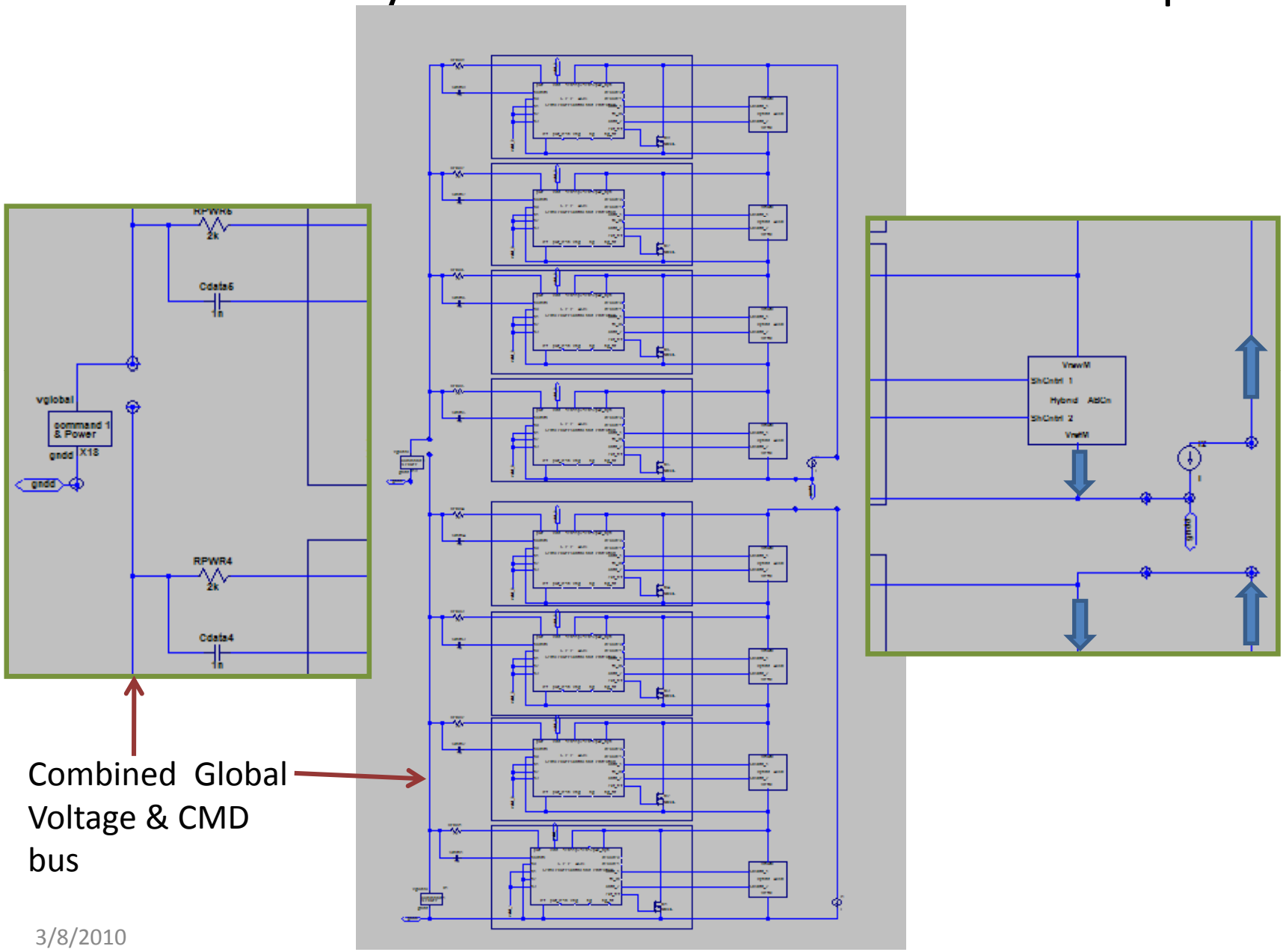
Jumper Fields in Schematic Version



Schematic hookup Using 2 Hybrid Loops

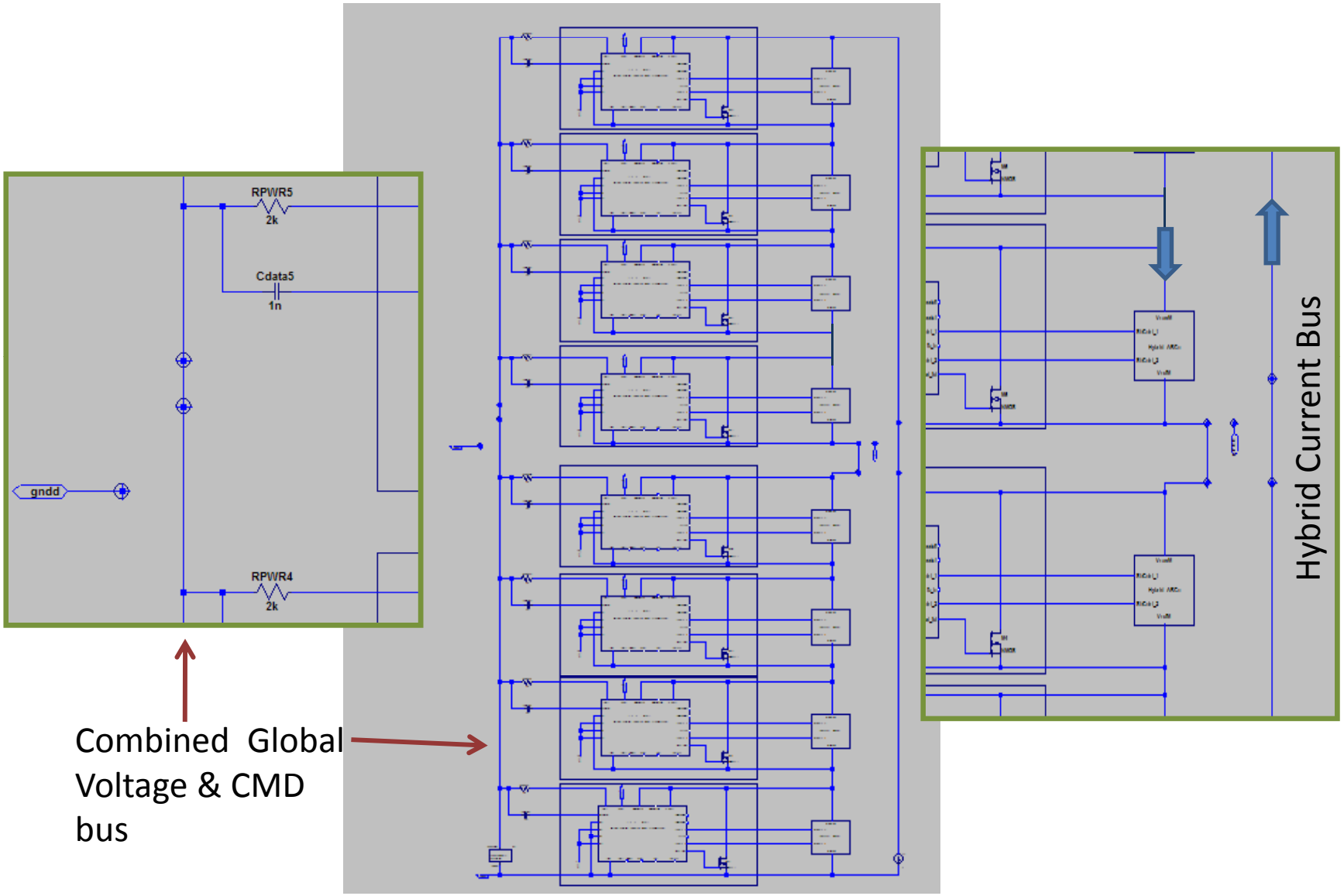


Schematically wired SPP and ABCn for two Loops



Combined Global Voltage & CMD bus

Schematically wired for one loop



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