Serial Power and Protection ASIC

PRELIMINARY

Hookup Details for ABCn implementations

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Implementation of the SPP on Stavelets for Stave 09

The **SPP** is planned to be a 24 pad ASIC for use with the distributed shunt hybrid voltage regulation and over voltage protection. Addressable lines allow the shunt function to turn off and on through external one line commands. A typical command consists of 4 bitsof address and one bit of data. This could be expanded to 5 bits, but at present it is seen to be more compatible with one power and data line for each 12 hybrids.

It requires a voltage dropping resistor (dissipation ~ 200mW) to connect to the common global SPP power supply, an AC coupling capacitor for the data line, 3 local filter caps, has the possibility of some reference adjustment. Most of its pads are for monitoring or filtering but it will require several external connections described here. The local connections for filtering etc. will be implemented on a PCB that has a mating plug for the BNL power board.

SPP PCB Hookup to a Stavelet or Stave 09.

Independent Power / Data (1 or 2 connections)

- Vglobal = n modules*2.4V + 5V
- Data may be superimposed on Vglobal or sent separately.

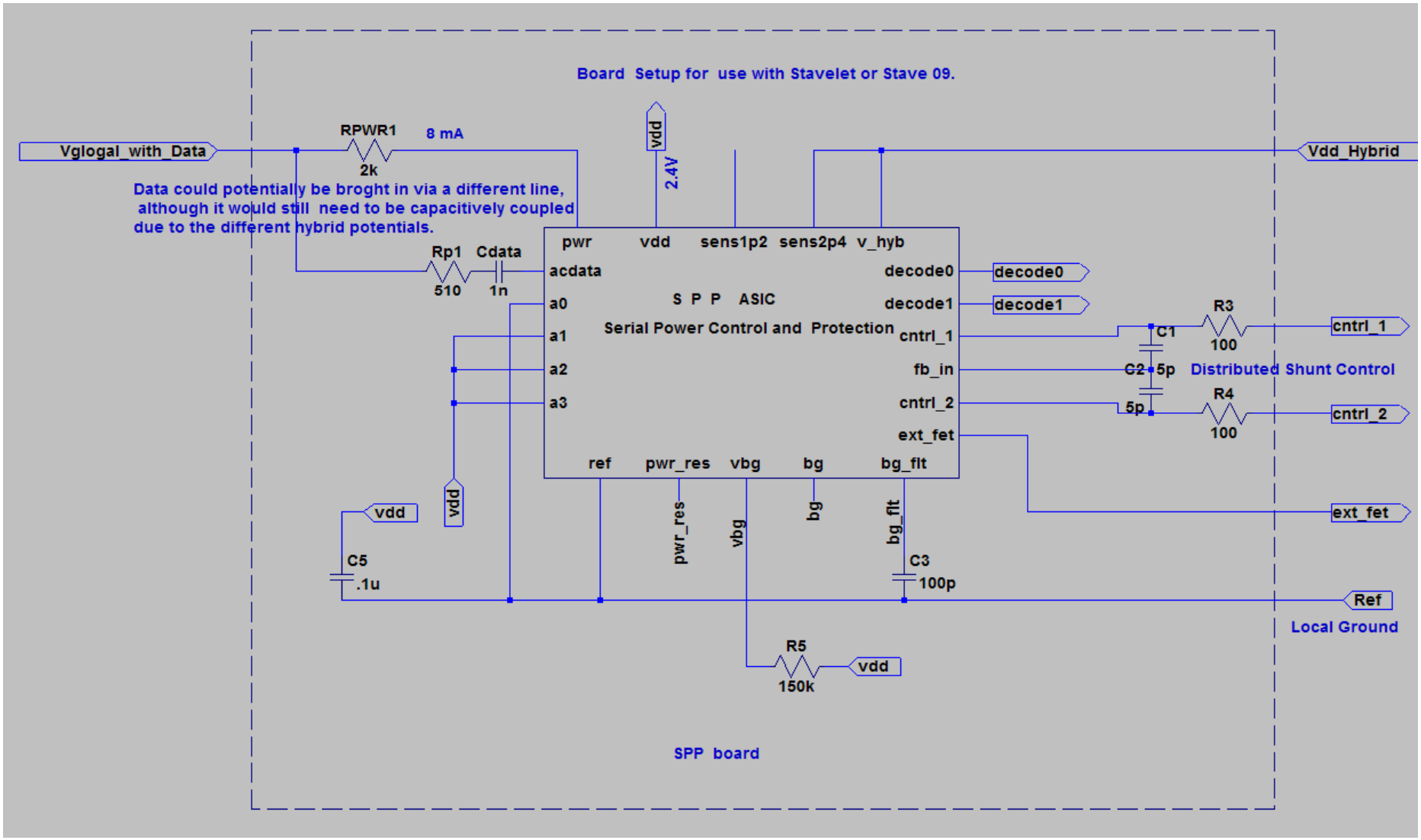
Hybrid Hookup (3 connections)

- Hybrid Vdd
- Distributed Shunt Cntrl_1 and Cntrl_2
- Ref (Hybrid 0V reference)

External (1 connection)

- External FET gate. (up to 2nF capacitance)

SPP hookup to outside world



SPP ASIC Signals (24 pads projected)

# pads	Name	Input / Output	Voltage	Current	Local / Ext	Function
1	pwr	Input	2 - 2.8V	~ 8mA	Ext	Connection to Global Supply Voltage that May have data
1	vdd	output	2.2 - 2.V	Ext Filter	local	intended for 100nF filter cap
1	sens1p2	input	1 to 1.5V	~ 80uA	hybrid conn	Sense Hybrid Voltage for control / OV sense loop ABC130nm
1	sens2p4	input	2.2 to 2.8V	~80uA	hyb	Sense Hybrid Voltage for control / OV sense loop ABCn
2	v_hyb	input	1 to 2.8V	Shunt Assist	hyb	Large internal transistor provides up to .5A to assist shunt module Shunt
						This line connects to either 1p2 or 2p4 sense line and one conductor
						goes to the hybrid
1	decode0	output	0 to 2.4 Logic sig	Low	debug	Diagnostic only
1	decode1	output	0 to 2.4 Logic	Low	debug	Diagnostic only
1	cntrl_1	output	0 to 2.4	up to 1.5mA	hybrid conn	Distributed Shunt Control/Shunt line 1
1	fb_in	input	0 to 2.4	N/A	local	Capacitice feedback to Shunt regulator
1	cntrl_2	output	0 to 2.4	up to 1.5mA	hybrid conn	Distributed Shunt Control/Shunt line 2
1	ext_fet	Output	0 to 2.4	up to 50mA	ext	External FET shunt transistor Gate Control
1	bg_flt	input	.5 to .7V	N/A	internal	Fractional BG voltage used in Filter for Control Loop
1	bg_flt	output	1 to 1.5v	N/A	internal	Band gap voltage buffered
1	vbg	output	1 to 1.5v	N/A	internal	Band gap
1	pwr_res	input	0 to 2.4 Logic	low	internal	External Reset held to 0V with 10K internally
3	ref	input	0V reference	up to 1A transient	hybrid conn	Hybrid reference voltage. Typically ~8mA except when
						Internal shunt is activiated.
1	a3	input	address 3	low	local	short to vdd @= hi to gnd @=low
1	a2	input	address 2	low	local	"
1	a1	input	address 1	low	local	"
1	a0	input	address 0	low	local	"
1	acdata	input	0 - 2V data input	low	external	AC coupled from power OR dedicated line