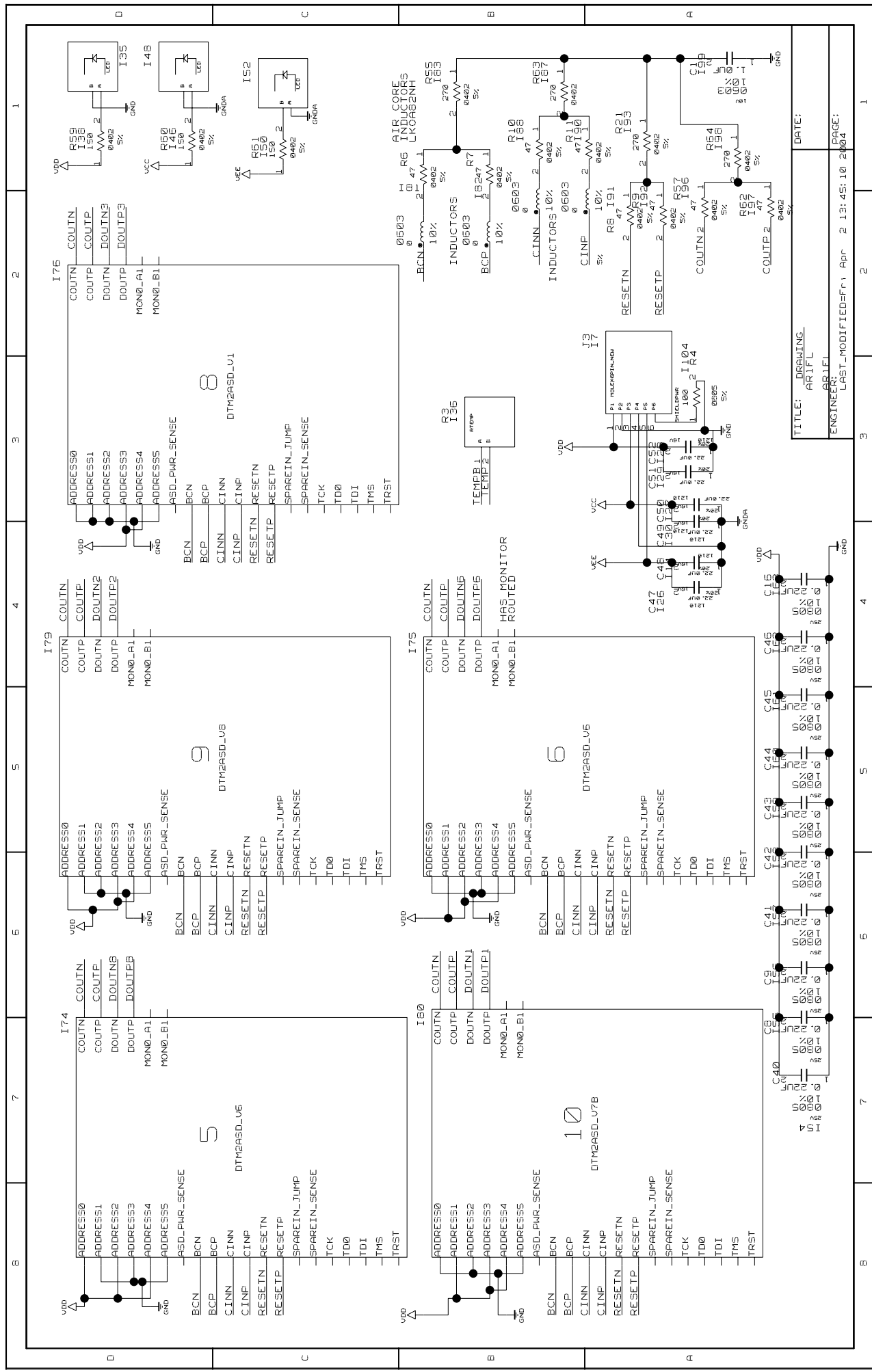


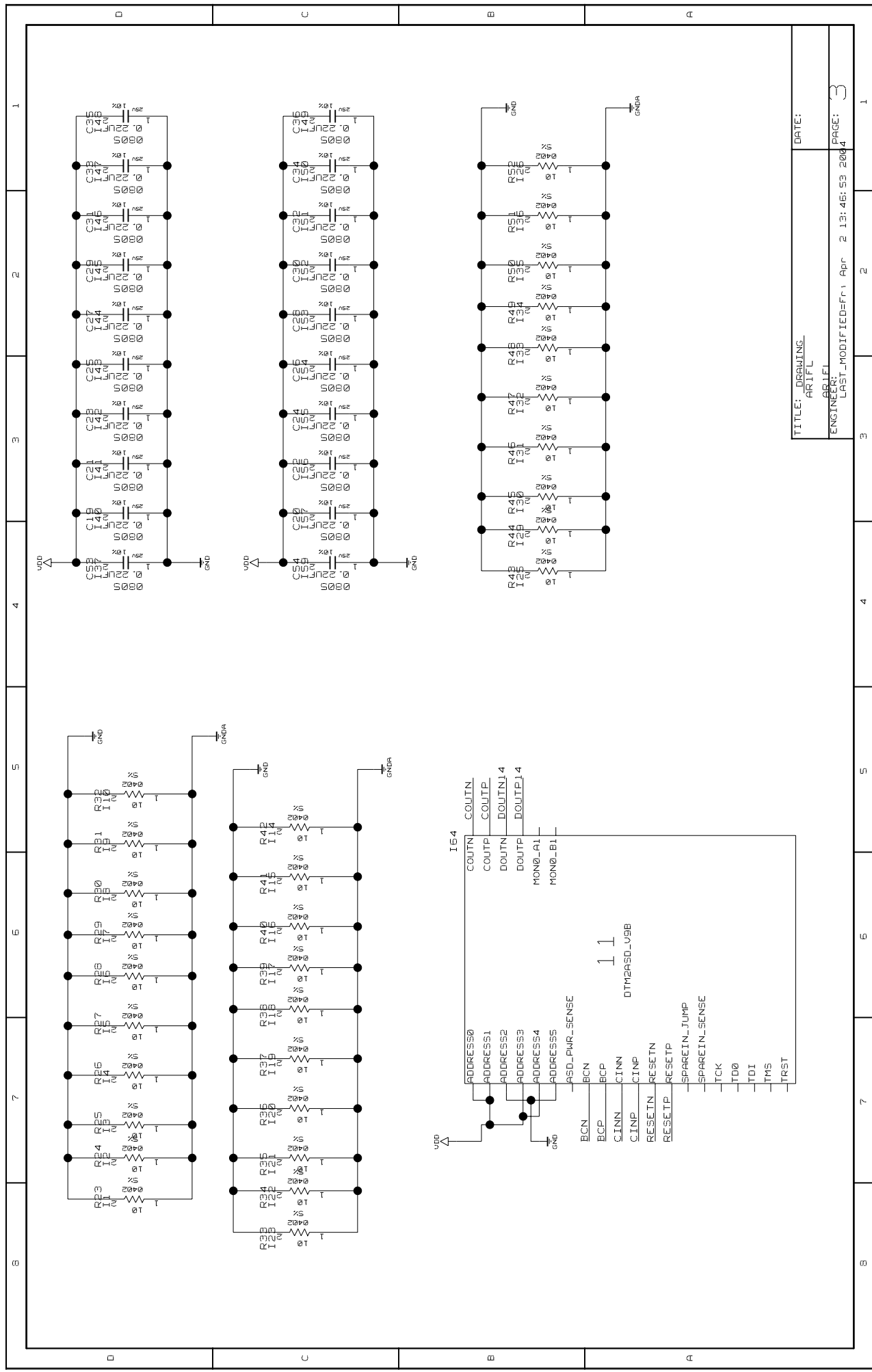
TITLE: DRAWING:  
 AR1FL  
 AR1E1  
 ENGINEER: LAST\_MODIFIED=Fr1 Apr 2 13:32:57 2004  
 DATE:  
 PAGE:  
 2/04



TITLE: DRAWING: ARIFL  
 ENGINEER: ARLEI  
 DATE: \_\_\_\_\_  
 PAGE: 2  
 LAST\_MODIFIED=Fr, Apr 2 13:45:10 2004

1 2 3 4 5 6 7 8

A B C D

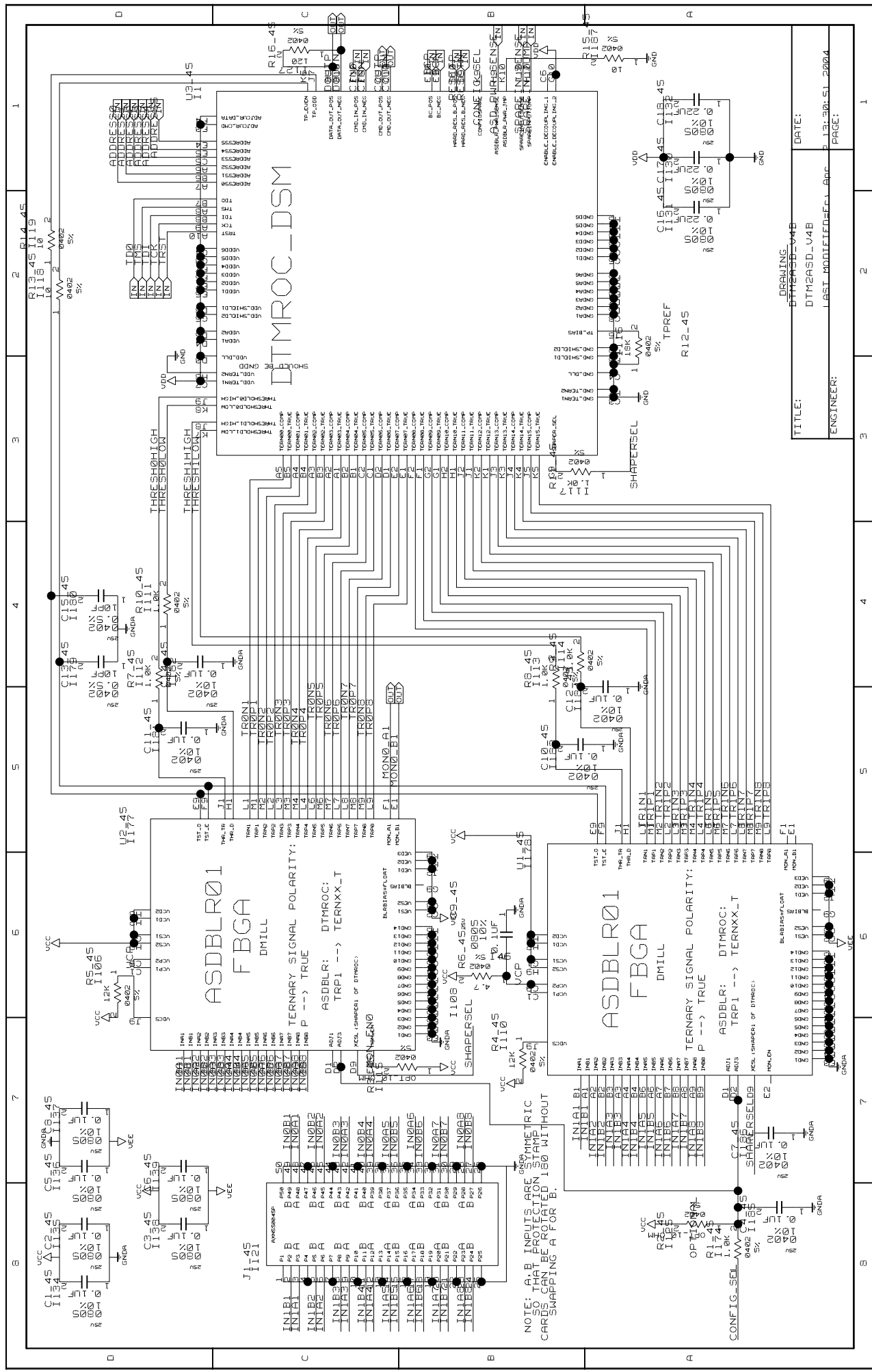


TITLE: DRAWING:  
 AR1PL  
 DATE: \_\_\_\_\_

ENGINEER:  
 AR1PL  
 LAST\_MODIFIED=Fr, 1 Apr 2 13: 45: 53 2004

PAGE: 3

1 2 3 4 5 6 7

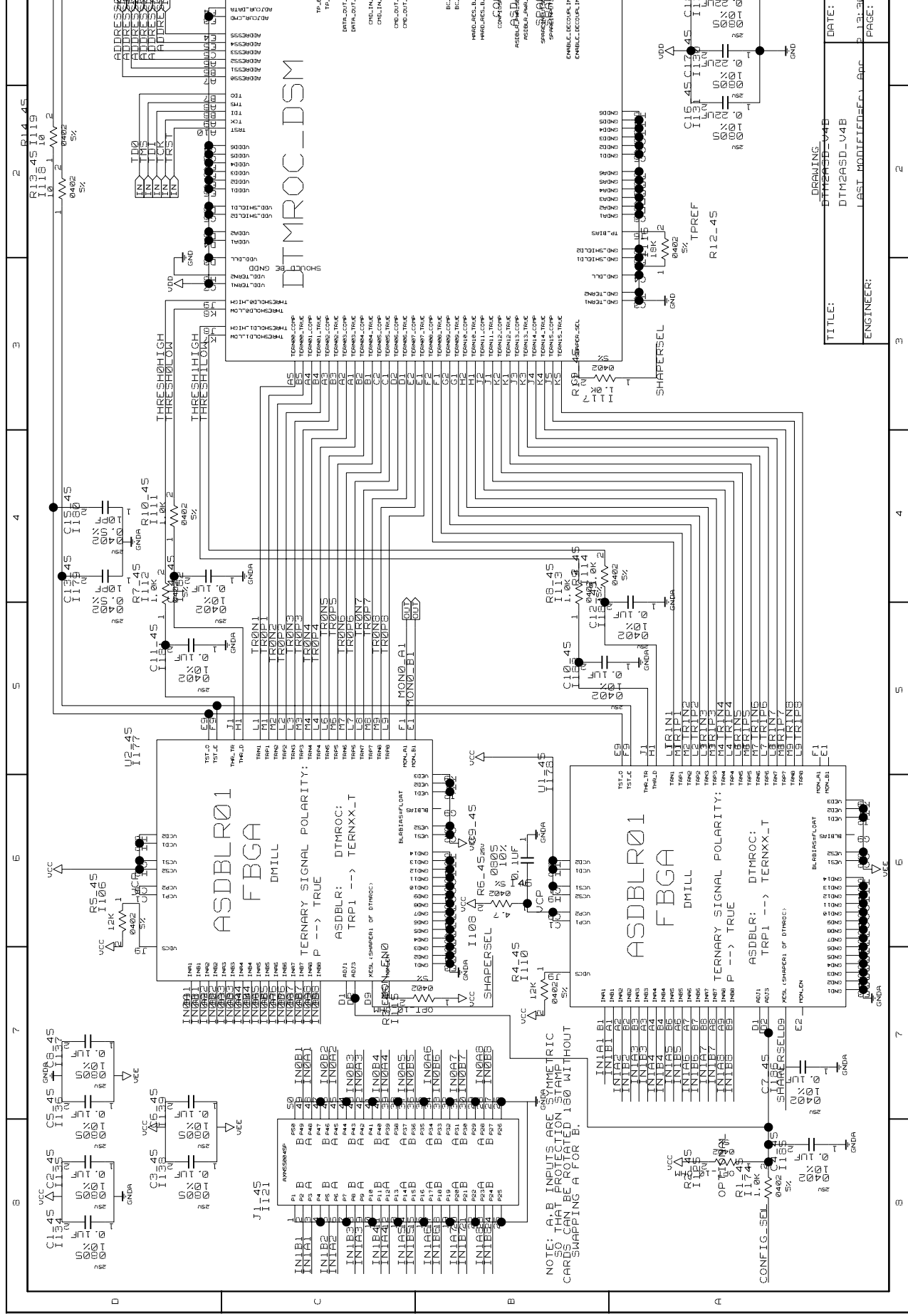


TITLE: DTMR0C-DSM  
 DRAWING: DTMR0C-DSM-V4B  
 DATE: 13-SEP-2004  
 ENGINEER: DTMR0C-DSM  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COFFSET 180 WITHOUT  
 SWAPPING A FOR B

TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMR0C;  
 TRP1 --> TERNXX-T  
 P --> TRUE

TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMR0C;  
 TRP1 --> TERNXX-T  
 P --> TRUE

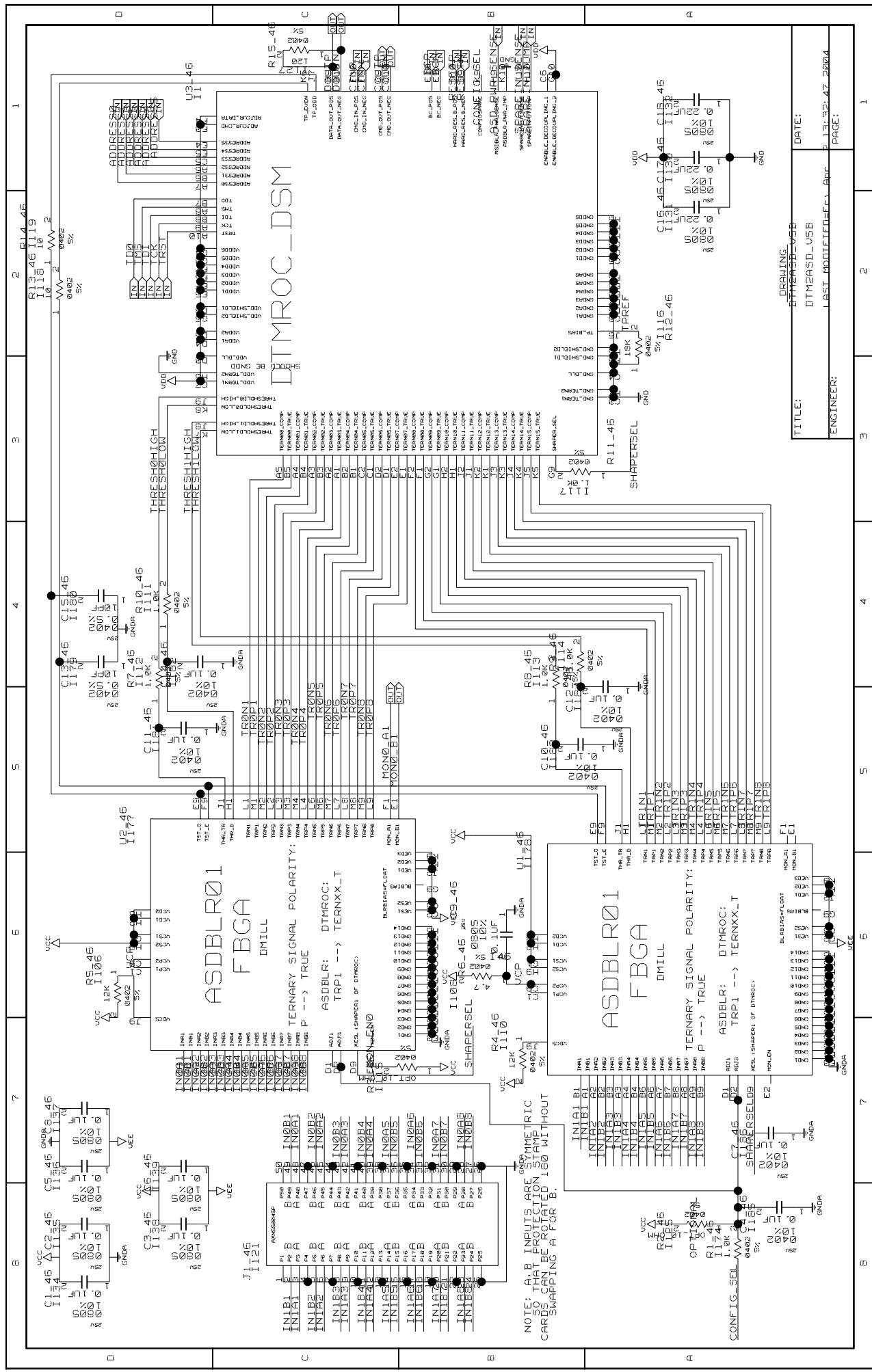


TITLE: DTMR0C-DSM  
 DRAWING: DTMR0C-DSM-V4B  
 DATE: 13-SEP-2004  
 ENGINEER: DTMR0C-DSM  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COFFSET 180 WITHOUT  
 SWAPPING A FOR B

TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMR0C;  
 TRP1 --> TERNXX-T  
 P --> TRUE

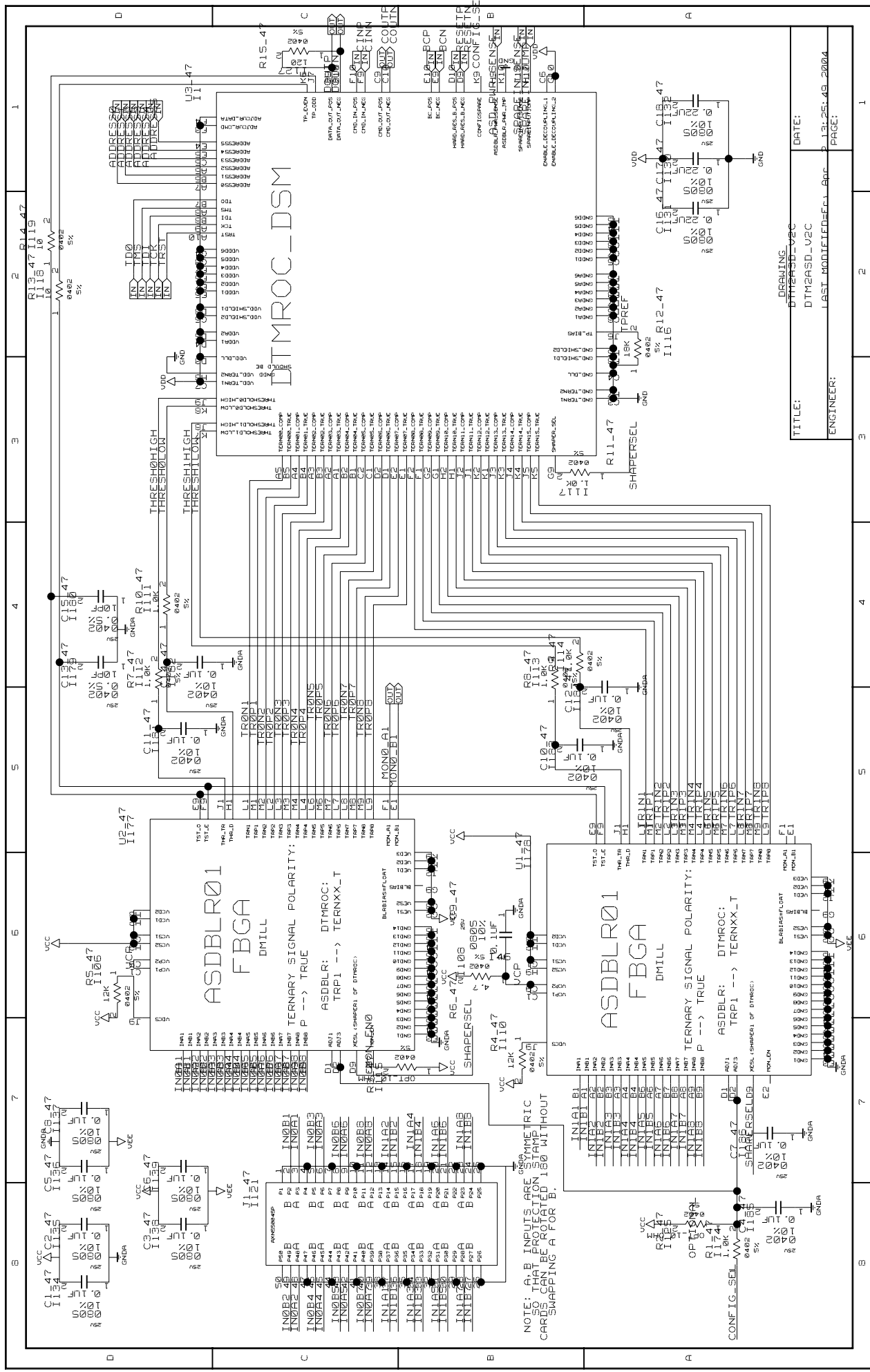
TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMR0C;  
 TRP1 --> TERNXX-T  
 P --> TRUE



TITLE: DTMROC-DSM  
 ENGINEER: DTMROC-DSM  
 DATE: 13:32:47 2004  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COFFSET 180 WITHOUT  
 SWAPPING A FOR B

CONFIG\_SEL[0:15]  
 R11-46  
 R12-46  
 R13-46  
 R14-46  
 R15-46  
 R16-46  
 R17-46  
 R18-46  
 R19-46  
 R20-46  
 R21-46  
 R22-46  
 R23-46  
 R24-46  
 R25-46  
 R26-46  
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 R85-46  
 R86-46  
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 R89-46  
 R90-46  
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 R92-46  
 R93-46  
 R94-46  
 R95-46  
 R96-46  
 R97-46  
 R98-46  
 R99-46  
 R100-46

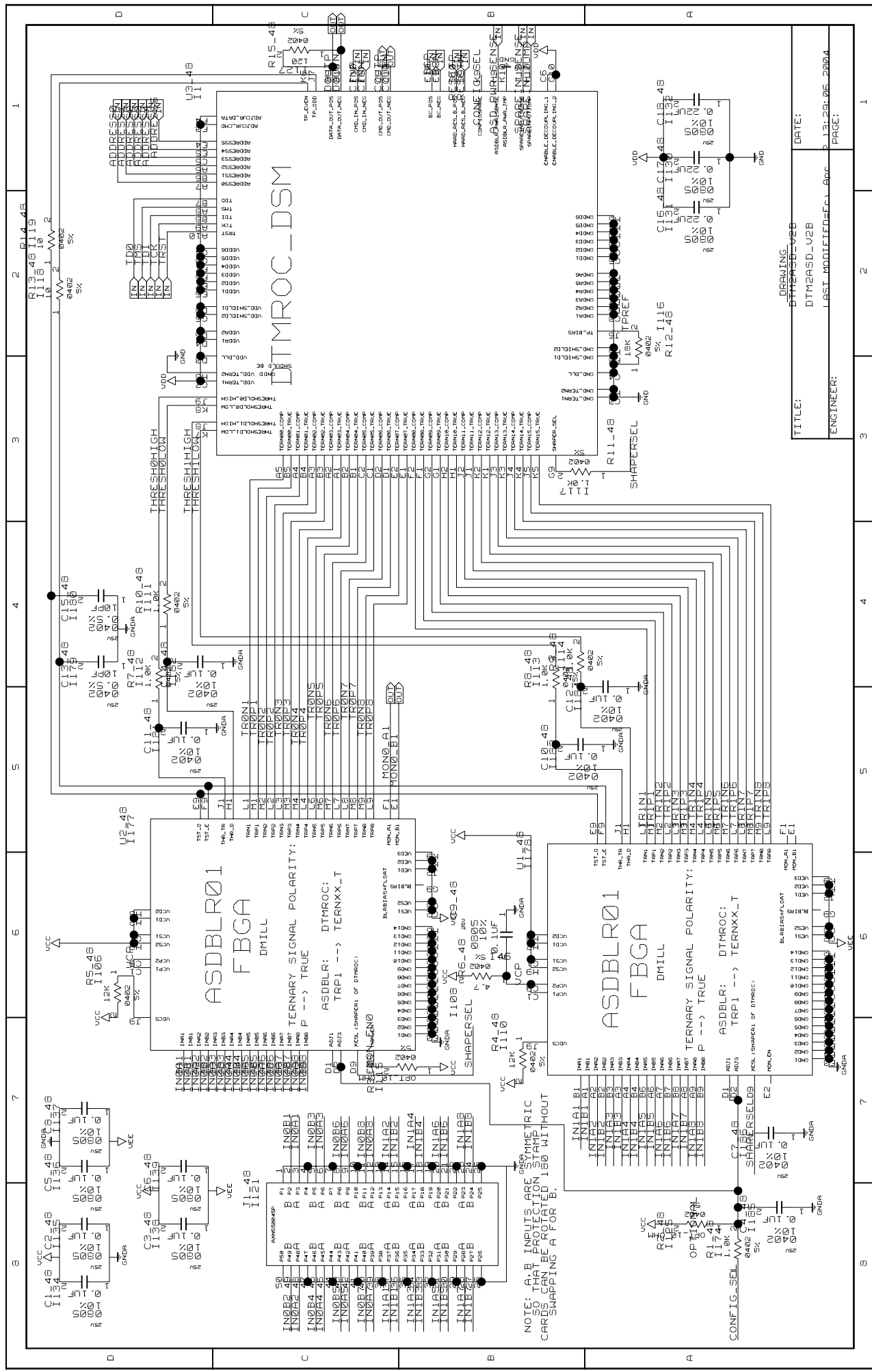


DATE: DTMSRD\_V2C  
 ENGINEER: DTMSRD\_V2C  
 LAST MODIFIED: 2004.09.25

NOTE: A,B INPUTS ARE SYMMETRIC AND MUST BE PROVIDED AT 1.80V WITHOUT SWAPPING A FOR B.

DTMSRD\_V2C

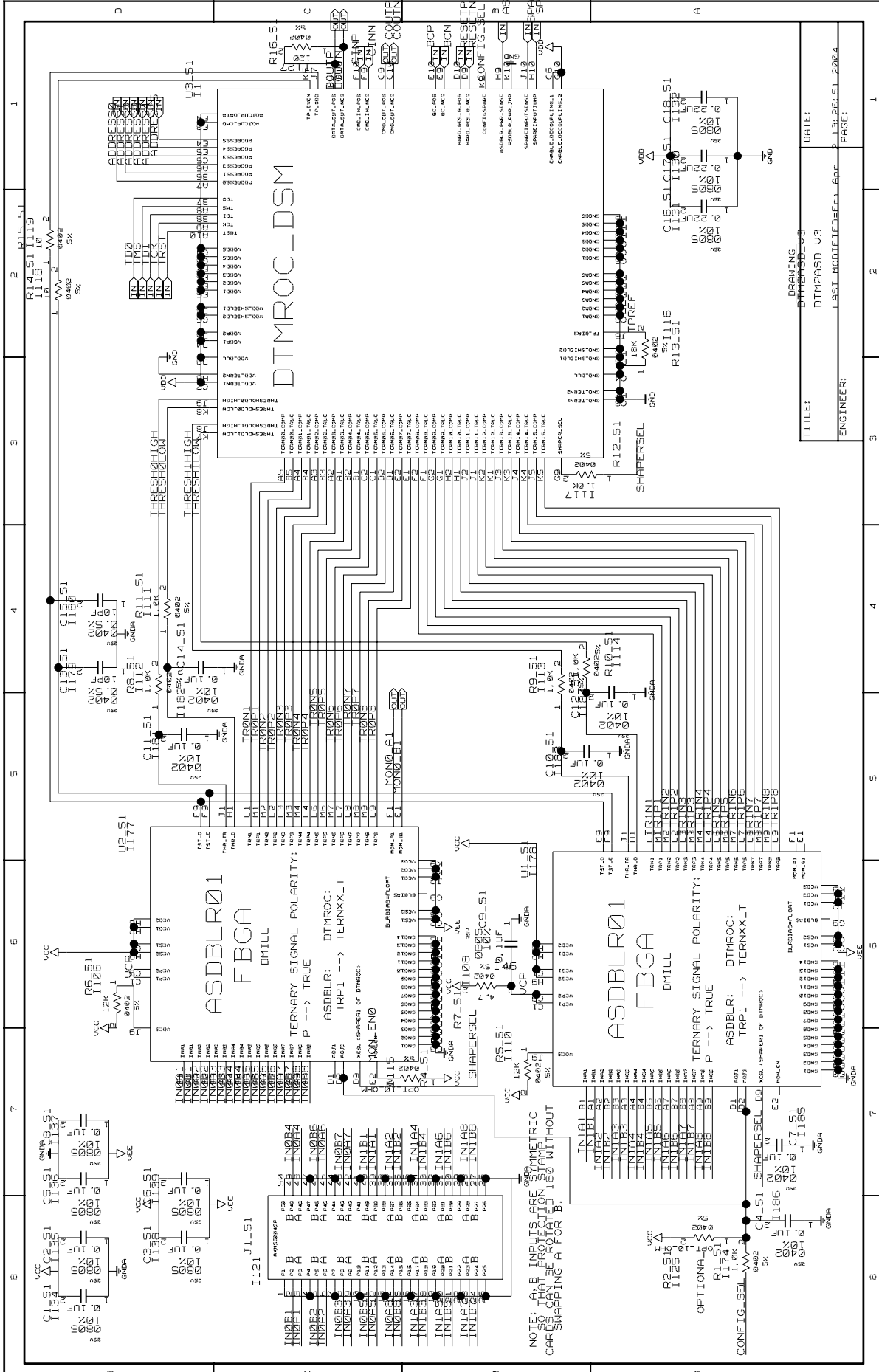
DTMSRD\_V2C



TITLE: DTMROC-V2B  
 DATE: DTMROC-V2B  
 ENGINEER: LAST MODIFIED=ET-1-APP  
 PAGE: 13:20:06-2004

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED 180 WITHOUT  
 SWAPPING A FOR B

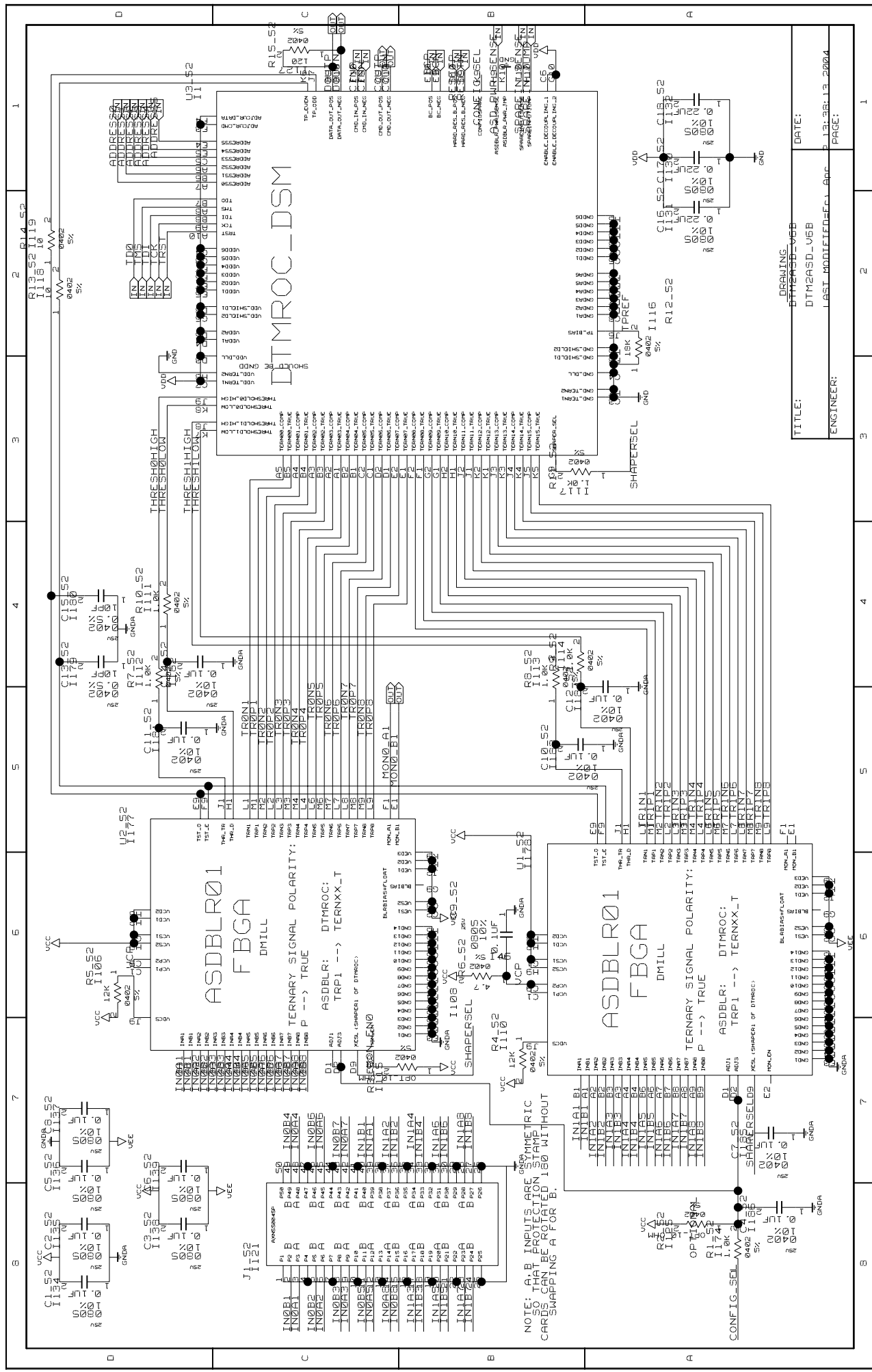
CONFIG\_SEL  
 R7-48  
 U11-48  
 U12-48  
 U13-48  
 U14-48  
 U15-48  
 U16-48  
 U17-48  
 U18-48  
 U19-48  
 U20-48  
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 U86-48  
 U87-48  
 U88-48  
 U89-48  
 U90-48  
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 U92-48  
 U93-48  
 U94-48  
 U95-48  
 U96-48  
 U97-48  
 U98-48  
 U99-48  
 U100-48



TITLE: DTMROC\_DSM  
 DTMEASD\_V3  
 ENGINEER: LAST MODIFIED: EFL\_APC  
 DATE: 13-SEP-51-2004  
 PAGE:

1 2 3 4 5 6 7 8  
 DTMROC\_DSM  
 DTMEASD\_V3  
 LAST MODIFIED: EFL\_APC  
 13-SEP-51-2004





DTMROC-DSM

ASDBLR01  
FBGA  
DMILL

ASDBLR01  
FBGA  
DMILL

DTMROC-DSM

**NOTE:** A, B INPUTS ARE SYMMETRIC  
CAPS CAN BE GATED 180 WITHOUT  
SWAPPING A FOR B

**CONFIG\_SEL**  
PULL UP  
0.5K  
R17-S2  
0.5K  
VCC

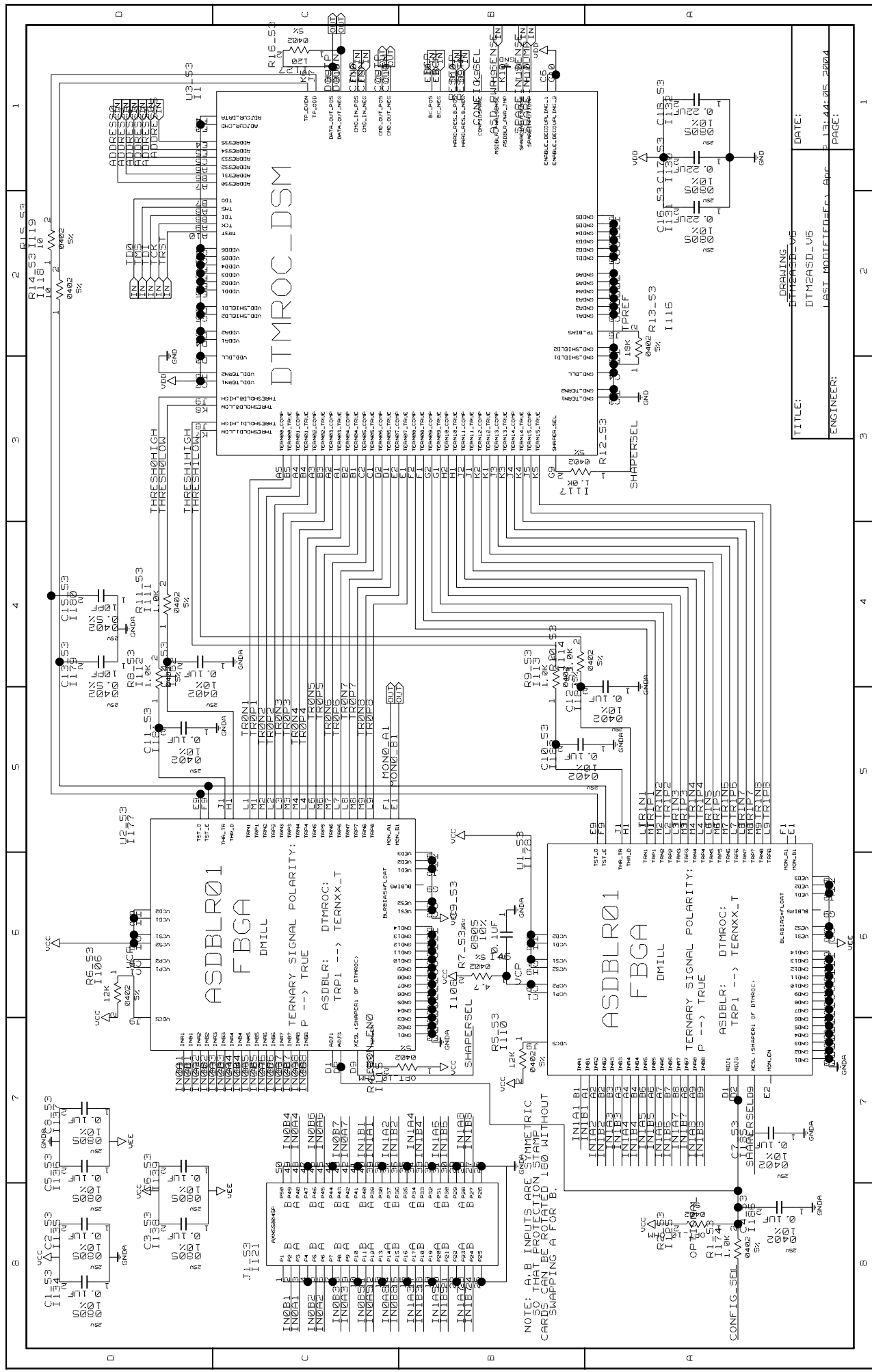
**SHAPERSEL**  
PULL UP  
10K  
R4-S2  
VCC

**MONOSEL1**  
PULL UP  
10K  
R3-S2  
VCC

**SHAPERSEL**  
PULL UP  
10K  
R3-S2  
VCC

TITLE: DTMROC-V06  
DTMROC-V06

ENGINEER: LAST MODIFIED BY: App  
DATE: 13-06-13 2004  
PAGE: 1



TITLE: DTMROC-DSM-V6  
 DTMROD-V6  
 ENGINEER: LAST MODIFIED=ET-1-APP-13:44:05-2004  
 DATE:

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED TO GND WITHOUT  
 SWAPPING A FOR B

DTMROC-DSM

ASDBLR01  
FBGA  
DMILL

ASDBLR01  
FBGA  
DMILL

TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMROC;  
 TRP1 --> TERNXX-T  
 P --> TRUE  
 (KEL: SHAPER1 OF DTROC)

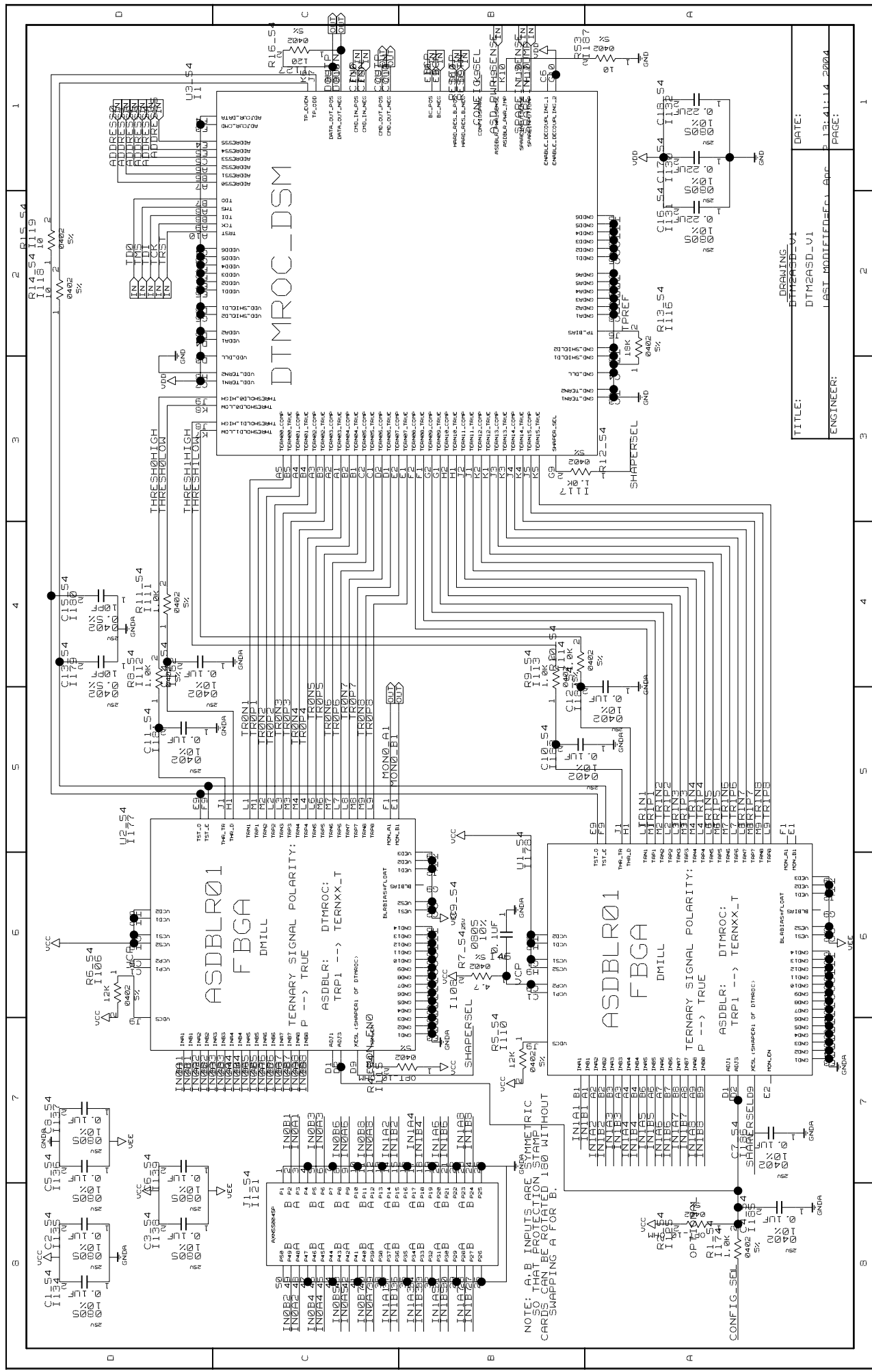
TERNARY SIGNAL POLARITY:  
 ASDBLR: DTMROC;  
 TRP1 --> TERNXX-T  
 P --> TRUE  
 (KEL: SHAPER1 OF DTROC)

J1121  
 IN0B1  
 IN0B2  
 IN0B3  
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 IN0B100

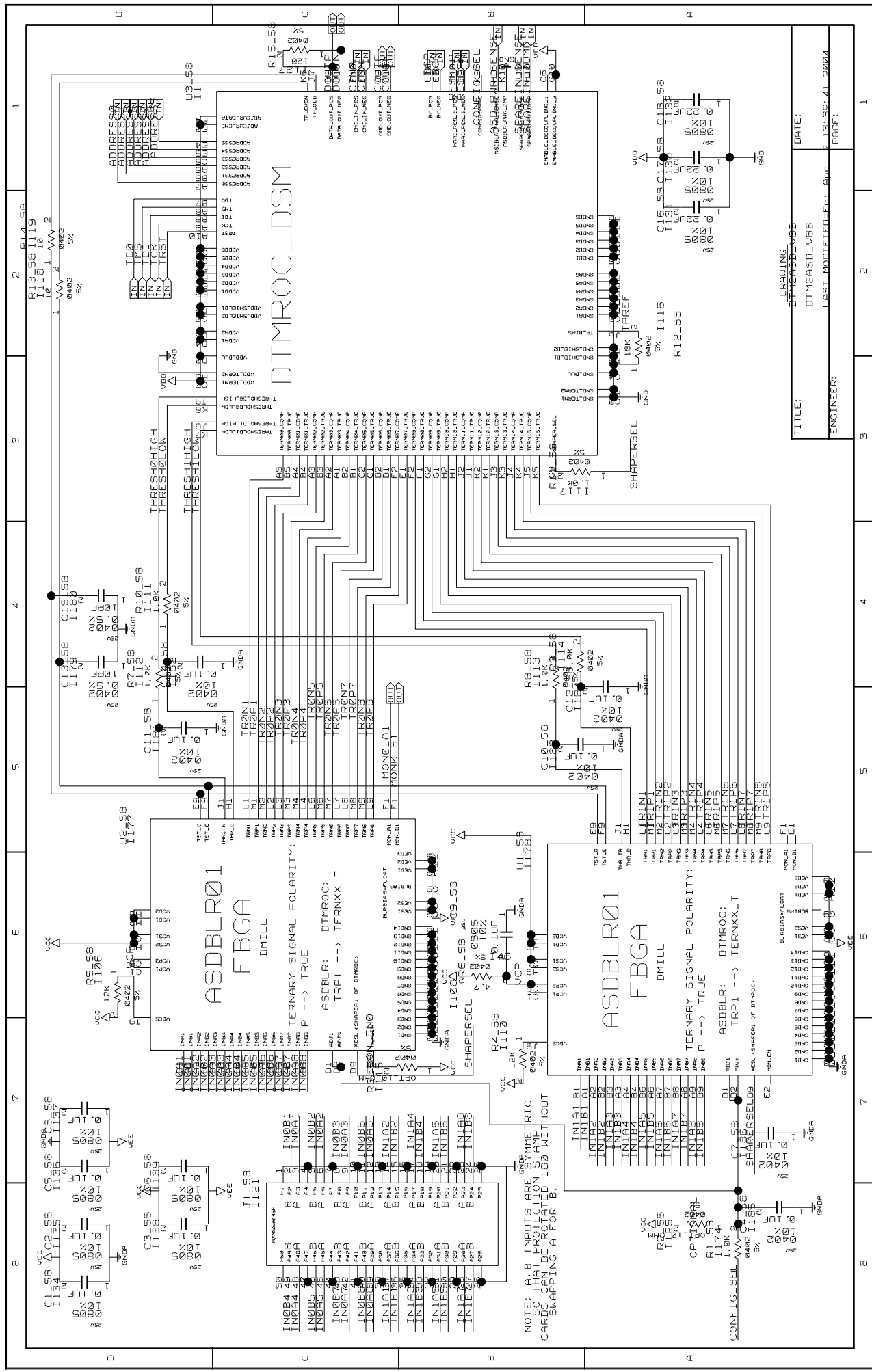
J1122  
 IN1A1  
 IN1A2  
 IN1A3  
 IN1A4  
 IN1A5  
 IN1A6  
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 IN1A9  
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J1123  
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J1124  
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 IN1A100



TITLE: DTMR05B-V1  
 ENGINEER: DTMR05D-V1  
 DATE: 13:41:14 2004  
 PAGE: 1



DTMROC\_DSM

AD5BLR01  
FBGA  
DMILL

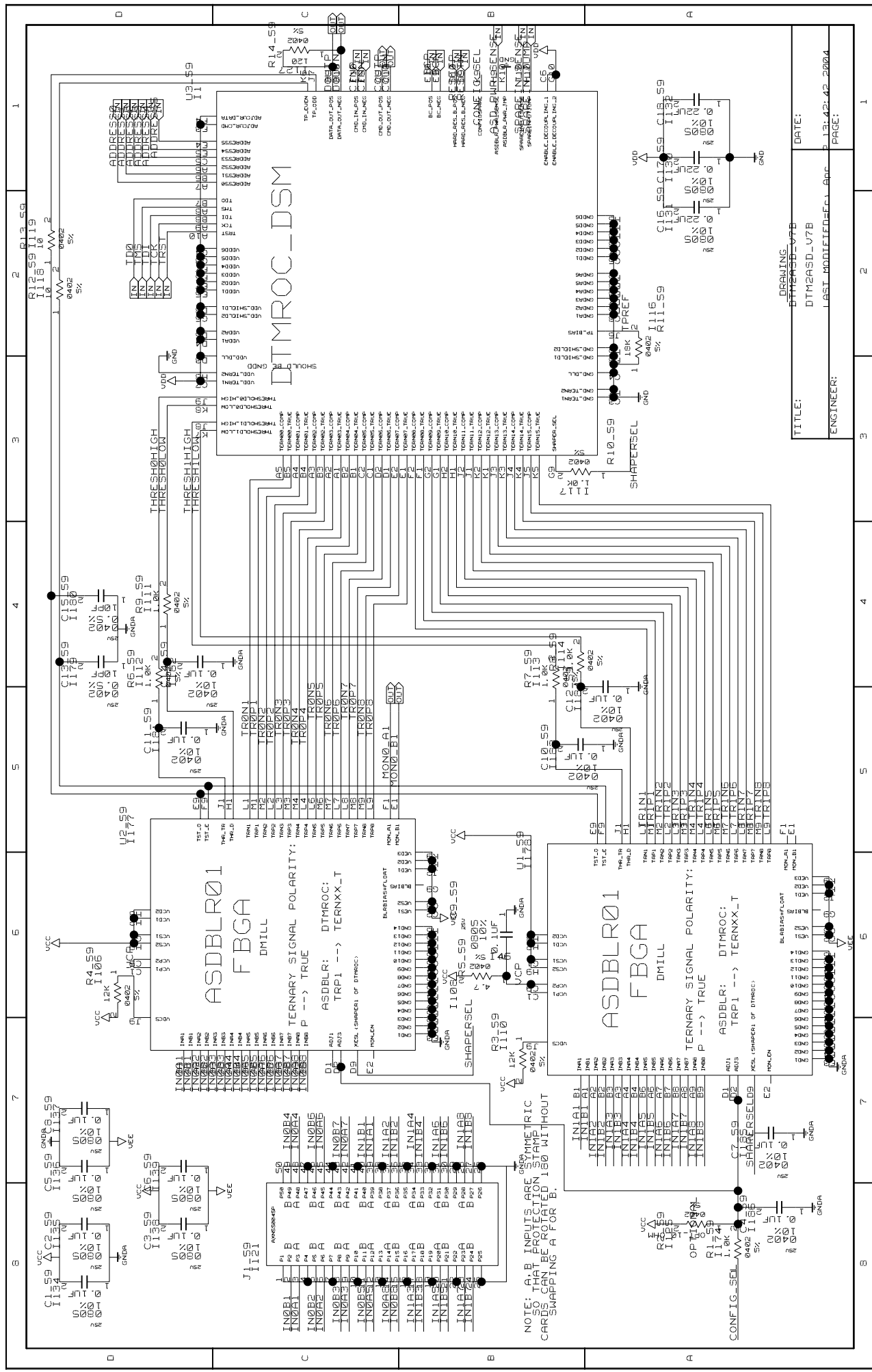
AD5BLR01  
FBGA  
DMILL

TERNARY SIGNAL POLARITY:  
ASDBLR: DTMROC;  
TRP1 --> TERNXX-T

TERNARY SIGNAL POLARITY:  
ASDBLR: DTMROC;  
TRP1 --> TERNXX-T

NOTE: A, B INPUTS ARE SYMMETRIC  
CAPS CAN BE GATED ON OR OFF WITHOUT  
SWAPPING A FOR B

DRAWING: DTMROC-V08  
TITLE: DTMROC\_V08  
DATE: 13:30:41 2004  
ENGINEER: LAST MODIFIED=...



TITLE: DTMROC-DSM  
 DRAWING: DTMROC-DSM-V7B  
 DATE: 13:42:43 2004  
 ENGINEER: LAST MODIFIED=ET-1  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COFFSET 180 WITHOUT  
 SWAPPING A FOR B

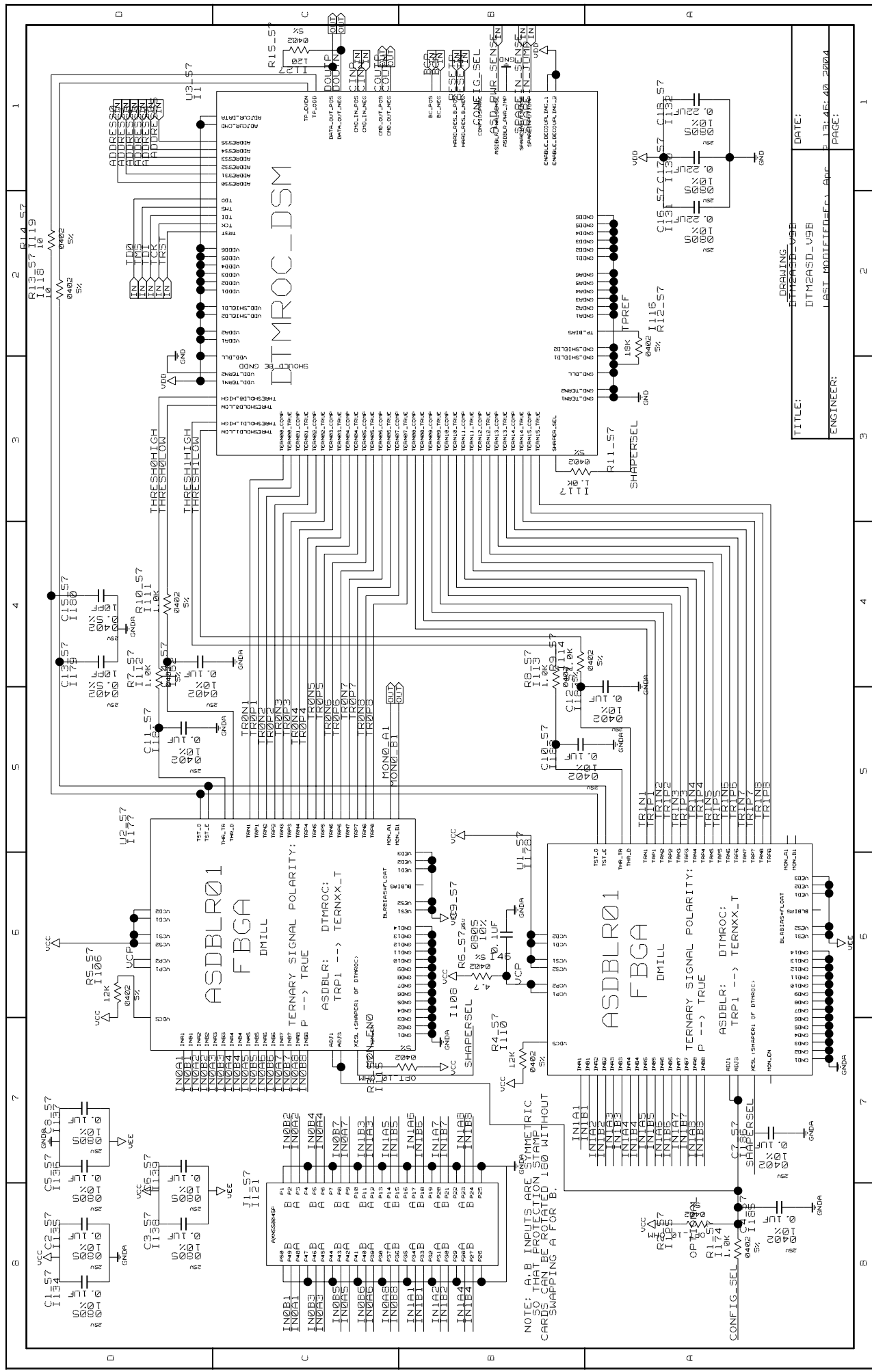
CONFIG\_SEL  
 1.9K  
 0402  
 1174

J1121  
 IN0B1  
 IN0B2  
 IN0B3  
 IN0B4  
 IN0B5  
 IN0B6  
 IN0B7  
 IN0B8  
 IN0B9  
 IN0B10  
 IN0B11  
 IN0B12  
 IN0B13  
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 IN0B88  
 IN0B89  
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 IN0B95  
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 IN0B97  
 IN0B98  
 IN0B99  
 IN0B100

ASDBLR01  
 FBGA  
 DMILL  
 TERNARY SIGNAL POLARITY:  
 P --> TRUE  
 ASDBLR: DTMROC;  
 TRP1 --> TERNXX-T  
 XEL (SHAPER) OF DTROC;  
 NON-FL  
 SHAPERSEL  
 110K  
 0402  
 VCC  
 1177  
 1.0K  
 0402  
 GND

ASDBLR01  
 FBGA  
 DMILL  
 TERNARY SIGNAL POLARITY:  
 P --> TRUE  
 ASDBLR: DTMROC;  
 TRP1 --> TERNXX-T  
 XEL (SHAPER) OF DTROC;  
 NON-FL  
 SHAPERSEL  
 110K  
 0402  
 VCC  
 1177  
 1.0K  
 0402  
 GND

DTMROC-DSM  
 SHAPERSEL  
 1.0K  
 0402  
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 TRP1  
 1.0K  
 0402  
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 1.0K  
 0402  
 GND  
 TRP3  
 1.0K  
 0402  
 GND  
 TRP4  
 1.0K  
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TITLE: DTMROC\_DSM\_V9B  
 DATE: 13-14-10  
 ENGINEER: LAST  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED 180° WITHOUT  
 SWAPPING A FOR B

CONFIG\_SEL  
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OP\_AMP  
 1.9K  
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