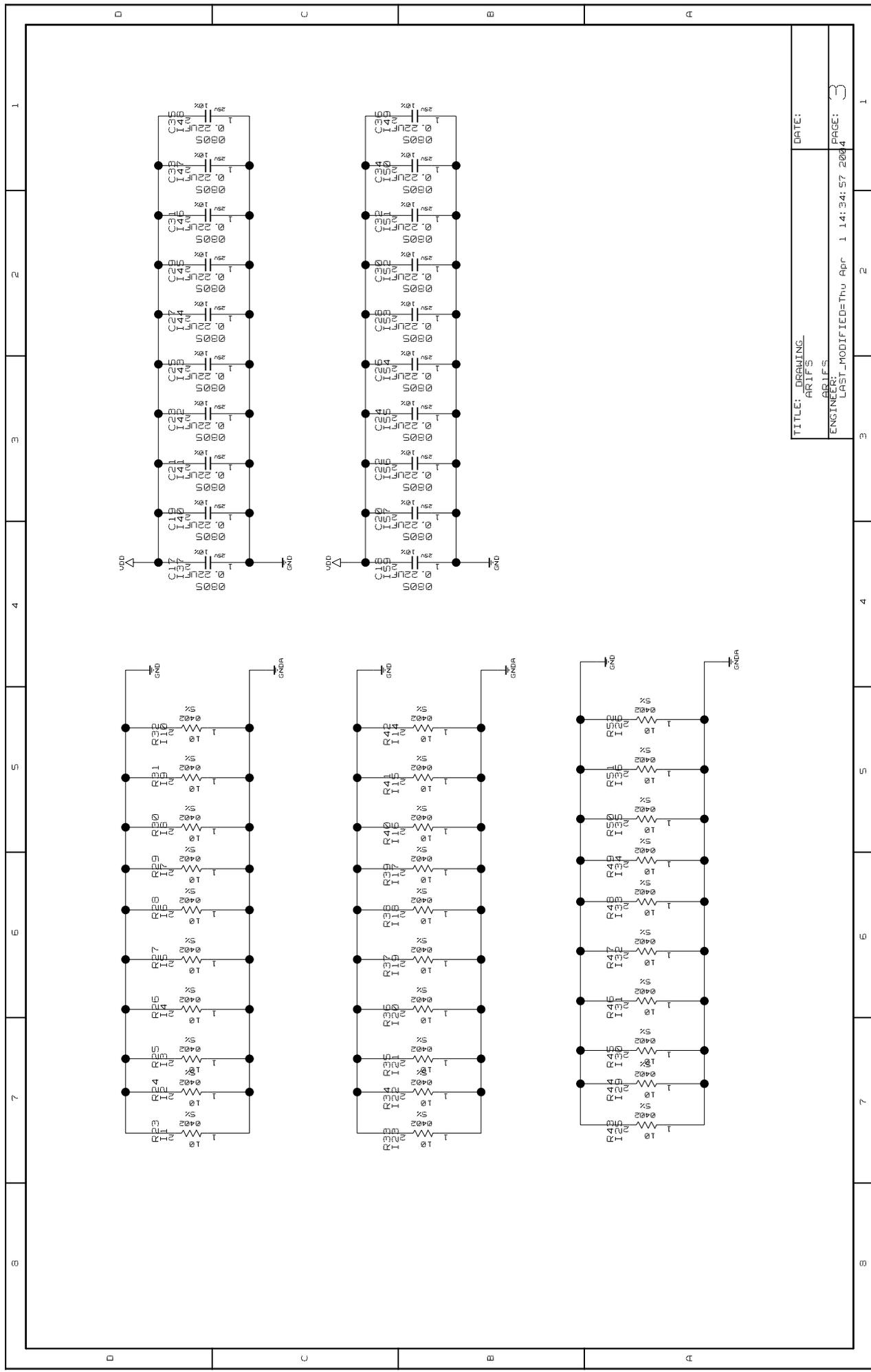
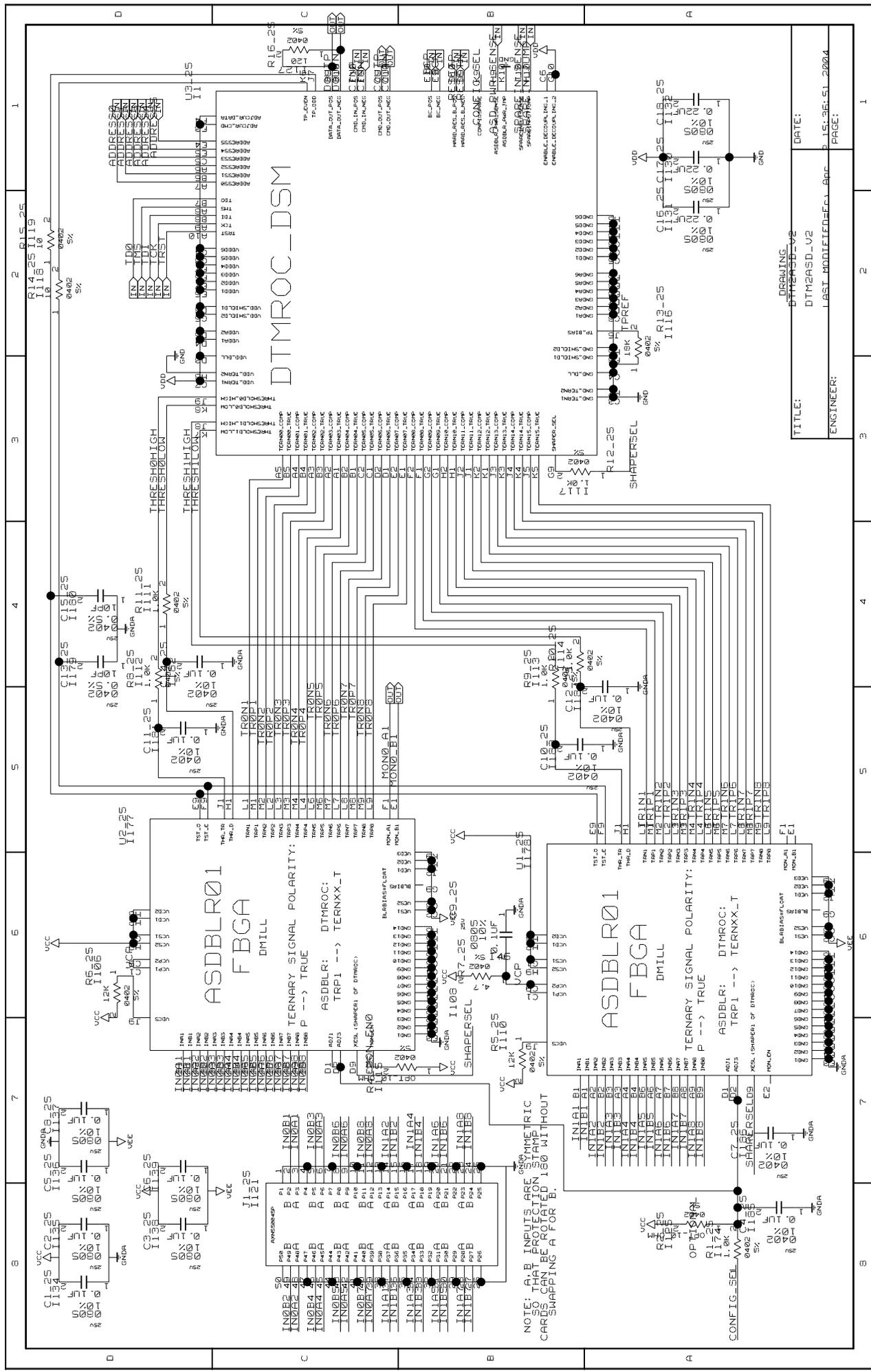


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 ENGINEER: AR1FS  
 DATE:   
 LAST\_MODIFIED=Fr1 Apr 2 15:46:01 2004  
 PAGE: 1



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 LAST\_MODIFIED=Thu Apr 1 14:54:57 2004  
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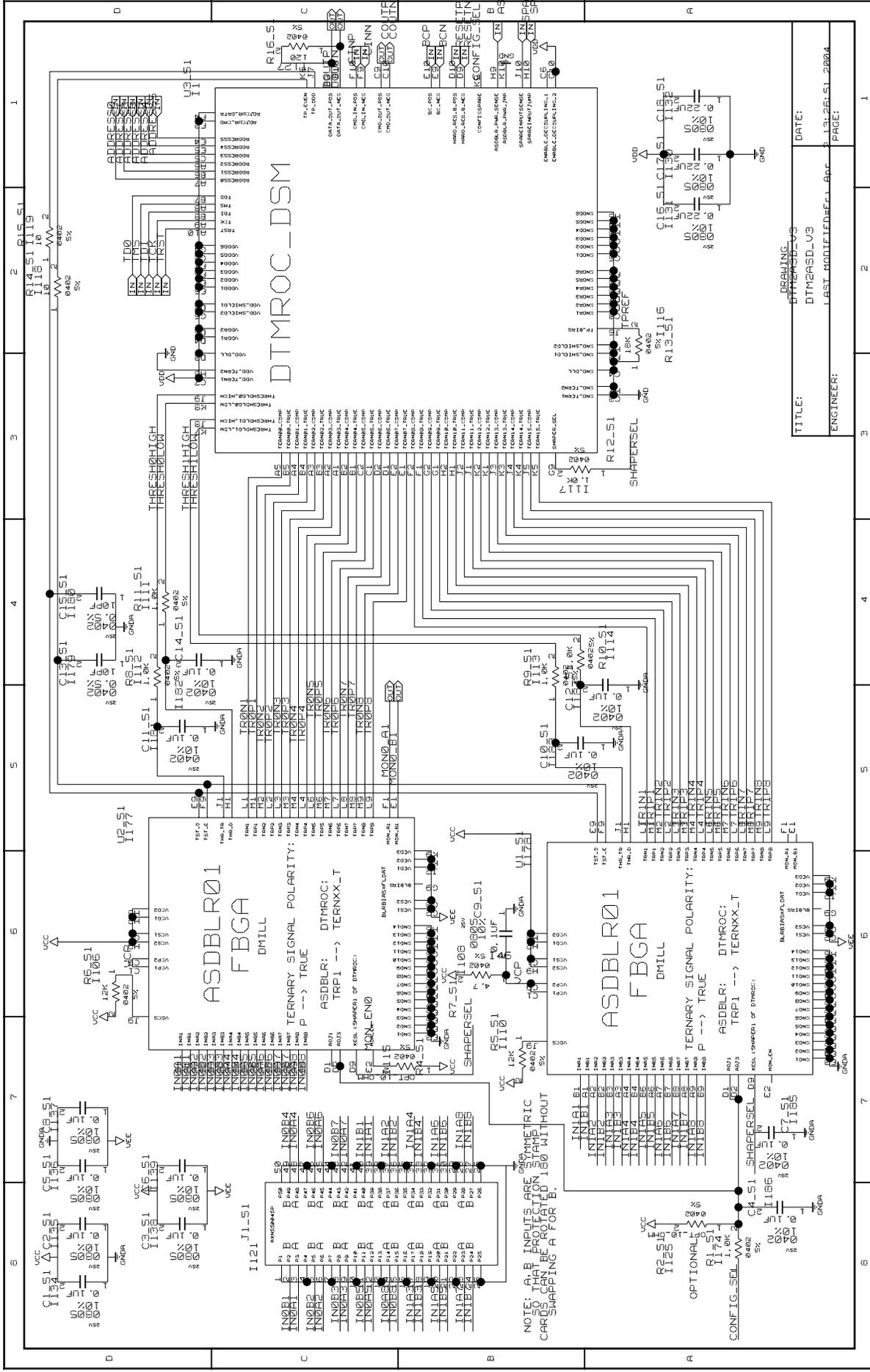




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NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED 180 WITHOUT  
 SWAPPING A FOR B

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DTMROC\_DSM

ASDBLR01 FBGA DMILL  
 TERNARY SIGNAL POLARITY: P --> TRUE  
 ASDBLR: DTMROC  
 TRP1 --> TERNXX\_T  
 XSEL (SUPPORT OF DTMROC):  
 MON-LEN0

ASDBLR01 FBGA DMILL  
 TERNARY SIGNAL POLARITY: P --> TRUE  
 ASDBLR: DTMROC  
 TRP1 --> TERNXX\_T  
 XSEL (SUPPORT OF DTMROC):  
 MON-LEN0

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NOTE: A:B INPUTS ARE ASYMMETRIC  
 SO THAT PROTECTION IS PROVIDED  
 WITHOUT SWAPPING A FOR B.

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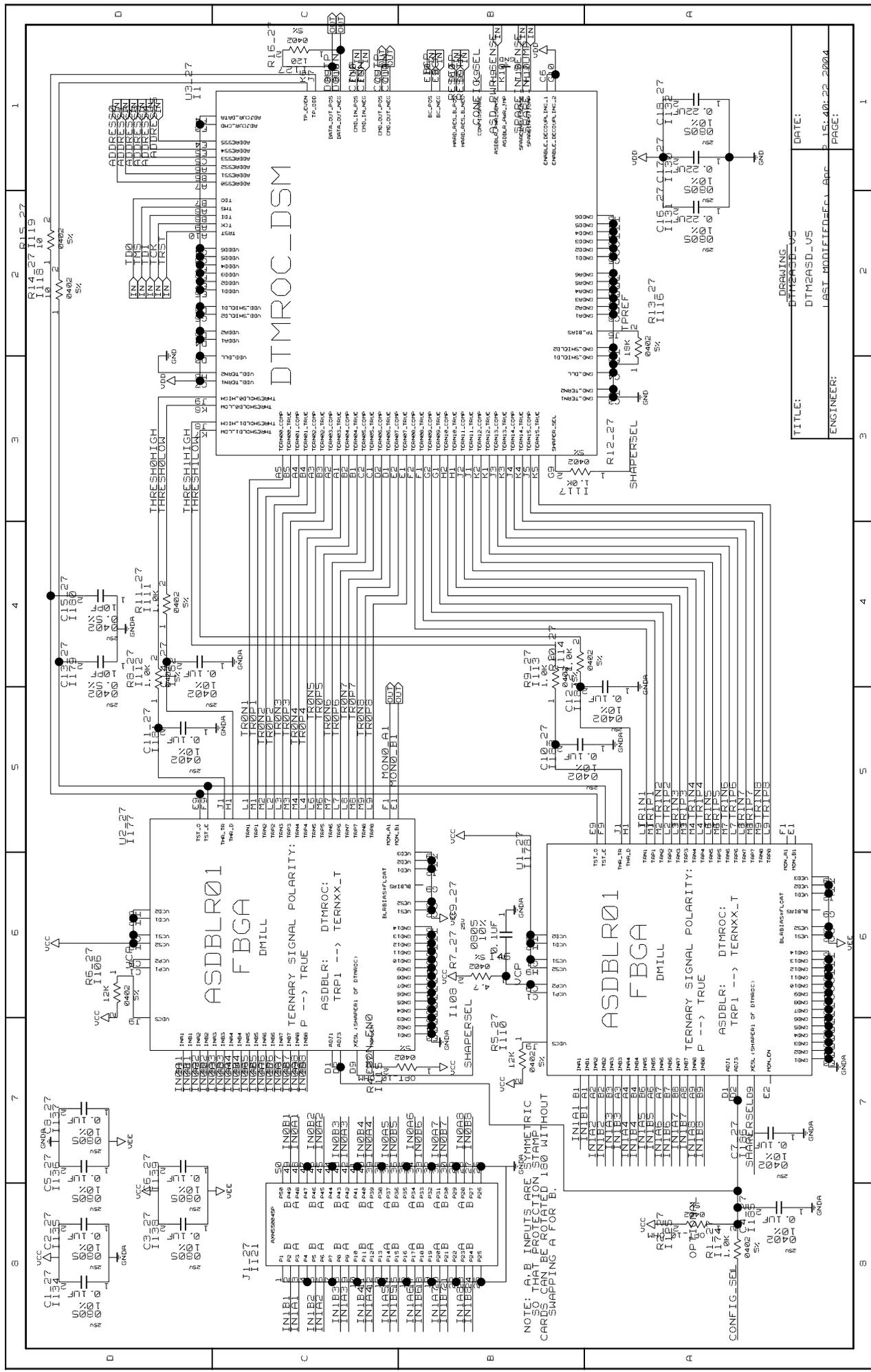
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 MON-LEN0

ASDBLR01 FBGA DMILL  
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TITLE: DTMROC-DSM  
 ENGINEER: DTMROC-DSM  
 DATE: 15:40:23 2004  
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NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED 180 WITHOUT  
 SWAPPING A FOR B

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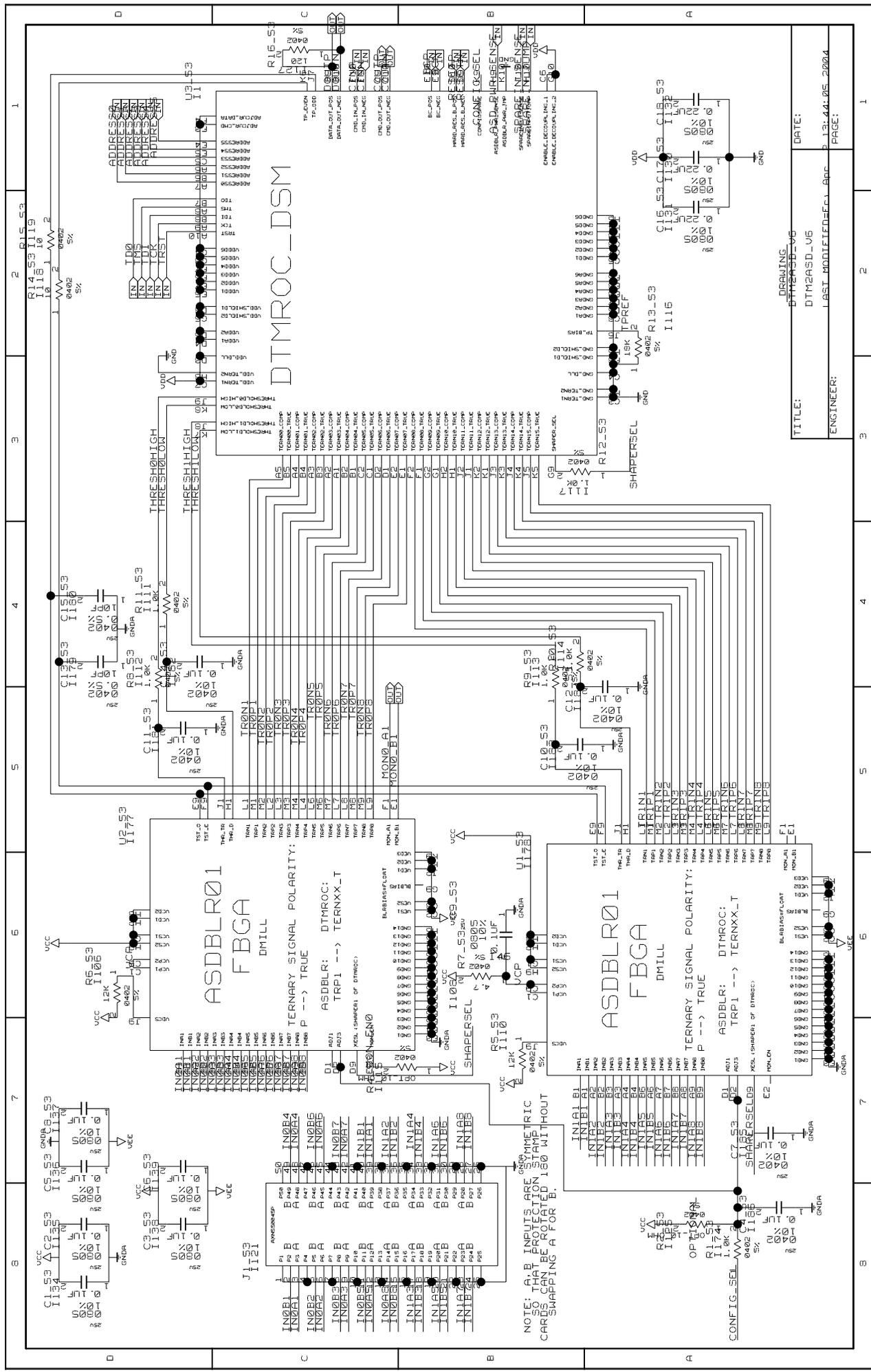
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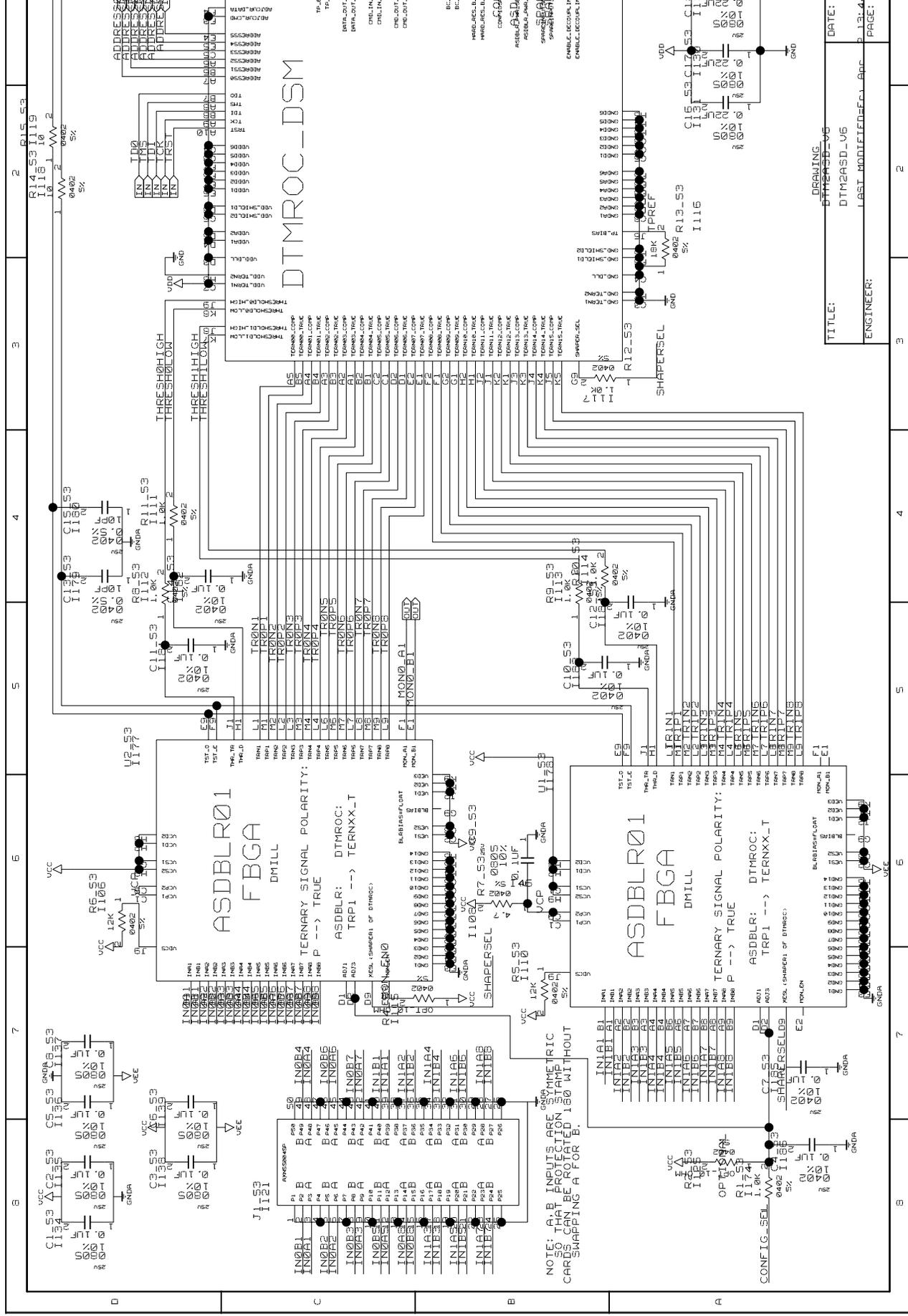
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DTMROC\_DSM

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ASDBLR01  
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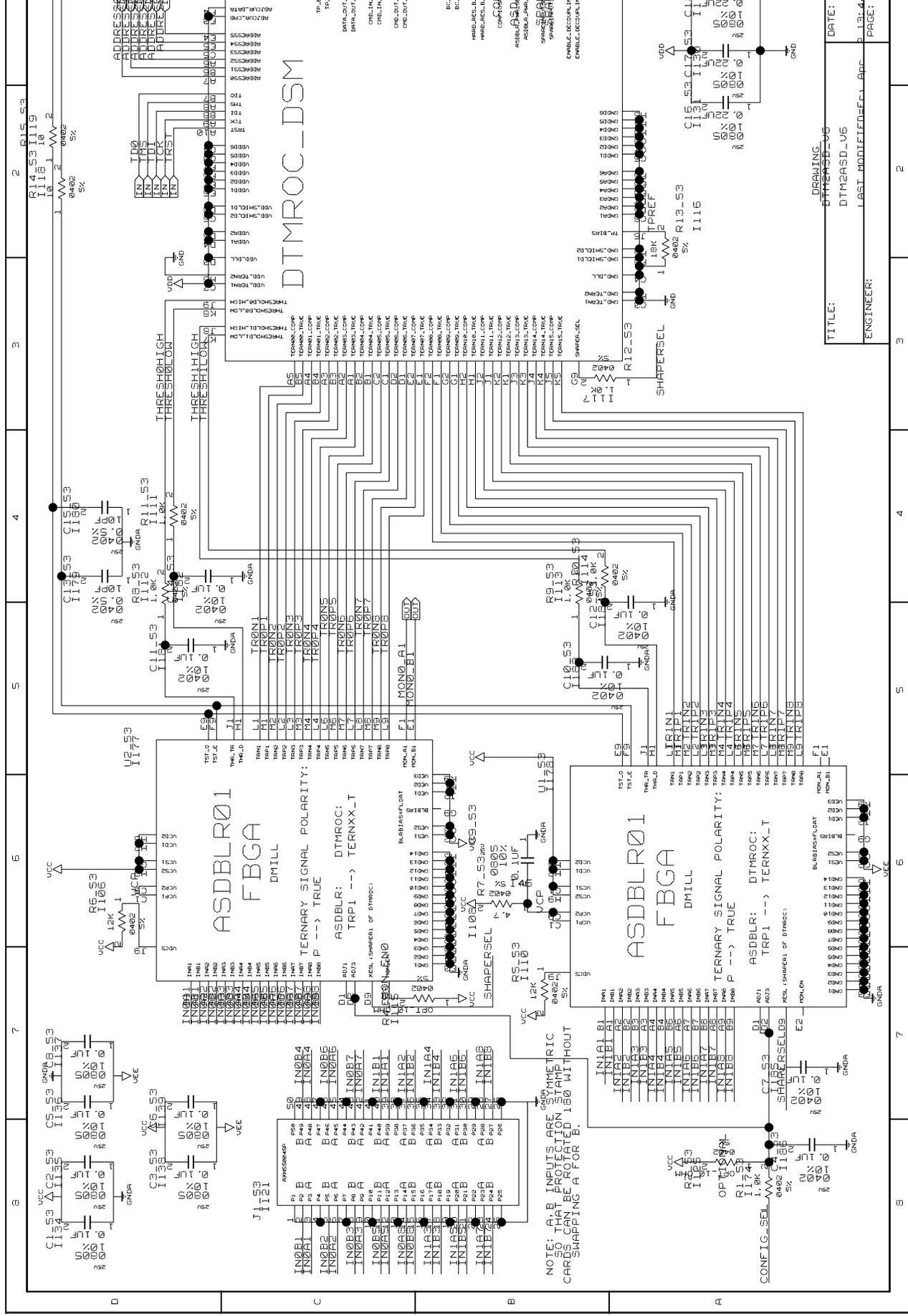
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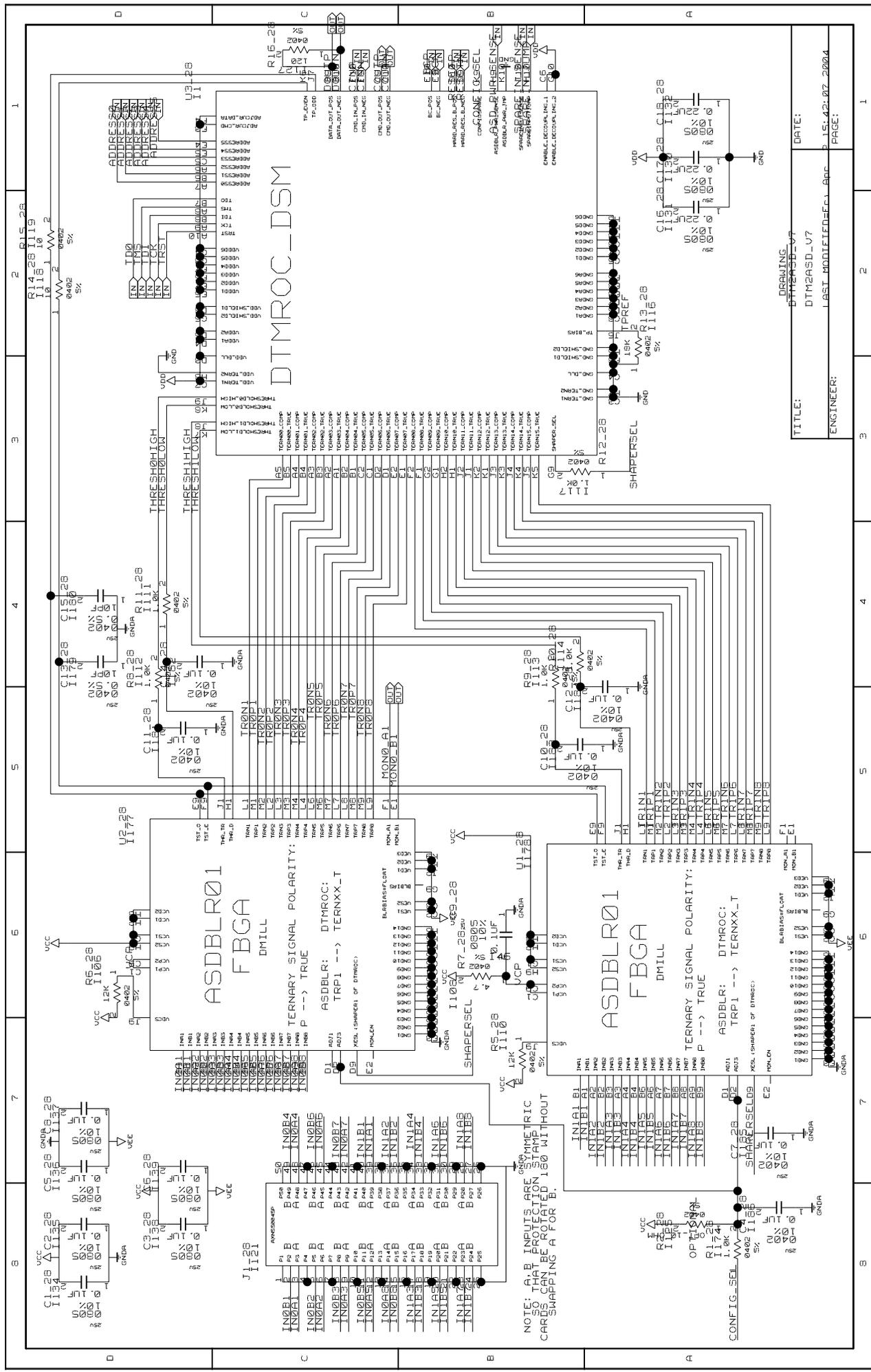
NOTE: A, B INPUTS ARE SYMMETRIC  
 CAPS CAN BE COUPLED TO EITHER  
 SWAPPING A FOR B

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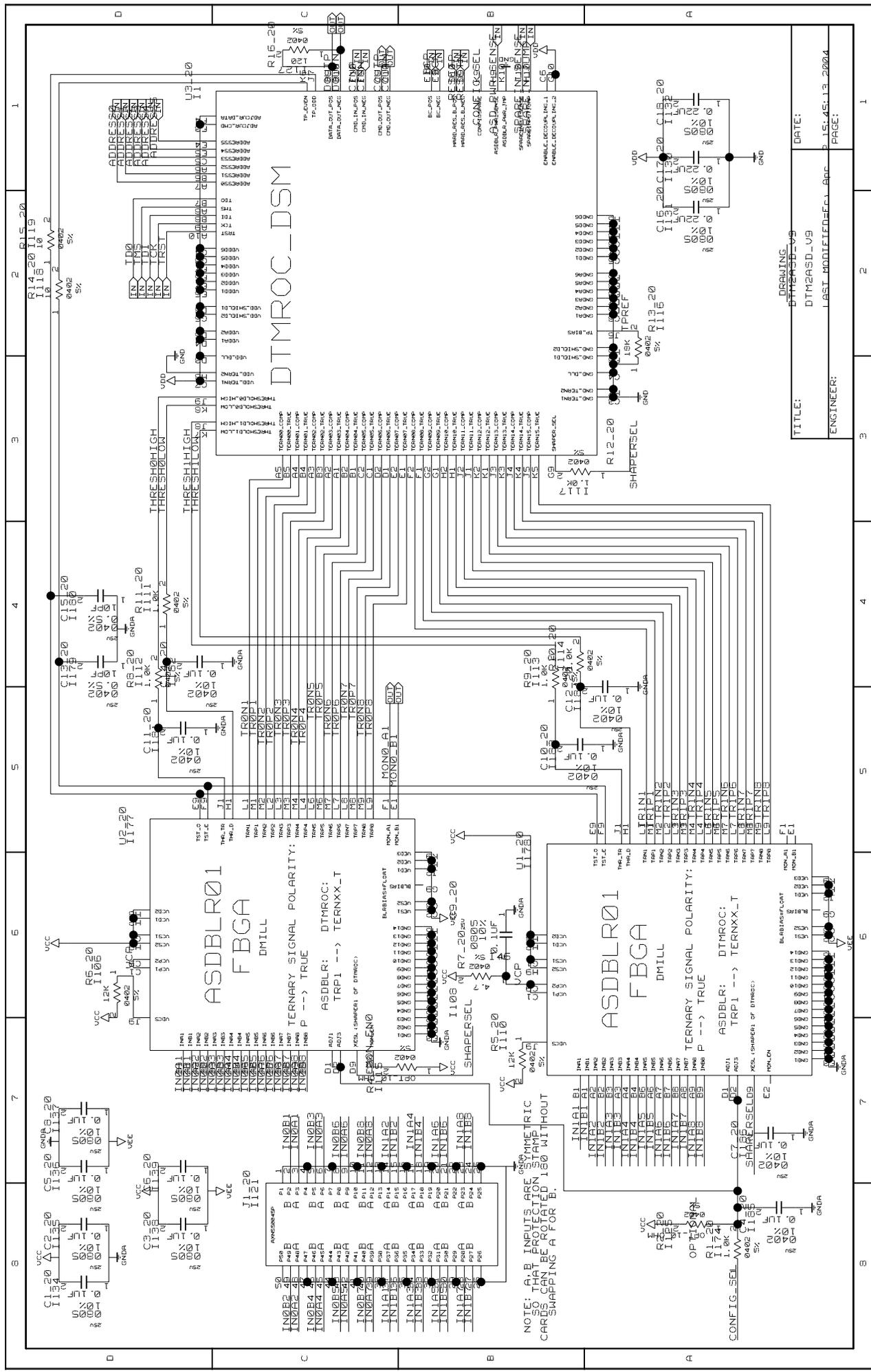
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TITLE: DTMROASD-V7  
 ENGINEER: DTMROASD-V7  
 DATE: 15:42:07 2004  
 PAGE: 1





TITLE: DTMROC-DSM  
 ENGINEER: DTMROSD\_V9  
 DATE: 15.45.13.2004  
 PAGE: 1

NOTE: A, B INPUTS ARE SYMMETRIC CAPS CAN BE GATED ON FAITH WITHOUT SWAPPING A FOR B

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