

AR3BS1

#3

November 19, 2004

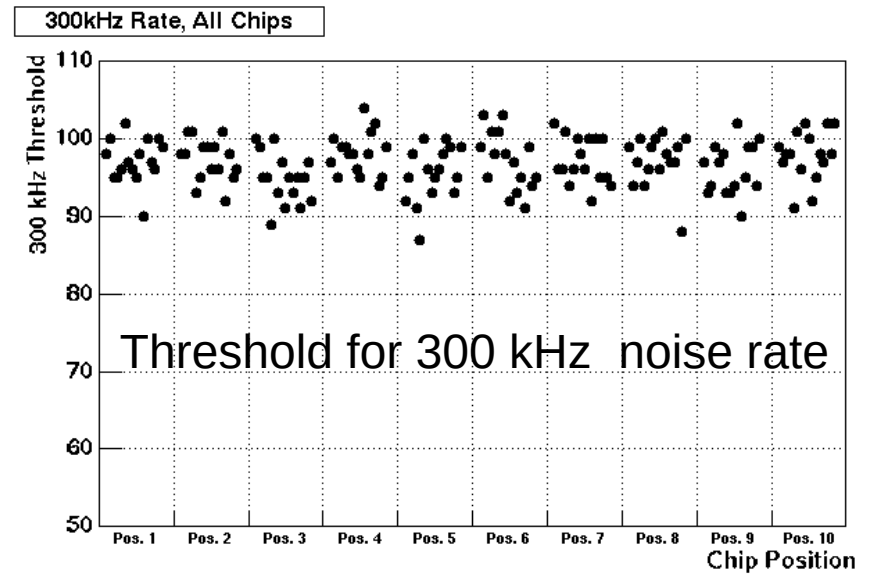
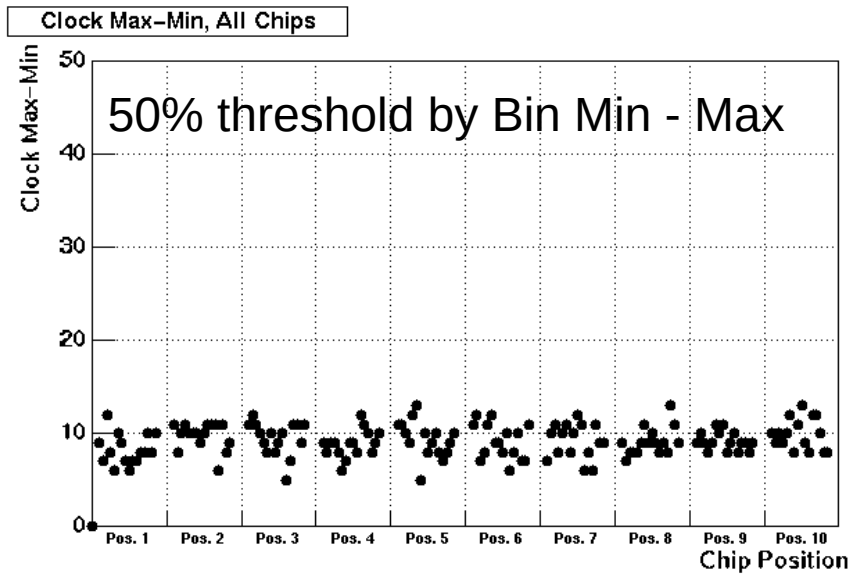
Mitch and Anton

Measurements

- DLL Lock works in all positions
- Timing scan shows expected ranges of BX and DX operation
- Voltage and temp measurement TBD

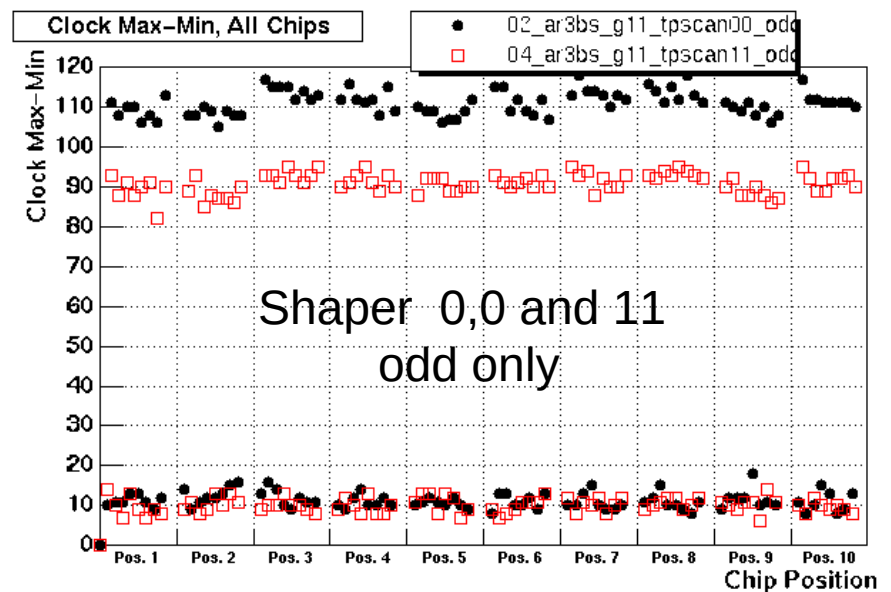
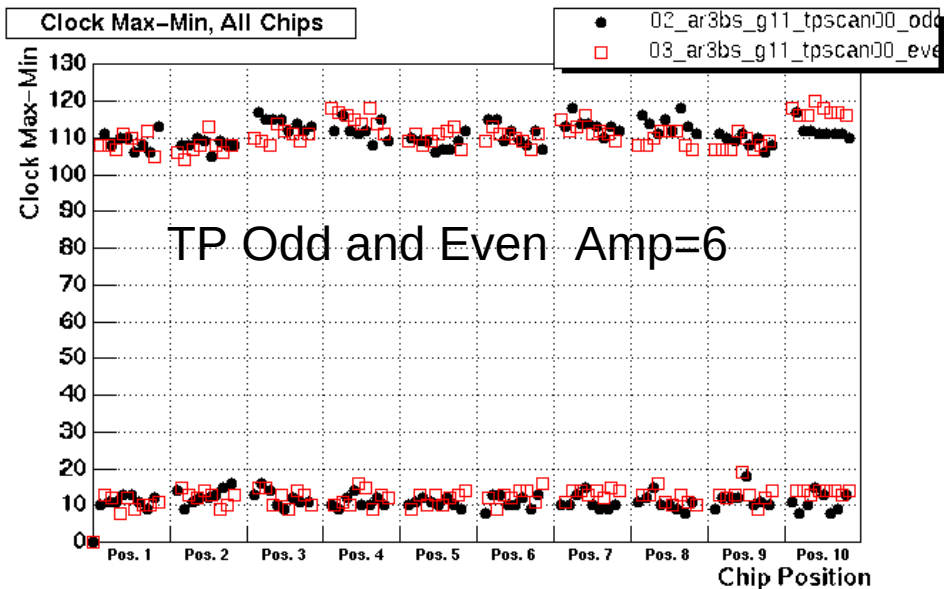
3BS1 Threshold Ramp

All positions except @#11



** note that position @#11 although not shown,
works for similarly to the others. Data is available.

3BS1 Test Pulse



Data from VT tests and DLL Lock

- | AR3BS_g1 | Temp | Vdd | Vcc | Vee |
|------------|------|-----|-----|---------------------|
| @(10) @(x) | | | | |
| 1 1 | 128 | 188 | 256 | 255 |
| 2 2 | 128 | 189 | 256 | 255 |
| 3 3 | 125 | 184 | 256 | 255 |
| 4 4 | 126 | 185 | 256 | 255 |
| 5 5 | 125 | 184 | 228 | 114 ← +/-3 monitor |
| 6 6 | 127 | 187 | 256 | 255 |
| 7 7 | 127 | 187 | 256 | 255 |
| 8 8 | 128 | 188 | 256 | 255 |
| 9 9 | 127 | 186 | 256 | 255 |
| 10 a | 128 | 187 | 232 | 115 ← +/-3V monitor |
| 11 b | 129 | 189 | 256 | 255 |

=====DONE=====

DLL_lock for AR3BS_g1 OK:

0: 1 1 1 1 1 1 1 1 1 1

1: 1 1 1 1 1 1 1 1 1 1

3BS1 Timing Scans

- Total chips per delay with 100% success rate clock edge = 1

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	11	11	8	8	9	11	11	11	11	1	11	11	11
2	11	11	8	8	10	11	11	11	11	11	1	11	11
4	11	11	8	8	9	11	11	11	11	11	10	1	11
6	11	11	8	8	10	11	11	11	11	11	11	11	2
8	-	11	8	8	9	11	11	11	11	11	11	11	11
10	11	-	8	8	9	11	11	11	11	11	11	11	11
12	11	11	-	8	9	11	11	11	11	11	11	11	11
14	11	11	8	-	10	11	11	11	11	11	11	11	11
16	11	11	8	8	-	11	11	11	11	11	11	11	11
18	11	11	8	8	9	-	11	11	11	11	11	11	11
20	11	11	8	8	10	11	-	11	11	11	11	11	11
22	11	11	8	8	9	11	11	-	11	11	11	11	11
24	11	11	8	8	9	11	11	11	-	11	11	11	11

- 3BS1
- Total chips per delay with 100% success rate clock edge = 0

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	11	11	11	11	11	11	11	11	9	-	11	11	11
2	11	11	11	11	11	11	11	11	9	10	1	11	11
4	11	11	11	11	11	11	11	11	9	8	10	1	11
6	11	11	11	11	11	11	11	11	9	9	11	11	1
8	-	11	11	11	11	11	11	11	9	9	11	11	11
10	11	-	11	11	11	11	11	11	9	9	11	11	11
12	11	11	-	11	11	11	11	11	9	9	11	11	11
14	11	11	11	-	11	11	11	11	9	10	11	11	11
16	11	11	11	11	-	11	11	11	9	9	11	11	11
18	11	11	11	11	11	-	11	11	9	9	11	11	11
20	11	11	11	11	11	11	-	11	9	10	11	11	11
22	11	11	11	11	11	11	11	-	9	10	11	11	11
24	11	11	11	11	11	11	11	11	-	10	11	11	11