B wheel Board Gain Differences

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Motivation

- Gain differences have been observed for a number of B wheel boards from ALGEN.
- Smallest Division ASD ASIC
- Typical - Board or DTMROC

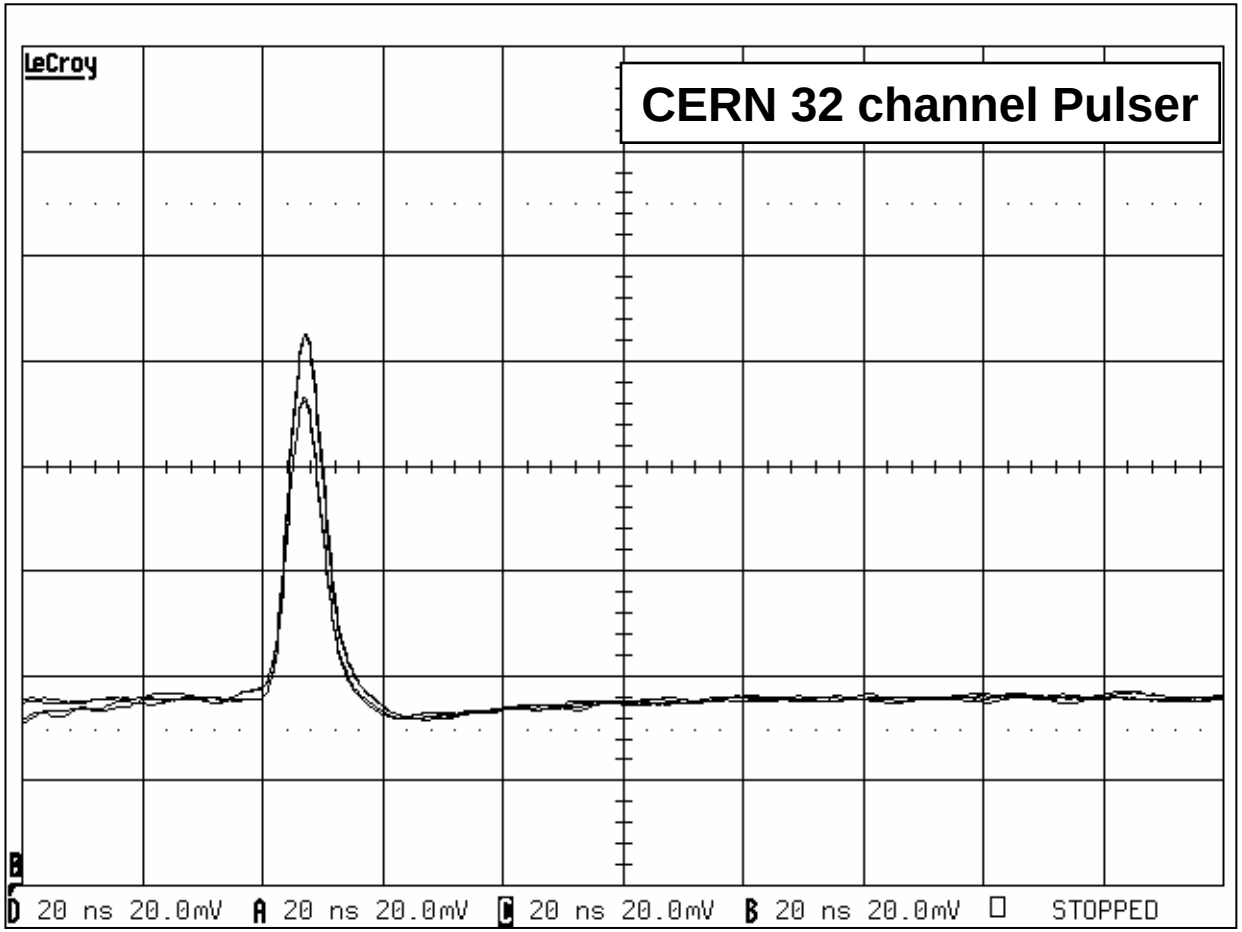
Two boards have been examined in detail.

Board	Chip	Gain
V656	A0053011(d)	Typical
V660	A0156162(d)	Low
V660	A0157867	Low

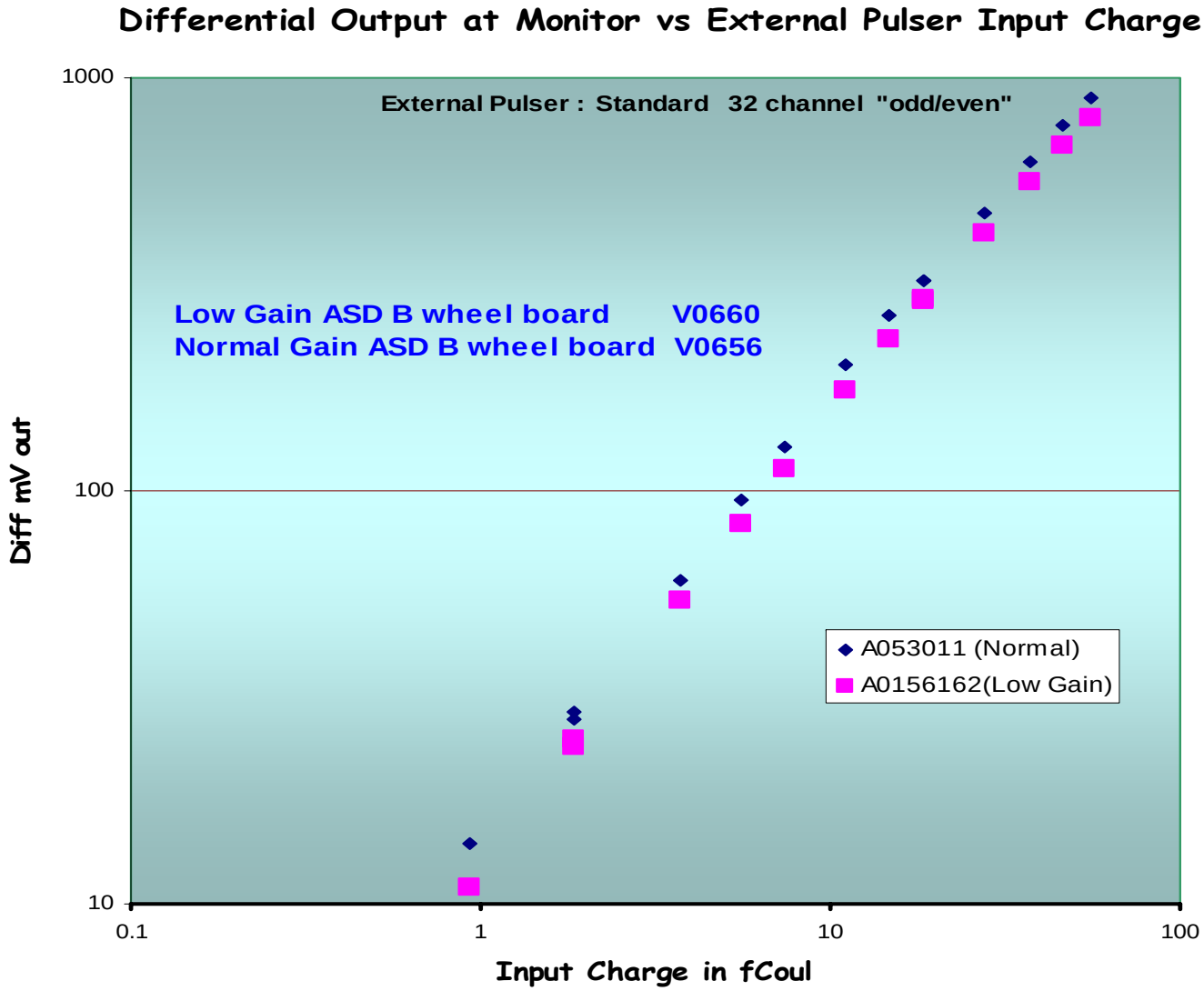
(d) Indicates Chip is oriented below
Silk screen diode symbol.

External Pulser Response at BLR Output

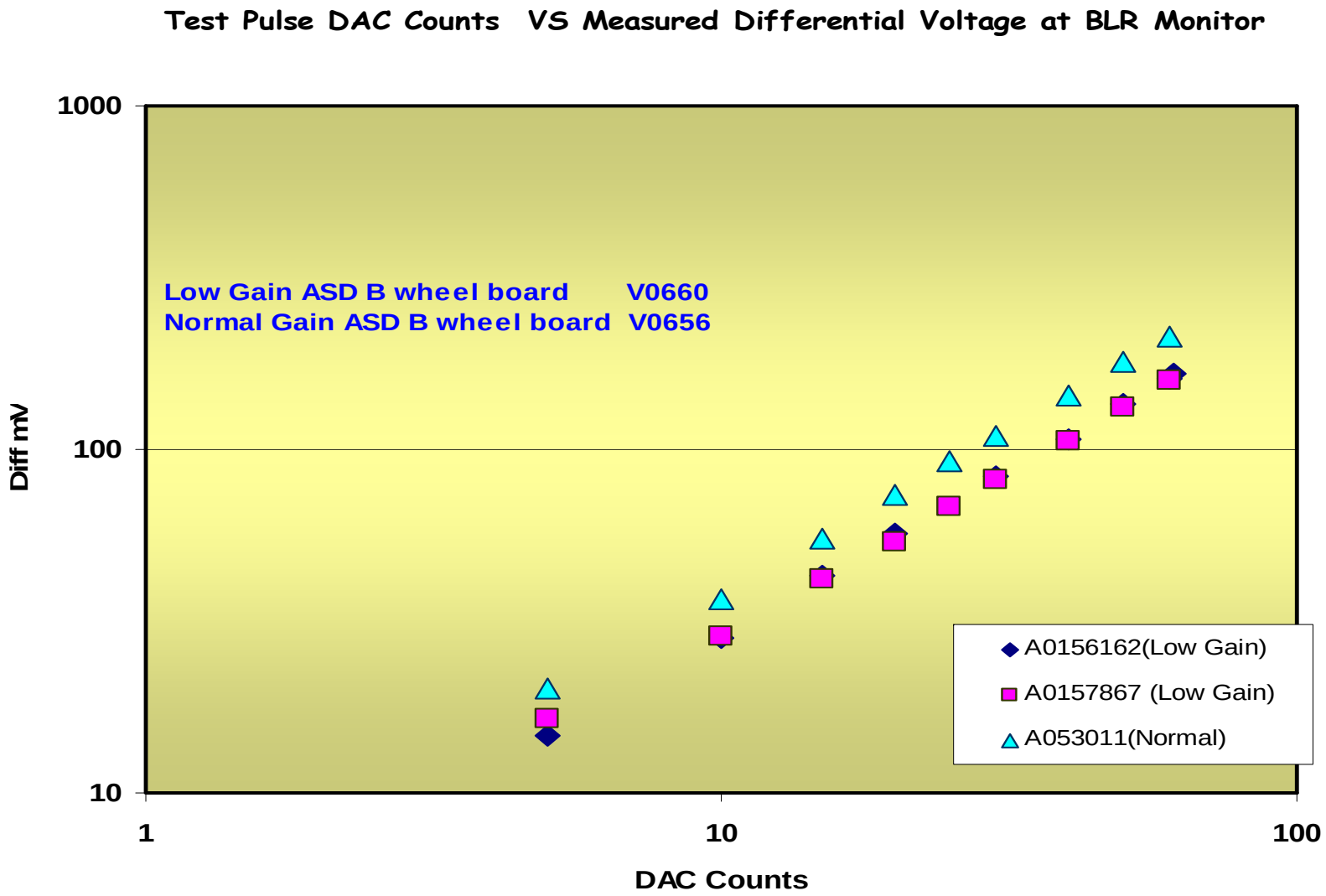
for two low gain and two typical channels 4fC



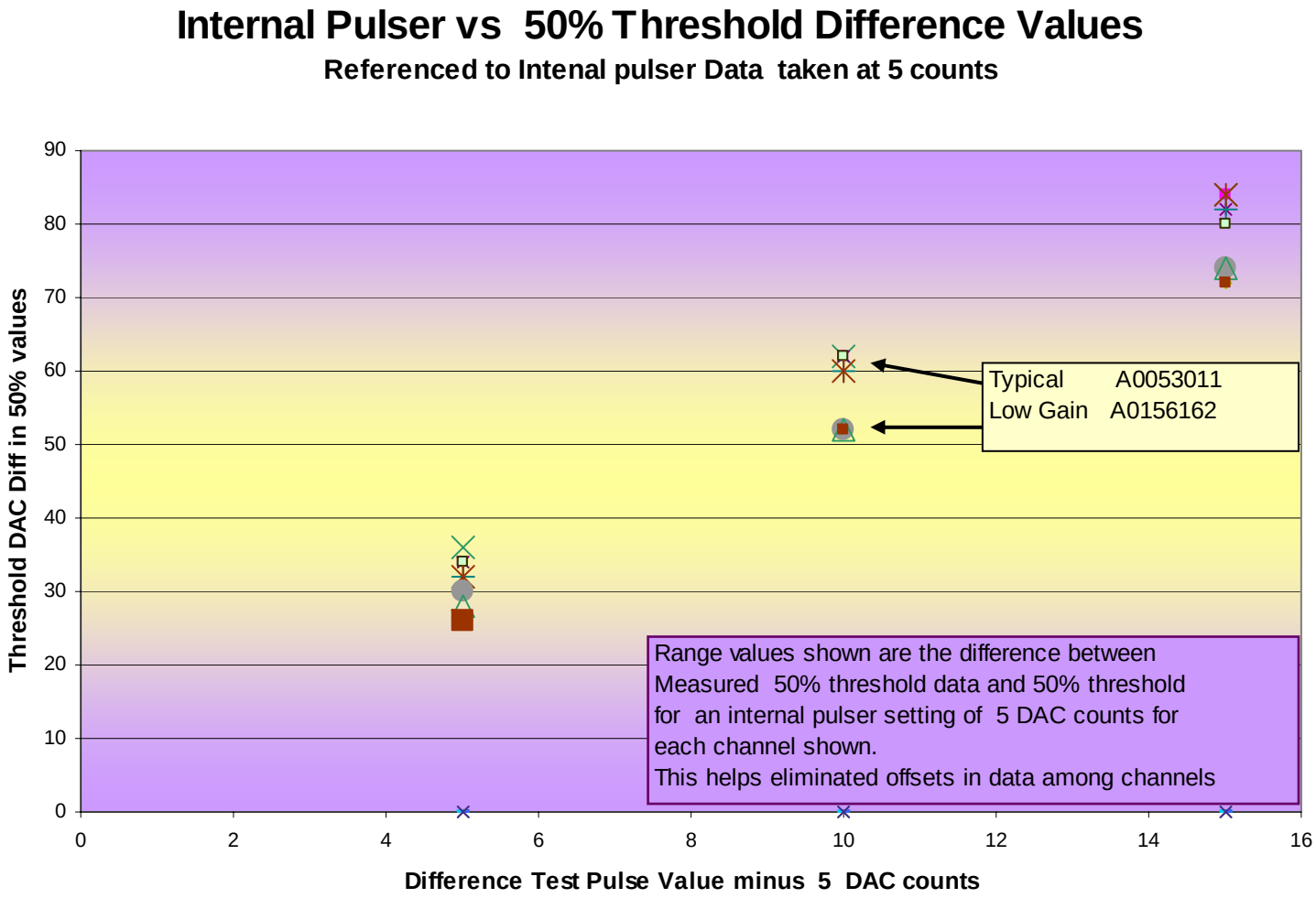
External Pulser → BLR Monitor Out



Internal Pulser → BLR Monitor Out

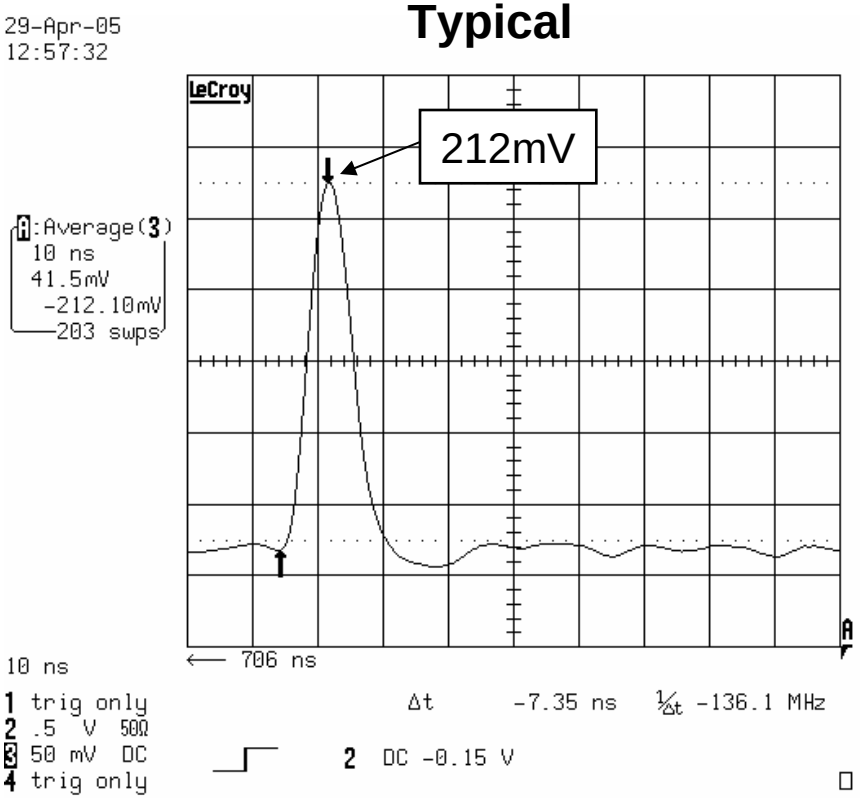


Internal Pulser to 50% DAC threshold

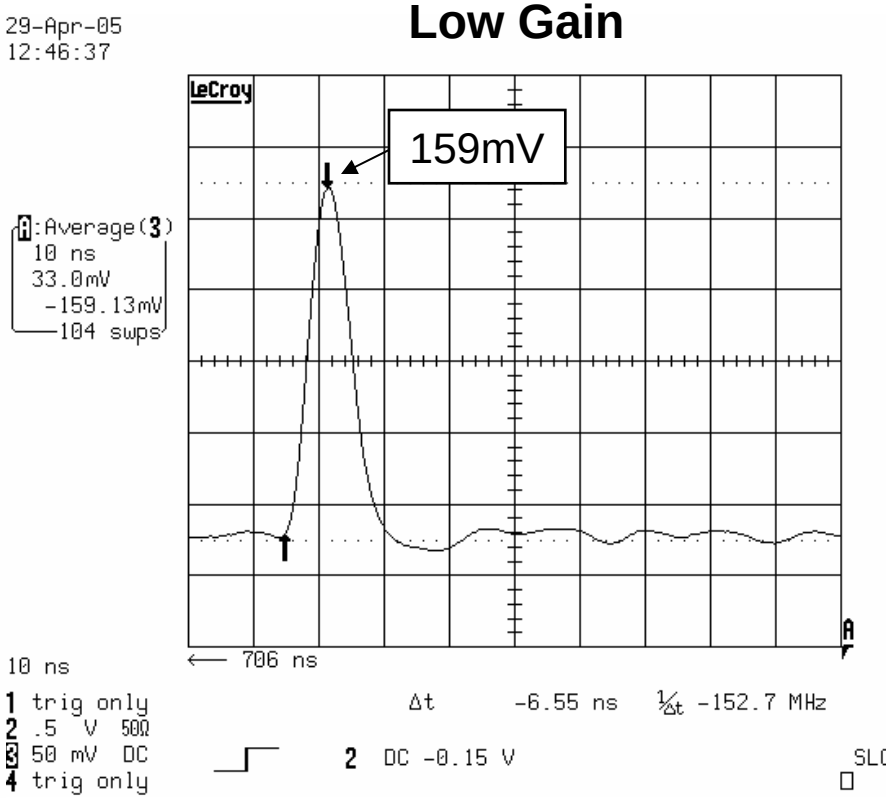


Test Pulse Response at BLR Output
TP Value set to 60 (11fC)

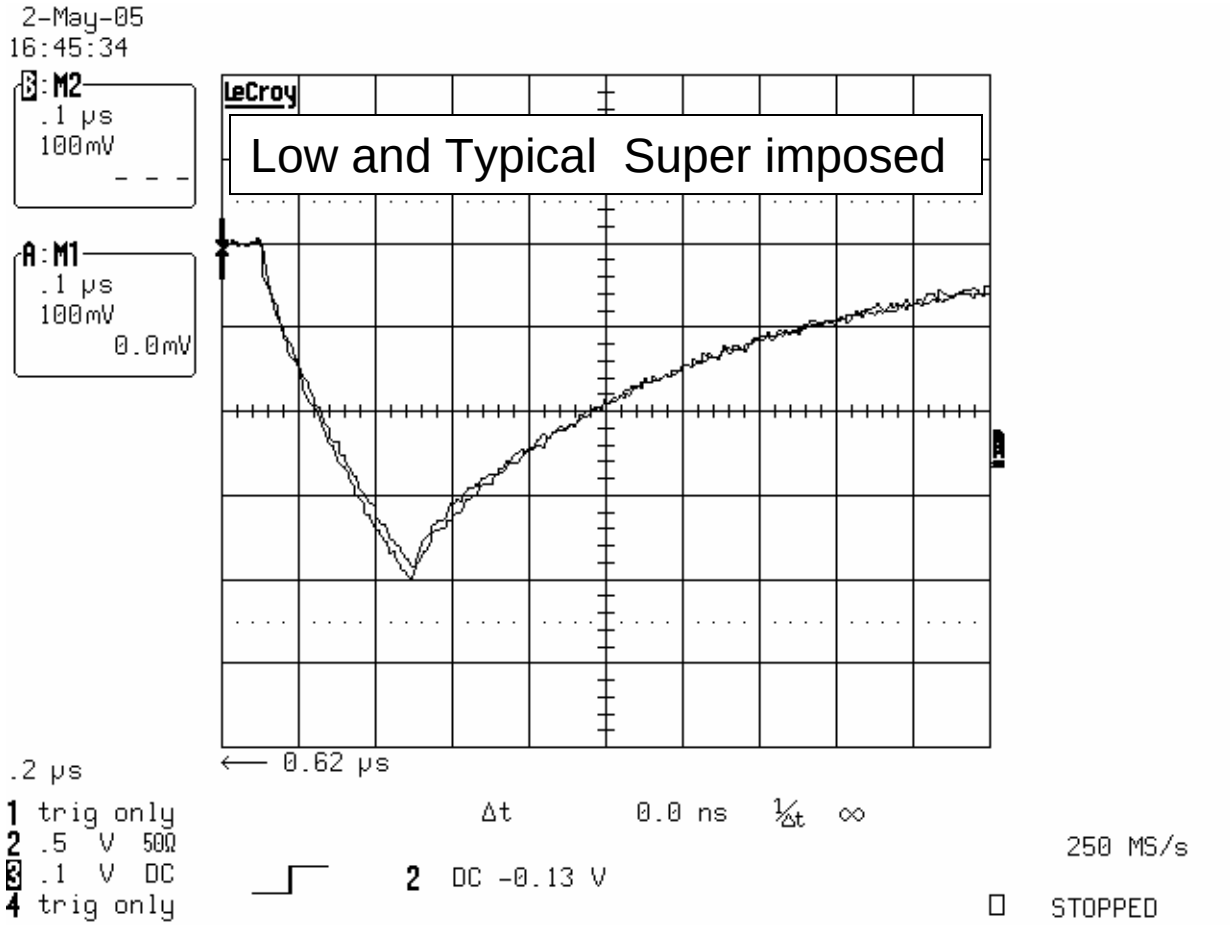
Typical



Low Gain



Test Pulse Input to ASDBLR from W0223 Triple Jumper Position #8 to Typical and Low Gain ASD



Preliminary Conclusions

1. Low Gain Channels are ~10% lower for External pulser and ~25% lower for the Internal pulser when measured at BLR monitor output.
2. Gain is constant down to ~1fC. Low Gain channels do not present risk that BLR will operate in a highly NL range for near threshold signals.
3. Using the same DTMROC to compare measurements of the whole signal processing chain indicate only a small gain difference between Low Gain and Typical ASDBLR boards. Examination of several chips has shown that the gain difference is relatively constant implying a batch difference.
4. Pulse shapes observed at the BLR output for low gain and typical chips are qualitatively the same from 2fC to 80fC of injected charge.
5. The maximum test pulse range is only about 12fC. Setting the DTMROC BLR bias resistor to a smaller value would increase this range.
6. Low Gain and Typical ASD's exhibit nearly identical test pulse shapes as observed at the Test pulse input to the ASDBLR.