Revision of test pulse lines on ASDBLR EC wheel boards

November 12, 2004

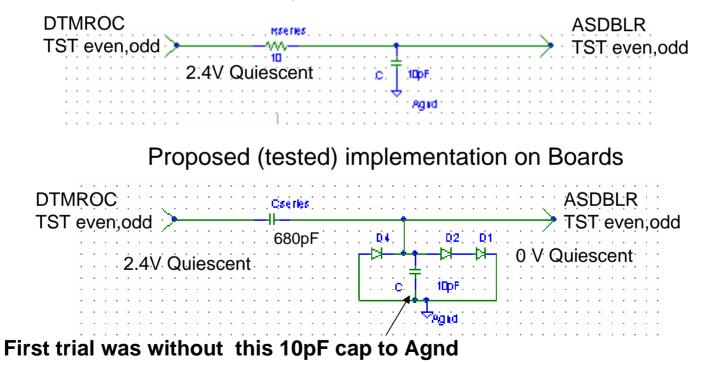
Mitch Newcomer

Input Protection on Test Pulse Lines

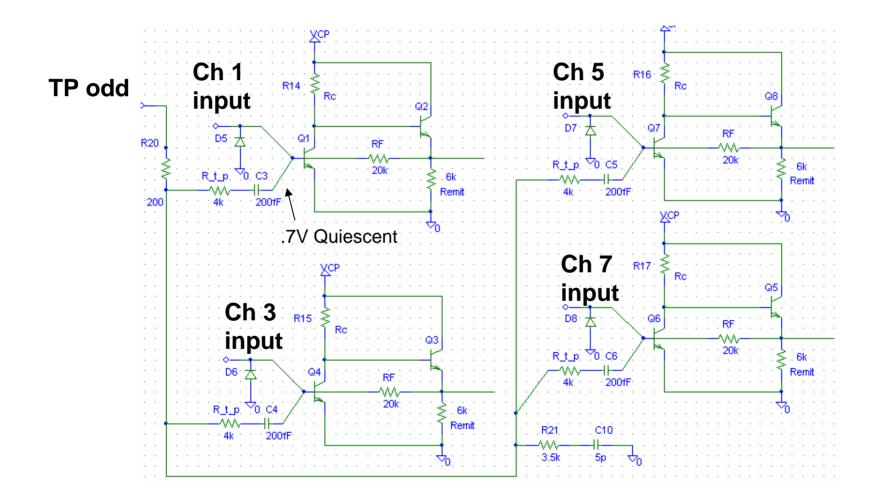
- The ASDBLR lacks input protection on the test pulse lines. End Cap Wheel boards that may be stored and tested separately from their DTMROC companion ASIC's potentially have a risk of being damaged without on board protection of the test pulse lines (TP even and odd).
- A proposed simple diode fix of all test pulse lines has been tested and appears to work. By using a capacitor to couple between the DTMROC and ASDBLR boards the potential across the Test Pulse capacitors on each channel of the ASDBLR can be maintained at a level close to ground. The proposed revision appears to work and may eliminate the functional loss of channels with test pulse failures. Results from B wheel board #5 are shown.

ASDBLR 'A' and 'B' wheel board Revised Test Pulse Inputs

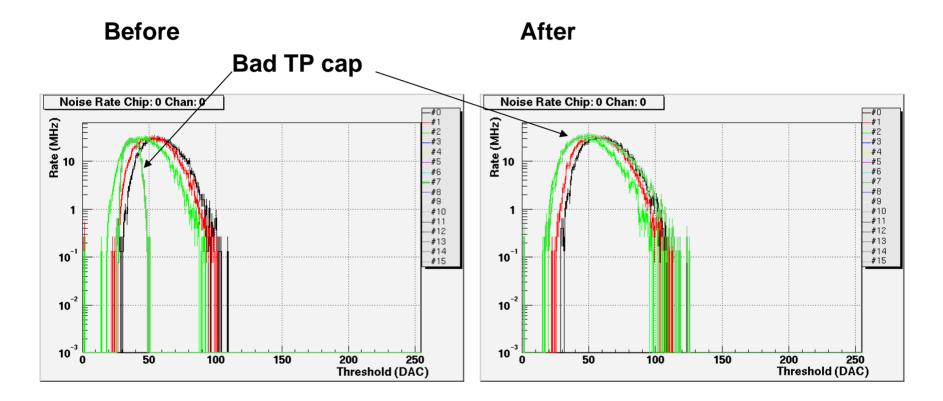
Present Implementation on Boards



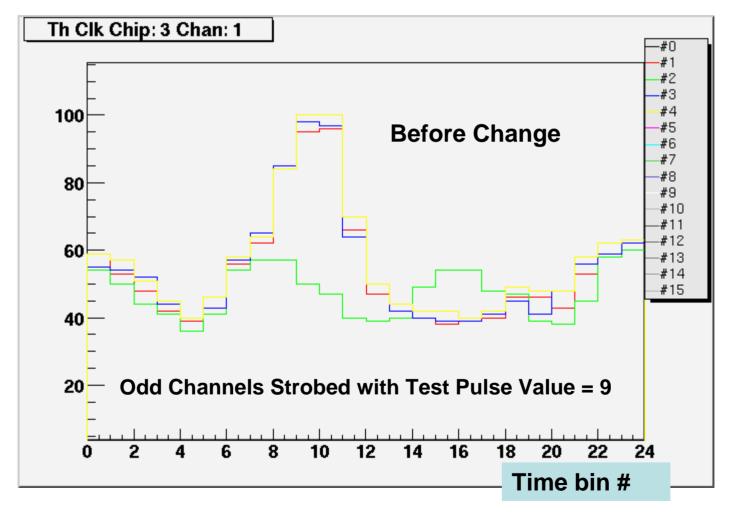
Approximate Schematic of ASDBLR Test Pulse Odd (on chip)



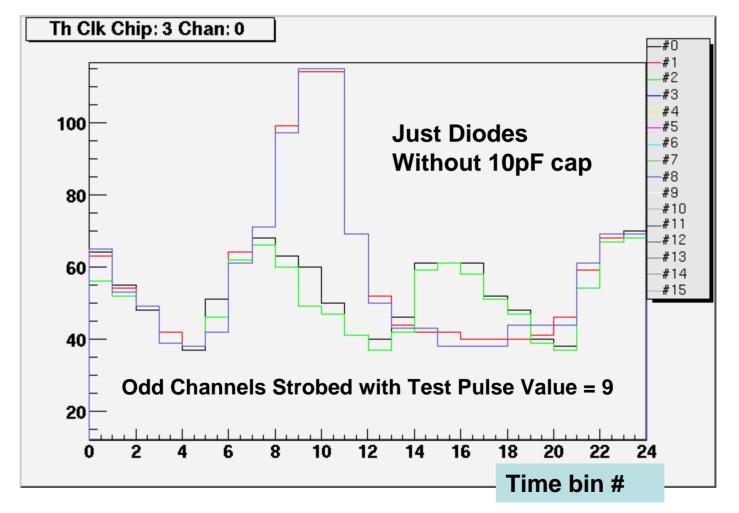
THRESHOLD Ramp Rate vs Threshold



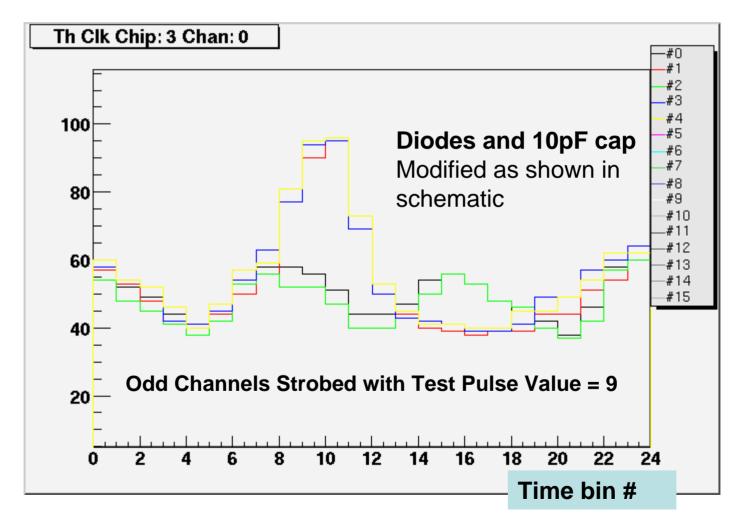
Test Pulse Scan 50% DAC values by Clock Bin (Normal working Channels)



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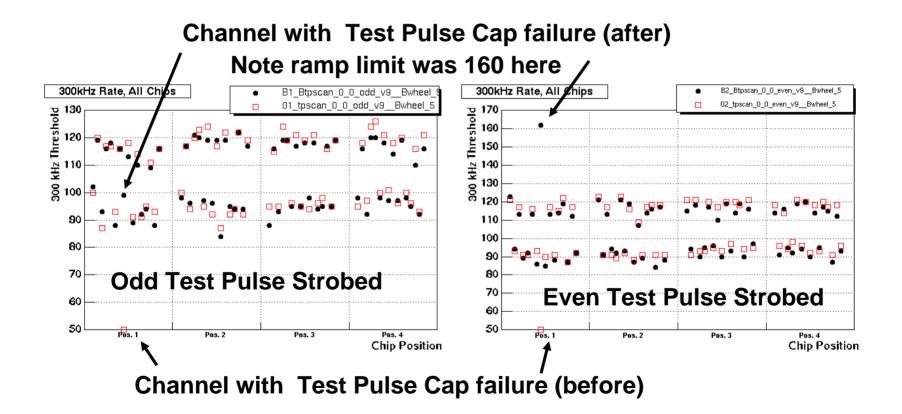


Test Pulse Scan 50% eff DAC Values by Clock Bin (Normal working Channels)



Odd/Even TP Before After with 10pF caps on TP even/odd

BEFORE Change • After adding Diodes and coupling cap

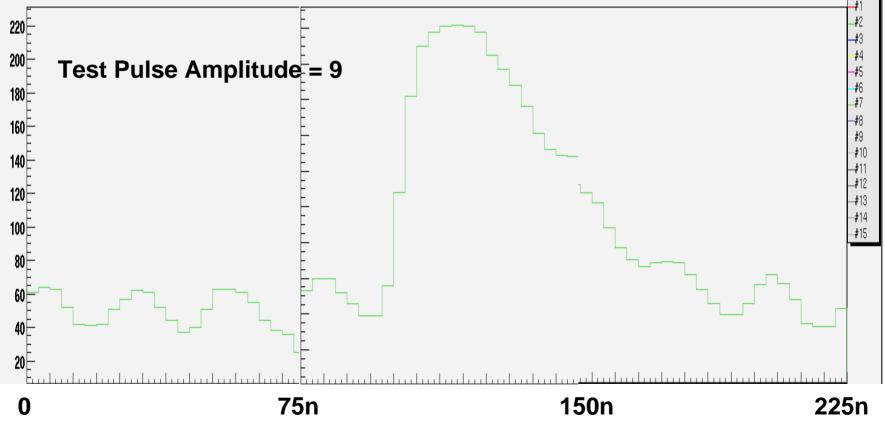


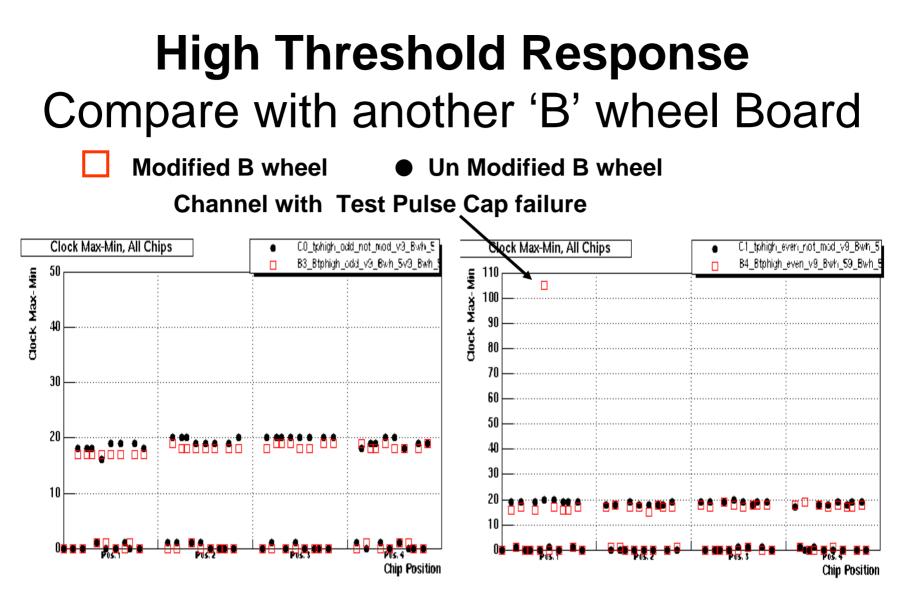
(All locations on B wheel End cap board #5 revised)

Response of Shorted TP cap Channel to Test Pulse on Modified Board

50% Threshold point by time bin for three 75ns windows

Soft Ware Channel #7 Rod Readout chip # 8





Test Pulse Amplitude Value = 60