Signal Quality Study with Triple Jumper Board and EC board to PP Cable

December 2, 2004

Mitch Newcomer

Setup

- MiniRod
- TTC99
- Original EC wheel PP (Using ROD 1 input only)
- Short cables to TTC (not studied)
- Cern Issue cable with BOC (Length = 9m)
- Pre Production Triple Jumper Board W0112

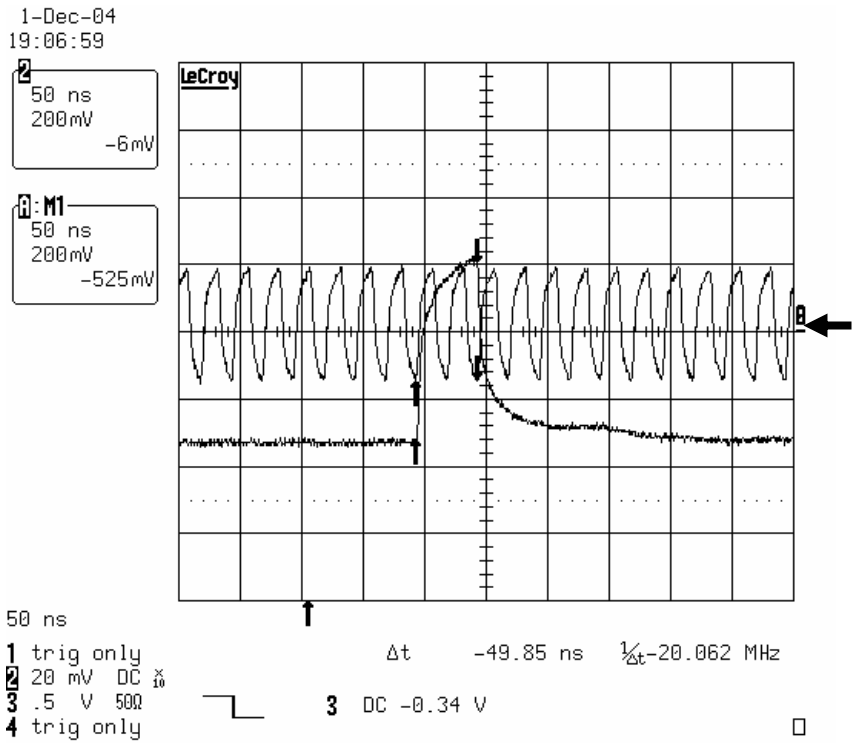
Purpose --

Examine of the effect of pre-comp on BX and CMDIN and effects of Differential Offset, Common Mode voltage and Compensation on CMDOUT.

Signals

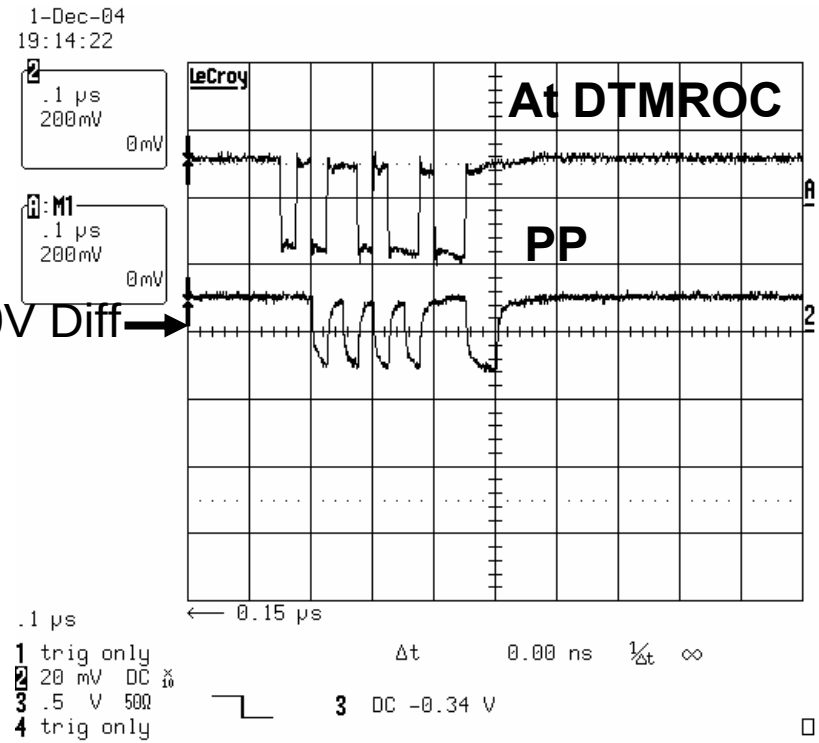
Differential measurements

BX and CMDIN at PP



0V Diff

Data Out



TTC99 Timing Scan

(Program provided by Mike Hance)

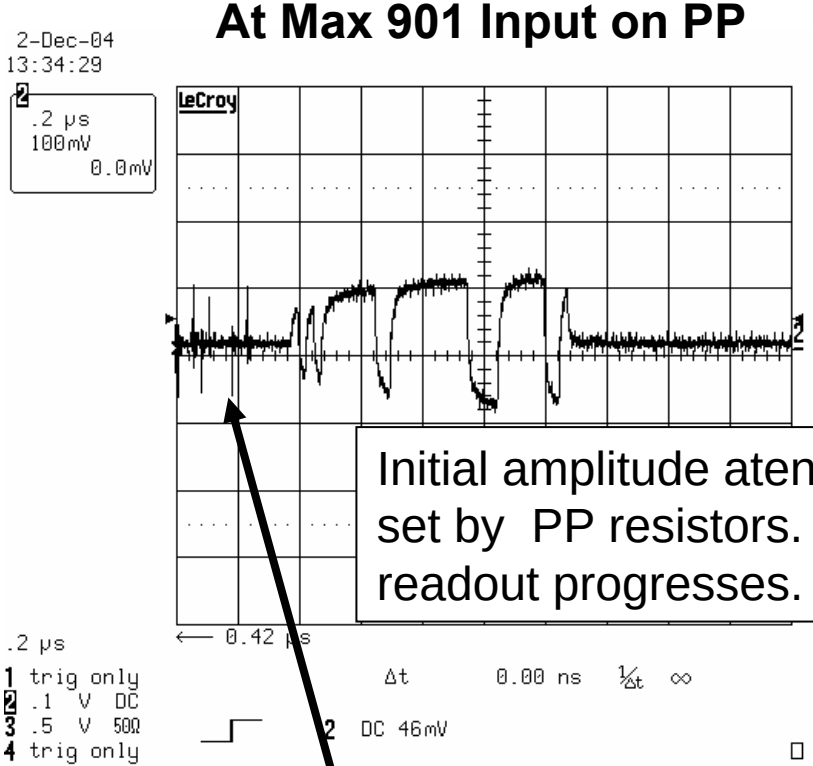
- TRIPLE W0112
  Total chips per delay with 100% success rate

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	12	12	7	-	-	7	5	3	3	4	7	9	12
2	12	12	12	8	-	-	4	2	3	4	7	9	12
4	12	12	12	12	8	-	-	2	3	4	7	9	12
6	12	12	12	12	11	6	-	-	3	4	7	9	12
8	12	12	12	12	11	8	3	-	-	5	7	9	12
10	12	12	12	12	11	8	6	1	-	-	7	9	12
12	12	12	12	12	11	8	6	2	2	-	-	9	12
14	12	12	12	12	11	8	5	2	3	1	-	-	11
16	1	12	12	12	11	8	5	3	3	4	5	-	-
18	-	2	12	12	11	8	6	2	3	4	7	8	-
20	-	-	-	12	11	9	6	3	3	4	7	9	7
22	12	-	-	-	11	9	6	2	3	4	7	9	12
24	12	12	-	-	-	9	5	3	3	4	7	9	12

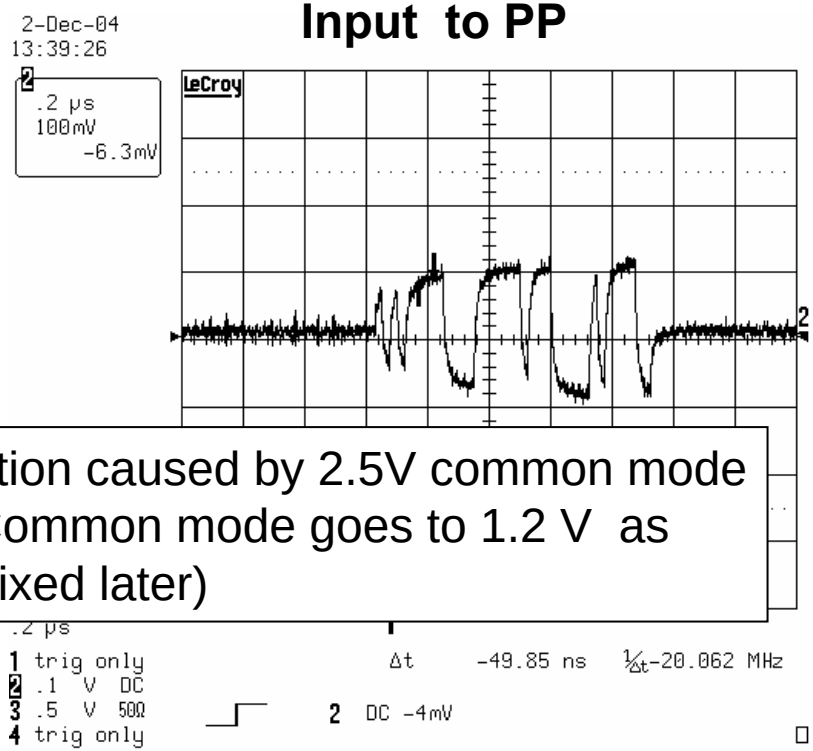
CMD OUT

Differential measurements

At Max 901 Input on PP



Input to PP

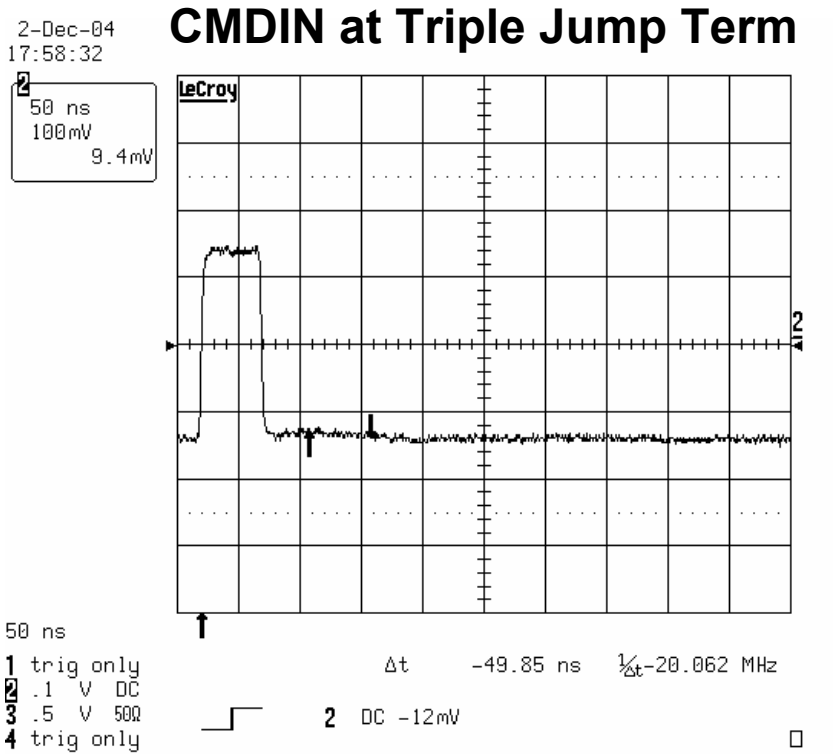


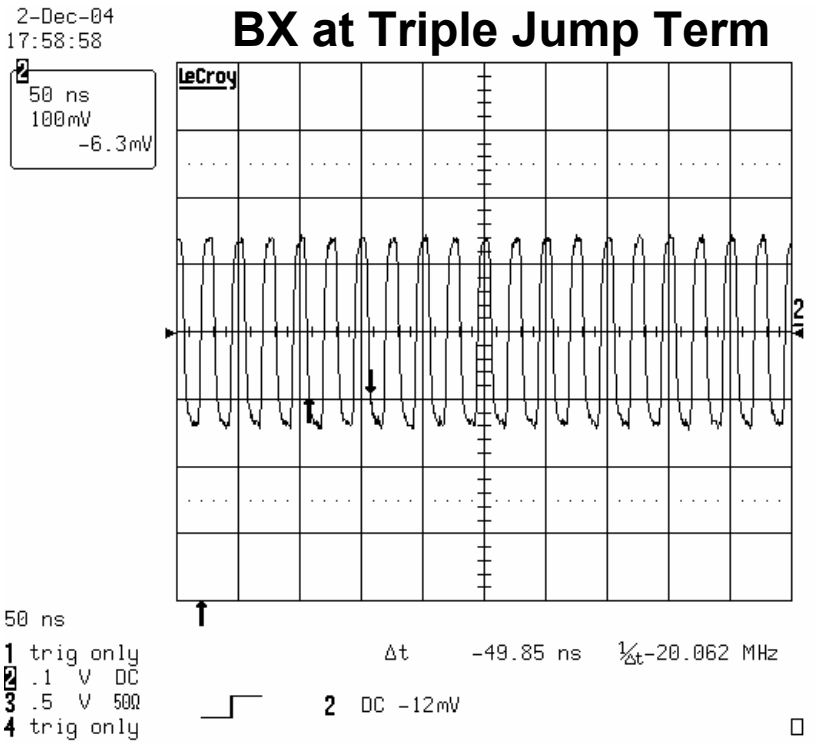
Initial amplitude atenuation caused by 2.5V common mode set by PP resistors. Common mode goes to 1.2 V as readout progresses. (fixed later)

Significant Pickup on PP at receiver input. Pickup evident from Resistive summing network. Will be eliminated on future PP's.

Add Pre Compensation

56Ω -1.5uH - 56Ω

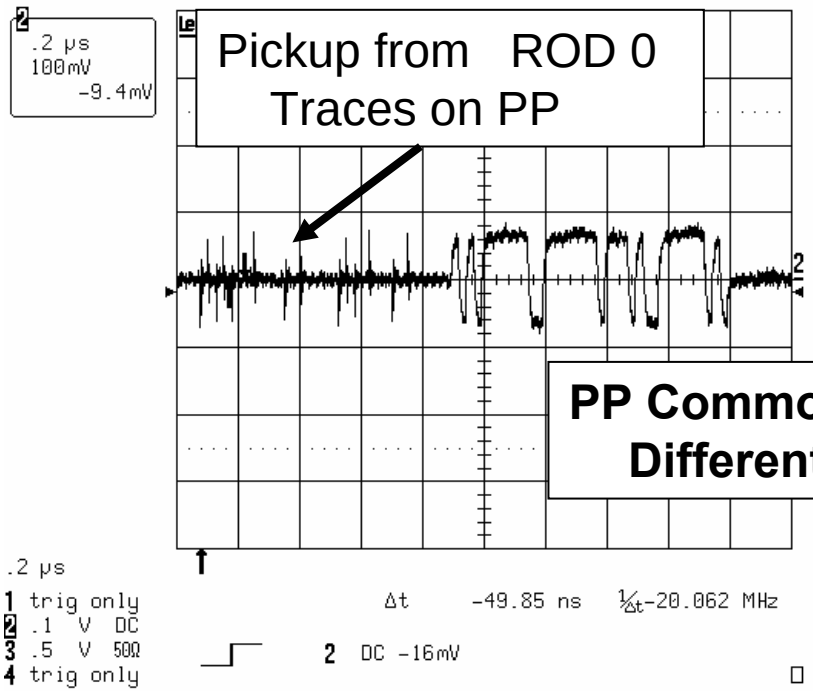




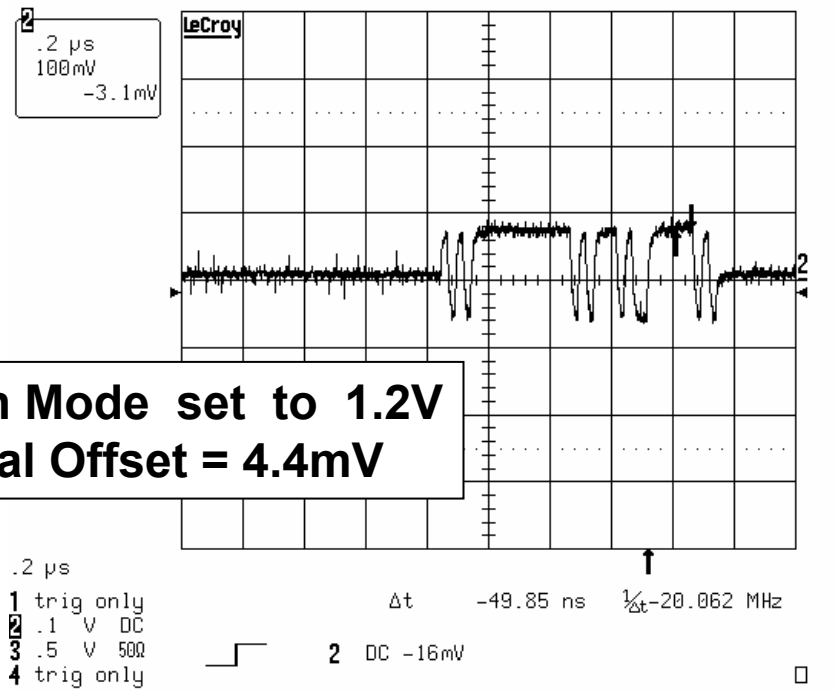
CMDOUT Compensation at PP

100Ω at input to MAX901 || with 56Ω - 1.5uh - 56Ω on cable

At Max 901 (comparator)
Input on PP



Input to PP at Cable Connector



PP Common Mode set to 1.2V
Differential Offset = 4.4mV

Timing Scan
→ CMD OUT Pickup Noise evident

T R I P L E 4.1mV diff threshold

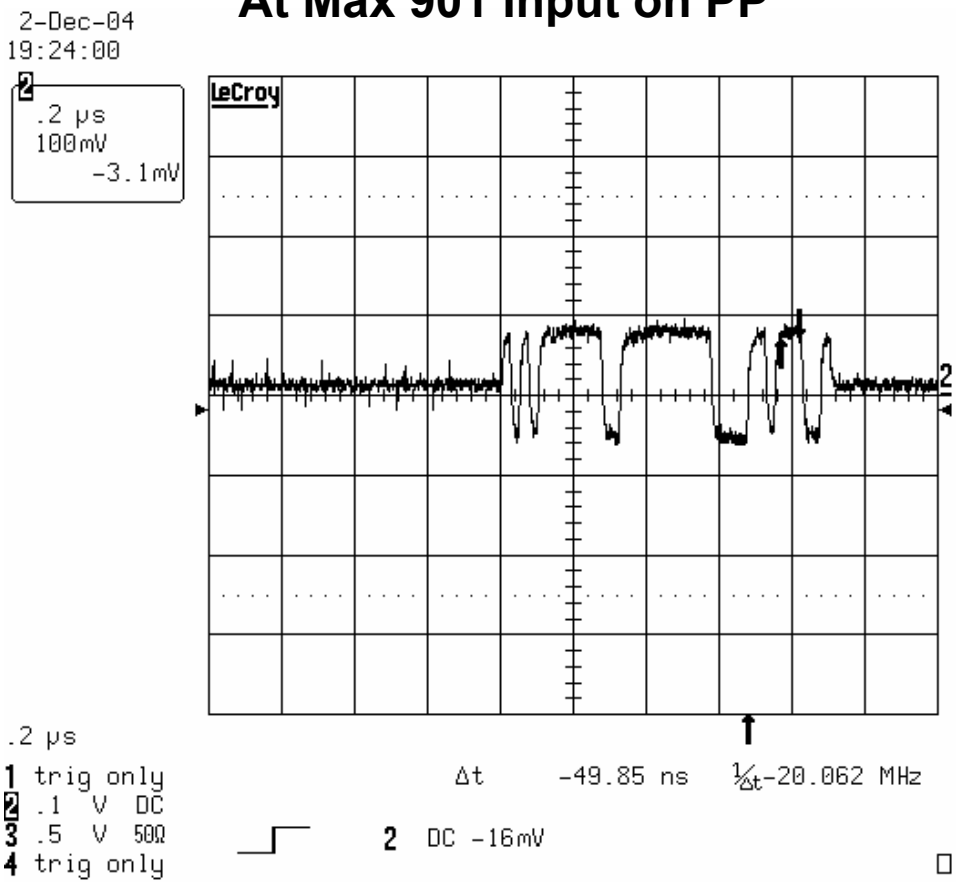
Total chips per delay with 100% success rate

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	12	12	8	7	12	12	12	12	11	11	10	11	12
2	12	12	12	5	3	12	12	11	11	11	10	11	12
4	12	12	12	12	5	3	12	12	11	11	10	11	12
6	12	3	-	-	-	4	3	12	11	11	10	11	12
8	-	-	-	-	-	-	-	-	-	-	-	-	-
10	-	-	-	-	-	-	-	-	-	-	-	-	-
12	12	-	-	-	-	-	1	-	7	4	10	11	4
14	12	12	12	12	12	12	12	12	11	4	1	11	12
16	12	12	12	12	12	12	12	12	11	11	5	2	12
18	12	12	12	12	12	12	12	12	11	11	10	6	3
20	-	12	12	12	12	12	12	12	11	11	10	11	6
22	12	-	12	12	12	12	12	12	11	11	10	11	12
24	12	12	-	12	12	12	12	12	11	10	10	11	12

Remove PP connection to Rod 0

100 ohms at input to MAX901
56Ω - 1.5uh - 56Ω on cable

At Max 901 Input on PP



Two sets of differential traces, CMDOUT from ROD 0 and 1, meet at the input to MAX901 comparator. The traces to ROD 0 are cut near the input to the MAX901 and the pickup is decreased.

Timing Scan Rod 0 PP lines cut

Common Mode 1.2V Differential Offset 4.1mV

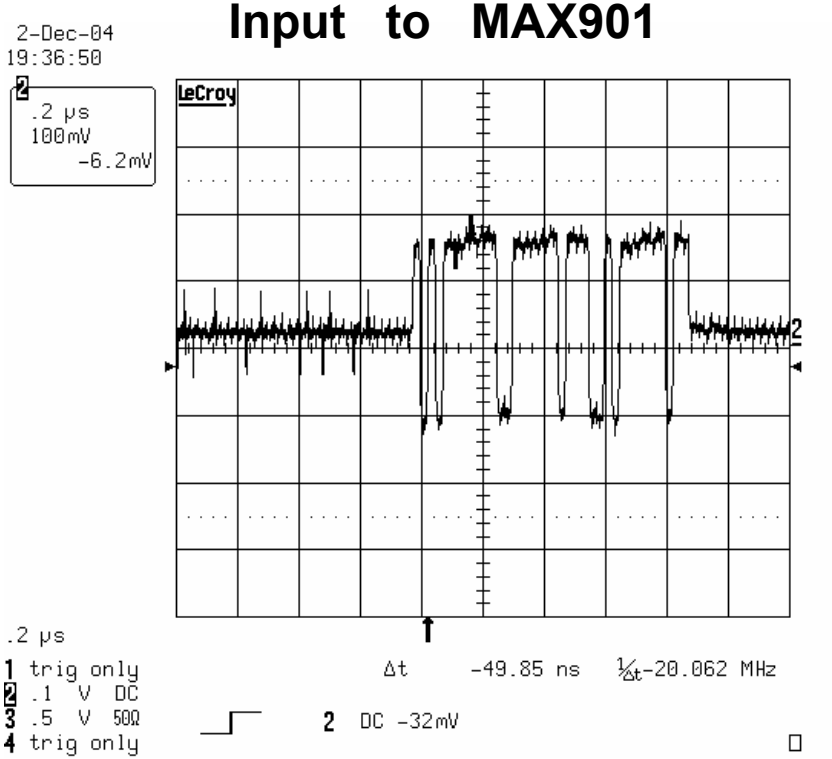
Total chips per delay with 100% success rate

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	12	12	9	4	12	12	12	12	11	10	10	11	12
2	12	12	12	7	3	12	12	12	11	10	10	11	11
4	12	12	12	12	5	2	12	12	11	10	10	11	11
6	12	12	12	12	12	5	2	12	11	10	10	11	11
8	2	-	-	-	-	-	3	2	11	10	10	11	11
10	12	-	-	-	-	-	-	-	-	10	10	11	11
12	12	12	12	10	12	12	12	12	7	3	10	11	11
14	12	12	12	12	12	12	12	12	11	4	1	11	11
16	12	12	12	12	12	12	12	12	11	11	7	2	11
18	12	12	12	12	12	12	12	12	11	10	10	8	3
20	-	12	12	12	12	9	12	12	11	10	10	11	7
22	12	-	12	12	12	12	12	12	11	10	11	11	12
24	12	12	-	12	12	12	12	12	11	10	10	11	11

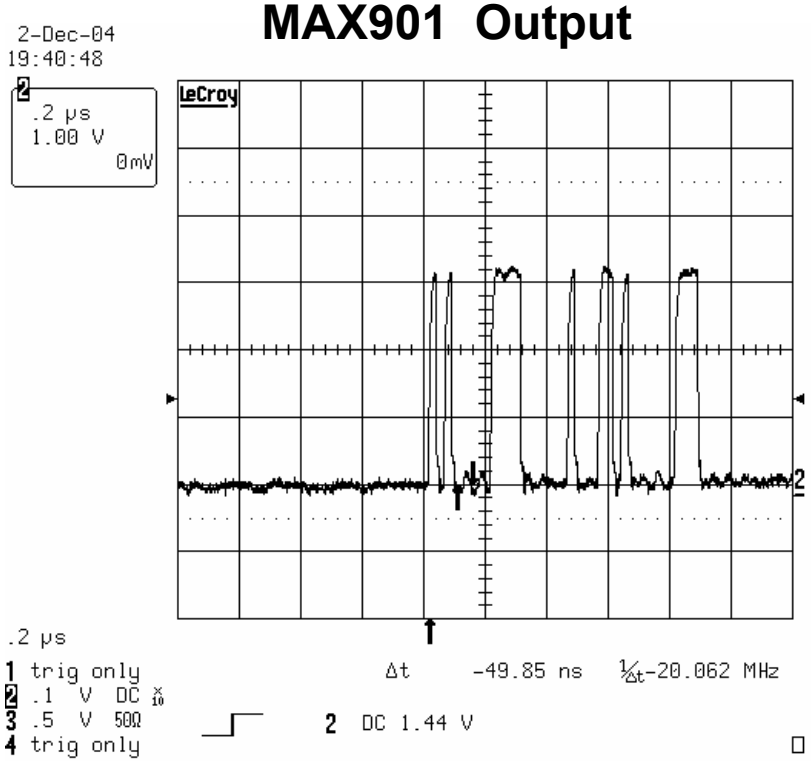
CMDOUT Revised Comp Increased Differential Offset

Common Mode 1.5V Differential offset 14mV
COMP revised to remove parallel 100 Ω

Input to MAX901



MAX901 Output



TTC Time Scan all Revisions

Vdd = 2.26V

TRIPLE 14mV final conf 4.7 down 9.1 up cm 1.5V

Total chips per delay with 100% success rate

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	10	12	11	2	12	12	12	12	12	11	10	11	11
2	10	12	12	9	1	12	12	12	12	11	10	11	11
4	10	12	12	12	9	1	12	12	12	11	10	11	11
6	10	12	12	12	12	9	1	12	12	11	10	11	11
8	10	12	12	12	12	12	10	1	12	11	10	11	11
10	10	12	12	12	12	12	12	11	1	11	10	11	11
12	10	12	12	12	12	12	12	12	10	1	10	11	11
14	10	12	12	12	12	12	12	12	12	8	-	11	11
16	10	12	12	12	12	12	12	12	12	11	7	1	11
18	10	12	12	12	12	12	12	12	12	11	10	10	1
20	-	12	12	12	12	12	12	12	12	11	10	11	9
22	10	-	12	12	12	12	12	12	12	11	10	11	11
24	10	12	-	12	12	12	12	12	12	11	10	11	11

TTC Timing Scan
Vdd = 2.5V

This is not necessarily as perfect as we might hope for, but it does help demonstrate the improvement that attention to signal quality has on final performance. More work is required to understand what we must put up with in the final system. All positions wired to Rod 1 (all except @#0 perform as expected

TRIPLE

Total chips per delay with 100% success rate

DX/BX	0	2	4	6	8	10	12	14	16	18	20	22	24
0	10	12	11	-	12	12	12	12	12	11	11	10	11
2	11	12	12	10	1	12	12	12	12	11	11	10	11
4	12	12	12	12	11	-	12	12	12	11	11	10	11
6	11	12	12	12	12	11	-	12	12	11	11	10	11
8	12	12	12	12	12	12	11	-	12	11	11	11	11
10	10	12	12	12	12	12	12	11	-	11	11	11	11
12	11	12	12	12	12	12	12	12	11	-	11	11	11
14	11	12	12	12	12	12	12	12	12	10	-	10	11
16	11	12	12	12	12	12	12	12	12	11	10	1	11
18	12	12	12	12	12	12	12	12	12	11	11	9	-
20	-	11	12	12	12	12	12	12	12	11	11	11	10
22	12	-	12	12	12	12	12	12	12	11	11	10	11
24	12	12	1	12	12	12	12	12	12	11	11	10	11

Conclusions

- **Control Signal quality impact on RO is significant.**
- **Some kind of cable compensation will be helpful.**
- **Some attention needs to be paid to pickup on differential signal lines.**
- **CMD Out differential offset of ~ 10mV improves sturdiness of RO at least using TTC99, miniROD and old PP.**
- **A signal quality study using the final cable to verify component values being stuffed on the EC triple jumper boards is needed soon.**