NSSLYON 2000 ATLAS TRT Electronics

ASDBLR99 Functional Block Summary

 CEA developed two terminal structure with Buried N+ shield

Input Protection – 380µm single stripe NPN
Collector → Input
Base+Emitter → Grounded

ODD AND EVEN TEST PULSE -

Compatible with DTMROC (Xe integral out)

Preamp — Pseudo Differential Dual Input Cascoded Common Emitter Gain ~ 1.5mV/fC t_p =1.5n Range 100KeV (1pC) SE input impedance 230 Ω @<10MHz 120 Ω @<50MHz Preamp Supply Filter on each channel

Shaping and Tail Cancellation –

Three Differential Stages

SE→Differential buffer - Gain 2
Selectable ION tail Canc. - Xe 70% or Ar-CF4
Programmable shaping adjustment
Operational to 60KeV(600fC)
Limiter Stage - canc. Preamp Tail
Soft Limit at > 10KeV (100fC)
Output Gain ~ 250mV/KeV (25mV/fC)
t₀ = 5n



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Functional Blocks

Baseline Restorer –

8pF Coupling caps followed by diode bridge with output sense current steering

Gain ~.80 for at threshold signals

Track Discriminator –

Threshold range: -200eV to 1.2KeV Amplifier Stage with shaping final t_p = 7.5n Fast Comparator with tuned Hysteresis Minimum output width 5-6ns 4 ns delay stage (aligns ternary outputs)

TR Discriminator –

Functional Threshold range: 1KeV - 12KeVAmplifier Stage with shaping final t_p = 10ns Fast Comparator with tuned Hysteresis

Ternary Driver –

Diff. Current Sum of Discriminator Outputs Programmable steps 0 – 2mA

Disc STATE		TERNARY Outputs	
Track	TR	Tern+	Tern-
OFF	OFF	$400\mu\mathbf{A}$	$0\mu\mathbf{A}$
ON	OFF	200 μ A	200 μ A
ON	ON	$0\mu\mathbf{A}$	400 μ A

ASIC SUBMITTED TO TEMIC 8/13/99

DIE SIZE 3.2X3.6MM 8 CHANNELS ~5500 COMPONENTS

Power 36mW/CH (WITH DRIVERS) +/-3V

