ASDBLR 99

Improvements / Objectives beyond ASDBLR 98

- First full implementation in DMILL
- Utilize only DMILL supported devices
- Eliminate Oscillation
  - Add differential stage with 2X gain at preamp output
  - Split capacitors used in tail cancellation differentiation
  - Use shielded pads at input and output
  - Extensive use of contacts to global substrate
- Stabilize back edge of Ternary output
- Add Odd/Even Test Pulse Input
- Maintain Full dynamic range within Power Budget

Submitted Aug 9,1999 Received Jan 2000

NSS LYON 2000 ATLAS TRT Electronics

Good News

- **All Blocks fully functional.**
  88% (7% 1 bad ch, 6% all chan bad) Functional Yield.
- **Meas. Threshold within a few % of SPICE Calculations.**
- **Measured Power Consumption 34.5mW/ch. Agrees with SPICE.**
- **No Oscillation observed at Monitor points.**
- **Channel to Channel Crosstalk below 0.5% on TB3 board.**
- **Pickup on test pulse lines NOT Observed to tested level of 30:1.**
- **Test Pulse Highly Uniform. Results MATCH manual injector.**
- **Back Edge of Ternary output stable through transition from "one" to "two" level output.**
- **Little parametric change after 10^{14} N/cm^2 or 10^{14} P/cm^2.**
- **Preliminary Noise measurements, 2200e ENC with 10pF input cap.**

Bad News

- **Parametric Yield 35 – 45% 100 chips on several wafers.**

Other News

- **Shaping time ~6ns, not 7.5ns as expected.**
- **Low threshold tests in chip test socket noisier than on board.**
- **Input Protection fails at 1500V with 560pF (180uM emitter).**