IMPLEMENTATION of the ASDBLR Straw Tube Readout ASIC in DMILL Technology

N. Dressnandt, Member IEEE, N. Lam, F.M. Newcomer, Member IEEE, R. Van Berg, Member IEEE, and H.H. Williams*

Abstract

The ASDBLR ASIC provides eight channels of low noise, low power, high rate on-detector readout suitable for the ATLAS Transition Radiation Tracker (TRT) at the LHC. The TRT's unprecedented wire chamber readout requirements of a maximum hit rate per wire of 20 MHz and double pulse resolution of ~25 ns with position resolution of better than 150 μm in a high radiation environment have been addressed in the design of the ASDBLR. A carefully tuned ion tail cancellation stage followed by an output sensing baseline restorer implemented in differential structures provides robust signal processing combination compatible with the realities of ASIC design. Two comparators track the output of the signal processing stage to provide tracking information from charged particles and evidence of higher energy Transition Radiation (TR) photons; their outputs are summed as current steps to form a differential ternary output. The ten year total dose requirement for neutrons of 10^{14} n/cm^2 and 1.5 MRad of ionizing radiation led to the implementation of this design in the radiation hardened DMILL process.

I. INTRODUCTION

The ATLAS TRT, will occupy a 20 m^3 volume inside the super-conducting solenoid magnet with 425,000 4 mm diameter straw tubes 40 to 80 cm in length filled with a 70%Xe+20%CF_4+10%CO_2 gas mixture and operating at a gain of 2X10^4 [1]. This detector subsystem will be used to identify and reconstruct the path of energetic ionizing particle tracks and to identify high energy electrons.

The electron drift velocity in the gas is ~90 μm/ns. An electronics goal of 1 ns timing resolution ensures that the inherent response of the electronics will not interfere with the position resolution goal of ~150 μm. A wide dynamic range of signals, up to 100 times threshold, high occupancy and the 25 ns beam crossing rate make this a challenging goal. Gas atoms ionized in the avalanche process near the wire induce a signal current as they drift away toward the cathode; this current, known as the *ion* tail is primarily determined by the type of gas and wire diameter. It is traditionally removed by building a mirror image impulse response into the signal processing electronics so that the ion tail and mirror signal cancel after the initial avalanche signal. In a cancellation process like this only a small fraction of the total avalanche signal is available, in our case about 20% of the 2X10^4 gain or 0.6 fC per primary drift electron in the gas. Since our objective is to detect the earliest clusters, the electronics must add as little noise as possible to the detected signal. After careful study and several design iterations, an electronics peaking time of 7 ns with a semi-gaussian shape after ion tail cancellation was targeted for this design. This allows integration of the avalanche signal from the first few clusters of drift electrons arriving at the wire.

TR photons are created in layers of polypropylene material placed between the straws. Xenon in the gas mixture allows efficient absorption of these photons whose energy is in the range of 7-8 KeV, well above the typical 2 KeV deposited by a minimum ionizing track in the straw. Extending the peaking time of the TR detection circuit to 10 ns allows integration of the direct and reflected signal from the far end of the unterminated straw to be summed. This reduces the variation in amplitude versus position of the avalanche along the straw [2,3].

Table I
Design Goals for the ATLAS TRT Front End Electronics

Peaking Time for Track Detection	7ns
Peaking time for TR photon detection	10ns
Double Pulse Resolution	25ns
Intrinsic Electronics Noise	<0.3fC RMS
Operational Track Disc. Threshold	2fC
Maximum Threshold for TR photons	120fC
10 year Neutron exposure	10^{14}/cm^2
Total Dose (10 year) Ionizing Radiation	1.5Mrad

The ASDBLR ASIC has been designed to provide the high rate functionality described above. A summary of the goals that guided the design are given in Table I.

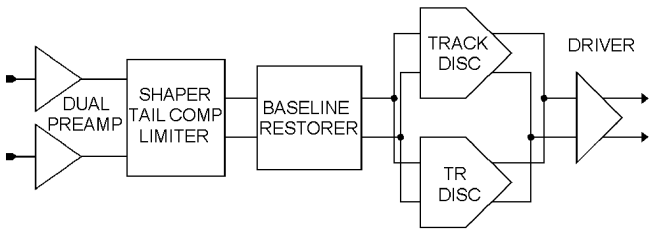

Fig. 1. Channel blocks of the eight channel ASDBLR.

II. THE ASDBLR CHANNEL BLOCKS

The basic channel blocks are shown in Fig 1. Intrinsic noise referred to in the text that follows is measured in the Track

• Manuscript submitted November 3, 2000. Authors are from The University of Pennsylvania, 209 S. 33rd St. Philadelphia Pa. 19104. Contact person: Mitch Newcomer, 215-898-4456, *email:* mitch@hep.upenn.edu

Disc Block where detection of the avalanche signal from a track provides the time marker to determine the closest point of approach for a track to the wire. The signal to noise at this point in the circuit ultimately determines the instrumental uncertainty in track position measurement.

The inputs to the Dual Preamp are bonded out and are available at the input of the packaged ASIC although only one input is attached to the straw wire anode. Fast response breakdown protection is achieved using the normally reverse biased collector-base junction of single stripe NPN transistors. For the input attached to the wire a total of 380 μm of emitter length provides 0.5 mJ breakdown protection when a series 24 Ohm resistor is used between the input and the wire. This external resistor contributes 8% of the total intrinsic noise at the Track comparator input.

The Dual Preamp has a gain of 1.5 mV/fC, dynamic range of more than 600 fC and peaking time of 1.5 ns. Two identical preamps provide a balanced DC bias into the following differential stage and serve to help reject common mode noise both on and off chip although they do not present a truly differential signal to the Shaper stage input. Consideration of intrinsic noise plays an important role in sizing the input transistor. Base resistance and base current in the input transistor are primary sources of noise in our circuit. Base resistance is inversely dependent on the total emitter length of the transistor and base current is determined by the total current divided by the gain, or beta, of the transistor. In a high radiation environment beta loss becomes significant below a value specific to the technology. Our measurements on irradiated transistors show that below 5μA/μm of emitter length beta loss increases rapidly. See Section *IV, B.* To allow for variation in the radiation sensitivity of the process we chose a minimum current density of 7 μA/μm resulting in an emitter length of 80μm for each input transistor. After ten years of operation in the ATLAS TRT we expect the beta of the input transistors to be reduced from a typical initial value of 200 to 60 resulting in an increase in the intrinsic noise of about 20% at the Track comparator input. Scaling models from the manufacturer we estimate the base resistance of the input transistors to be 32 Ohms. Noise analysis shows that with the expected capacitive load of 10pF at the input to the preamp this resistance will account for 12% to the total intrinsic noise.

Analog signal processing occurs in the three stage Shaper block that follows the Dual Preamp. The first stage has a gain of two and converts preamp input to a symmetric pulse suitable for differential processing. The next stage utilizes passive pole-zero networks to provide externally selectable Argon or Xenon dominated ion tail cancellation and is biased toward under compensation to ensure that process variations do not create overshoot in the output. The final shaping stage is used to cancel the short tail added by the preamplifier feedback network and limit the shaper output response to signals below 120 fC. Equivalent multi-pole shaping is achieved by adding a 1.5 ns R-C integration at each shaping stage. Counting the second dominant pole of the preamp, four poles (or integrations) in total combine, to yield a peaking time at the Shaper block output of about 5 ns. The gain at the Shaper block output is 25 mV/fC.

The Baseline Restorer, BLR, serves to eliminate process dependent DC offsets at the output of the shaper, reduce sensitivity to baseline shifts due to high rate and reduce sensitivity to imperfections in the ion tail cancellation network. Two series connected 8 pF capacitors couple the differential signal from the shaper into the BLR while removing the DC bias of the shaper stage. A bridge diode network shunts across the outputs of the two coupling capacitors creating a variable impedance and maintaining a baseline of zero Volts across the outputs. At baseline the bridge current is 25 μA/diode resulting in an impedance of 1000 Ohms between the outputs. Considering the 8 pF coupling capacitors, this makes a 4ns decay time constant. As signals of desired polarity are processed, the current in the bridge is decreased, increasing the time constant and limiting the discharge of the coupling capacitors. When the shaper signal returns to baseline, lost charge in the coupling capacitors results in overshoot or a change in polarity of the outputs. This causes an increase in bridge current, lowering its shunt impedance and shortening the overshoot with a discharge time constant of as little as 1.5ns.

The attenuation of the signal in the BLR depends on the shaper peaking time (5 ns) and magnitude of the input due to the non-linear impedance of the BLR diode bridge. For signals near threshold, a longer peaking time would result in an undesired partial differentiation of the input pulse due to the short time constant of the BLR for small input signals. A 2 f C signal is attenuated by 20% while a 20 fC signal, typical of a track deposition, is attenuated by 5%. The measured response at the Shaper output and BLR outputs are shown in Fig. 2.

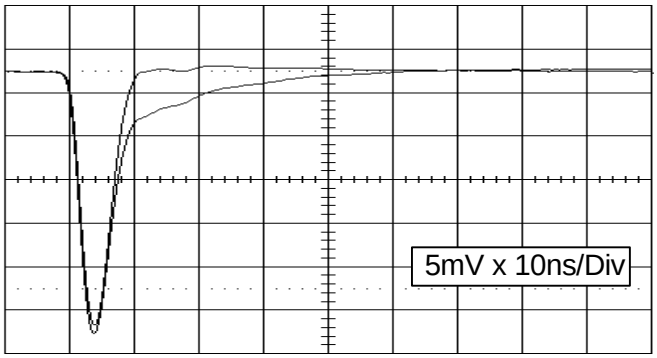

Fig. 2. Measured (test socket) response of the ASDBLR99 in a test socket to a 30 fC charge, shaped to duplicate the TRT straw signal. Traces show the output of the Shaper and BLR Blocks measured at the monitor outputs. The gentle return to baseline of the Shaper output helps keep the BLR output from having an enhanced overshoot.

The Track and TR discriminators attach in parallel to the BLR output. The track discriminator adds an explicit 2 ns R-C integration to meet the target peaking time of 7 ns. A single threshold for all eight channels is provided with a programmable range (in terms of effective input pulse) of –1 fC to +12 fC. This insures the ability to calibrate the threshold zero.

The TR Discriminator is nearly identical to the Track Discriminator except that an attenuator reduces the magnitude of the BLR signal by a factor of 10 and the peaking time is increased to 10ns by two, 2.5 ns R-C integrations to achieve the target value for the TR Discriminator. The chipwide threshold for the TR discriminator can be set between an effective input value of –10 fC to +120 fC.

To minimize connections between the ASDBLR and the time digitizing chip (DTMROC) a two level, ternary output is employed to register the presence of signals over the Track and TR discriminator thresholds. Since we intend to use the TR threshold to select events with a much larger deposition than tracks we take advantage of the fact that the Track comparator will always be triggered if the TR comparator is triggered and form an equal current sum of the TR and Track outputs. If either output current is switched independently, a low Ternary level is detected by the DTMROC and interpreted as indication of a triggered Track Discriminator. Thus a misinterpretation can occur if the Track and TR comparator outputs are not coincident in time. A 4 ns delay is added to the Track comparator output prior to ternary encoding to compensate for the early arrival of its output due to its lower effective threshold and shorter shaping time. Fig. 3 shows the ternary output for a signal just above the TR threshold. A hysteresis network ensures that the minimum output width is 5 ns for both comparators.

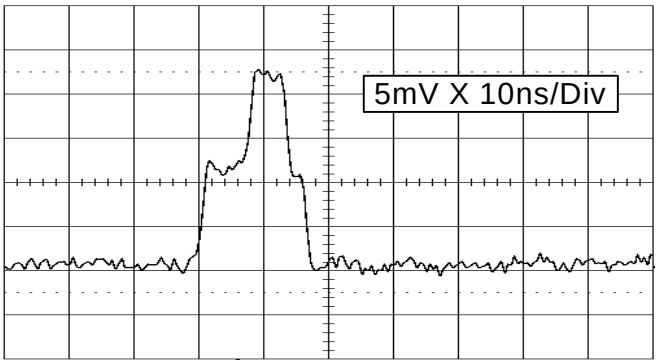

Fig. 3. Ternary output of the ASDBLR99. An input pulse of 30 fC triggers both the Track and TR discriminator outputs. The TR threshold was set to be 50% efficient for 30 fC signals. As the plot shows, the minimum output width is more than 5 ns for signals just over threshold. The trailing edge shows a distinct break where the TR output returns to baseline prior to the Track Discriminator output.

III. Previous Versions

The ASDBLR is currently in its third generation. The original circuit was implemented in an analog bipolar, bulk process and qualified for use on the ATLAS TRT in 1997 [4]. Subsequent versions have been fabricated in DMILL, a radiation hardened analog BICMOS process first developed by a consortium of CEA, Thompson-TCS and IN2P3 and recently commercialized by TEMIC [5]. As a first test of the suitability of the this process for implementation of the ASDBLR a six channel prototype containing all the major blocks was submitted to TEMIC as part of a multi-project fabrication.

Measurements of this prototype showed full functionality of each circuit block and an equivalent input noise charge of 0.32 fC RMS. The tail cancellation network was tested using a pulse injector that mimics the straw tube signal. As shown in Fig. 4 the output of the shaper returns to within 10% of baseline in 35 ns without overshoot in spite of the fact that the process resistors were 25% higher than nominal. One source of concern was oscillation observed at the analog monitor, a diagnostic output intended to verify the signal shape presented to the discriminator. A hookup dependent damped harmonic ring with a characteristic frequency of ~150 MHz was superimposed on the expected output signal as shown in the lower trace in Fig. 4. The severity of the ring was dependent on which of the pseudo differential inputs was used and the balance of stray capacitance between them. The cause was determined to be feedback coupled through the SOI insulator to the underlying substrate. Stray capacitance to the substrate below the insulating layer was not accounted for in the analog simulation models provided for the process devices. After revising the SPICE models to include the calculated capacitance to the underlying or *back* substrate the layout extracted netlist indicated the observed dependence of the harmonic response on input hookup conditions.

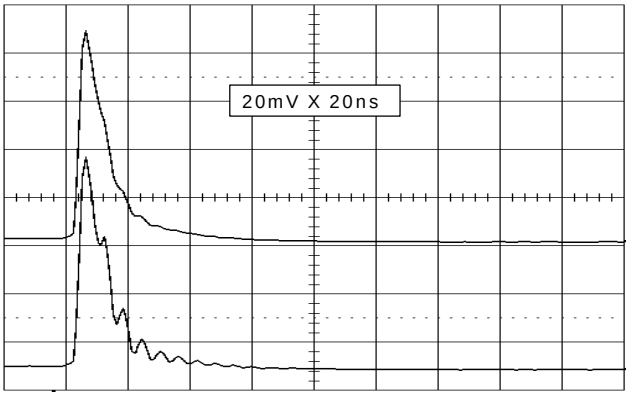

Fig. 4. Response at shaper monitor output of the first DMILL prototype ASDBLR indicated a potential for harmonic ring when the capacitance at the inputs was not balanced as in the lower of the two traces where the capacitance on one input was 22 pF and 7 pF on the other. In the upper trace the conditions are the same except that the inputs both have 22 pf capacitance.

IV. ASDBLR99 First Full Engineering Prototype

The ASDBLR99, an eight channel prototype that utilizes only foundry provided devices was submitted for a fabrication run with its partner ASIC the DTMROC that supplies time measurement and readout control discussed in Ref. [6]. Four measures to eliminate the oscillation observed in the first prototype were included:

1) A differential stage added at the outputs of the dual preamp to symmeterize the signal.
2) Use of split capacitors, connected in parallel with inverted polarities in the tail cancellation network to insure differential coupling to the back substrate.

3) Use of shielded bonding pads, developed by CEA, at inputs and outputs to limit input coupling to the back substrate through the bonding pads.
4) Addition of a filter network in the power supply input for each preamp to reduce the chance that some ring was coming from pickup coupled through the power lines.

Measurements of the fabricated devices (Figs. 1, 2) show that the harmonic oscillation has been eliminated, and that the performance is nearly the same as SPICE simulations predict. The peaking time is about 15% faster than SPICE predictions, and absolute threshold matches to 5%.

A. ASDBLR99 Yield

Functional yield of the ASDBLR99 is approximately 85%, but parametric yield after channel to channel matching requirements are applied is only about 35%, less than half of that achieved for a design of similar complexity in a bulk process. Measurements have isolated the most significant source of threshold mismatch to the input stage of the Tracking Discriminator where two problems appear to be responsible for at least half of the parametric yield loss. A differential attenuator network on the output of the BLR is referenced to analog ground unnecessarily setting up a DC current in resistors that mismatch by ~1%. This results in an input offset uncertainty of several millivolts. In addition to this offset, the mismatch in the base-emitter voltage of the DMILL NPN transistors was expected to be less than one millivolt, but measurements of matched NPN transistors in process monitor sites have yielded mismatch values that are three times higher than expected, adding a second source of unexpected comparator offset of a few millivolts. These problems will be addressed in the next version of the ASIC by elimination of the unnecessary analog ground reference and by the use of four larger NPN transistors with bi-quad layout geometry.

B. Radiation Tests

The performance of two ASDBLR99 ASICS was virtually unchanged after exposure to 10^{14} n/cm^2 at a reactor facility, while the beta of NPN transistors (@5 μA/μm of emitter length) changed from an average value of 240 to 60 after exposure. Process resistors exposed in the same run changed by less than 1% . We have also measured the effect of exposure to protons at the CERN PS where a total of six ASDBLR99 ASICS were exposed to 10^{14} protons/cm^2 while under power. Measurements after radiation were consistent with zero change taking systematic uncertainties into account. Relative channel to channel threshold offsets remained quite similar to pre-exposure values. Table II summarizes the measured changes for implanted base resistors (1.6 KΩ/Square) and NPN transistors tested at a Vce of 1 V and current density of 5 μA/μm.

Table II
Summary of Radiation Results for DMILL devices
exposed to Neutrons and Protons

Devices	Pre Exposure	10^{14} P/cm^2 Powered	10^{14} N/cm^2 Unpowered
NPN Beta	338	72	58
Resistor Change		+7.5%	+0.75%

C. Test Beam Results with prototype TRT straw

Measurements of position resolution and efficiency versus rate were made at the CERN H8 test beam using CAMAC TDC's and compared to the performance of previous prototypes.

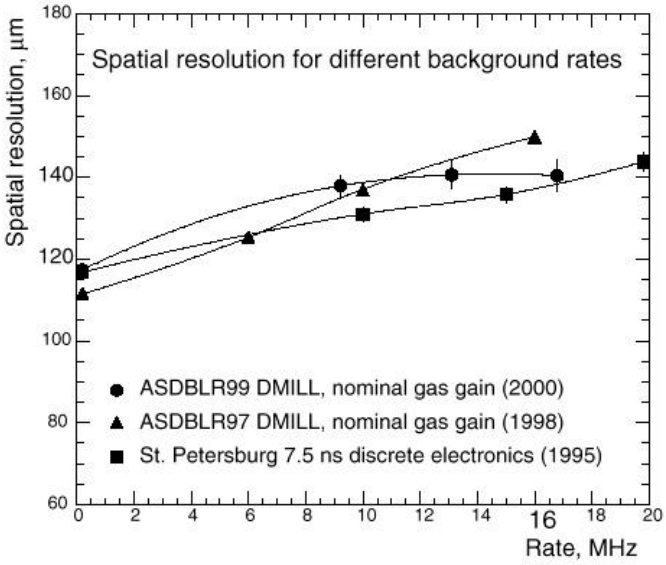

Fig. 5. Using track positions determined by a silicon strip telescope, measured position resolution for tracks as a function of triggering rate is shown for various prototype electronics. The ASDBLR99 matches well with a hand tuned discrete component prototype.

At 17 MHz background rates, the position resolution is about 130 μm and efficiency for detecting a track within 2.5 σ of the reconstructed position is 65%. In both cases the performance is better than the previous prototype and nearly matches that of a hand tuned prototype intended to set the standard for the best performance that can be expected.

D. High Density Prototype Readout

The complete readout chain was tested with a TRT sector prototype in the CERN H8 Test Beam. The sector prototype was instrumented with two 64 channel stacks that included eight ASDBLR99's and four DTMROC, digital time measuring and readout chips. Readout into a VME processor was performed by a Read Out Driver (ROD) prototype. With very little noise reduction effort, the system was made to operate at the design thresholds and position resolutions of as good as good as 135 um were achieved.

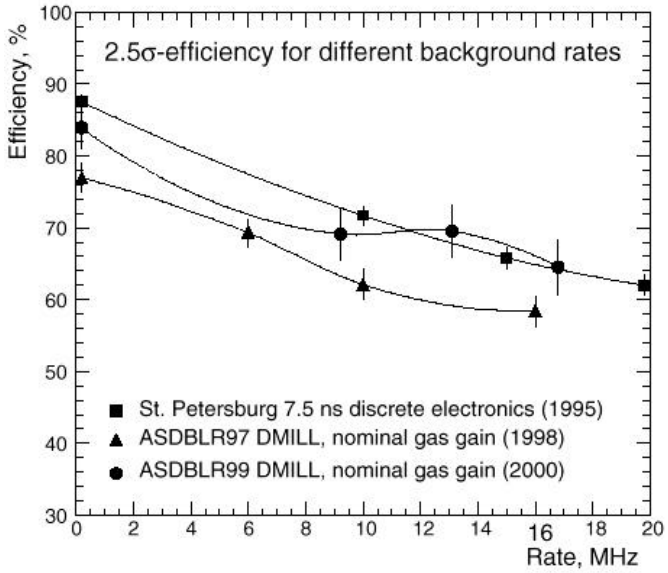

Fig. 6. Tracks with position determined by a silicon strip telescope are compared with position data determined by various prototype wire chamber readouts. Straw hits within 2.5 σ of the track position are considered to be efficient. The ASDBLR99 is shown to be as efficient as a hand-tuned channel built with discrete components.

V. Custom Test Structures

In order to overcome limitations of the foundry provided devices for our application, we have had several device test structures fabricated by TEMIC including two input protection devices and several versions of multi-stripe NPN transistors.

A. Multi-stripe NPN Transistors in DMILL

Multi-stripe NPN transistors are potentially beneficial for improving the noise performance of the input transistors by lowering their intrinsic base resistance. In a single stripe NPN transistor two base stripes control current to one single stripe emitter. Each base stripe has access to an emitter on one side only. Additional emitter and base stripes give the base contacts access to emitter stripes from both sides, lowering the base resistance while increasing the area of the transistor in one dimension by about 4um per stripe. In one version of the submitted multi-stripe NPN devices we increased the distance between base and emitter by about 25% to relax the tight lateral dimensions and hopefully improve both yield and robustness. Measured NPN devices with 4, 10 μm long emitters display similar beta and radiation performance with virtually no failing devices detected. The V_{be} matching is better than the 1 mV resolution of our test setup. We intend to replace the 4, 20 μm single stripe input transistors currently used in each preamp with two of multi-stripe NPN transistors described above reducing the collector exposure to the back substrate by 22% and possibly improving the noise performance at the same time.

B. Input Protection Structures

The NPN transistor is chosen for input protection against spontaneous breakdown because of its inherent speed and robustness. For the TRT Straws, a coupling capacitor of 1nF will be charged to 1800 V, representing an energy of about 1.6 mJ. A spontaneous breakdown would cause one channel to discharge this capacitance directly. The speed of the breakdown is moderated somewhat because of the inductance of the connections and the addition of a 24 Ohm resistor in series between the amplifier and the wire. This impulse of energy requires a large area of silicon to protect the input transistors. A drawback of the present technique is that the collector of the NPN, which serves as the cathode when wired for input protection is directly above the back substrate. This node is directly wired to the input and requires significant area to achieve the 1.6 mJ of protection required. An alternative technique is to use the base–emitter junction, usually not a preferred technique since the reverse bias breakdown of a high frequency NPN is usually only a few volts. However this should not be an issue for the ASDBLR. It's common emitter input is at ~700 mV, well below the breakdown value for a reverse biased base emitter junction. With this configuration, the collector can be wired to a shield potential and serves to shield the input from signals on the back substrate. The only input capacitance added by this structure is the reverse bias base emitter junction capacitance since the emitter is the top level of the vertical NPN structure. In a test structure submitted to TEMIC, 21 expanded geometry NPN transistors with 3.4 X 19 μm emitters, and base to emitter lateral distance of 2.9 μm were wired in parallel to form a large input protection diode using the emitter base junction. Thermal runaway is avoided by expanding the distance between base and emitter to increases the intrinsic resistance in the junction. Bench tests on the fabricated parts have shown this structure capable of surviving 1.2 mJ discharges, offering almost three times more protection than the present input protection scheme utilizing collectors of conventional single stripe transistors. Qualification for use in the ASDBLR design was completed by examining radiation sensitivity with exposure of several devices to 10 year doses of neutrons and protons. No signs of increased leakage at levels that would affect the base current of input transistors have been found.

In the next submission of the ASDBLR we will use 20 single stripe NPN devices with emitter-base distance expanded to 3.4 μm and resize the emitter of protection transistor to 3.8 X 30 μm. This will increase the emitter length used in the test structures by 50% and hopefully produce an input protection structure that requires only an external 24 Ohm resistor to withstand the 1.6 mJ breakdowns of the TRT decoupling capacitors with high reliability.

VI. Acknowledgment

This ASIC development has had the benefit of many individual contributors whose work we would like to recognize:

Anatoli Romaniouk of the Moscow Engineering and Physics Institute (MEPHI) for guidance in developing, implementing and testing the design goals for the TRT front-end electronics. Serge Smirnov of MEPHI for his analysis of the ASDBLR test beam data shown in Figs. 5 and 6. Peter Lichard of the CERN ATLAS TRT electronics group for the design testing and readout of high density prototype boards for the ASDBLR and DTMROC. Philippe Farthouat, leader of the ATLAS TRT Electronics group for his help in arranging the irradiation of the ASDBLR and test structures. Godwin Mayers at Penn for his patience in building test fixtures, and assembling miniaturized components on boards designed for high density readout and Chuck Alexander at Penn for developing and implementing automated tests for the ASDBLR.

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