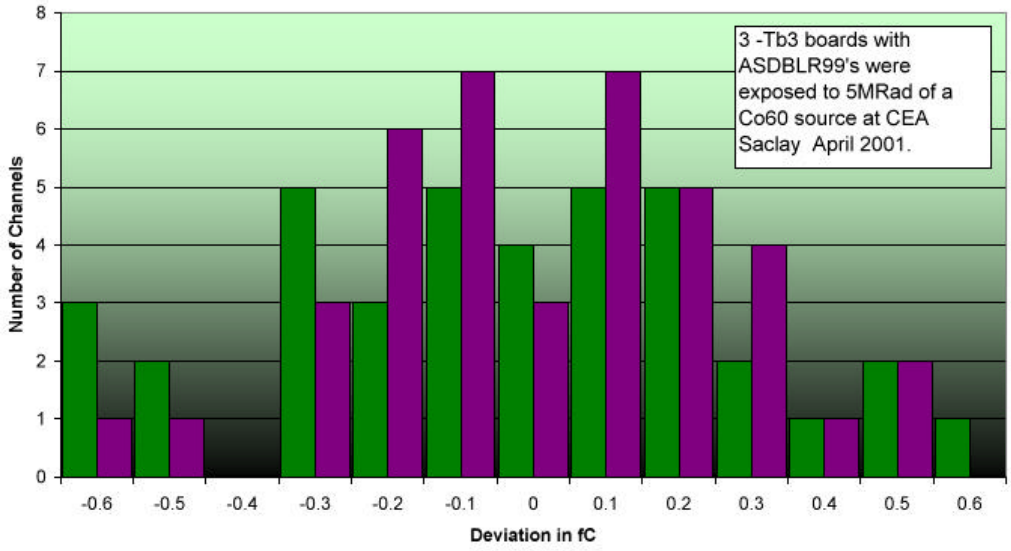
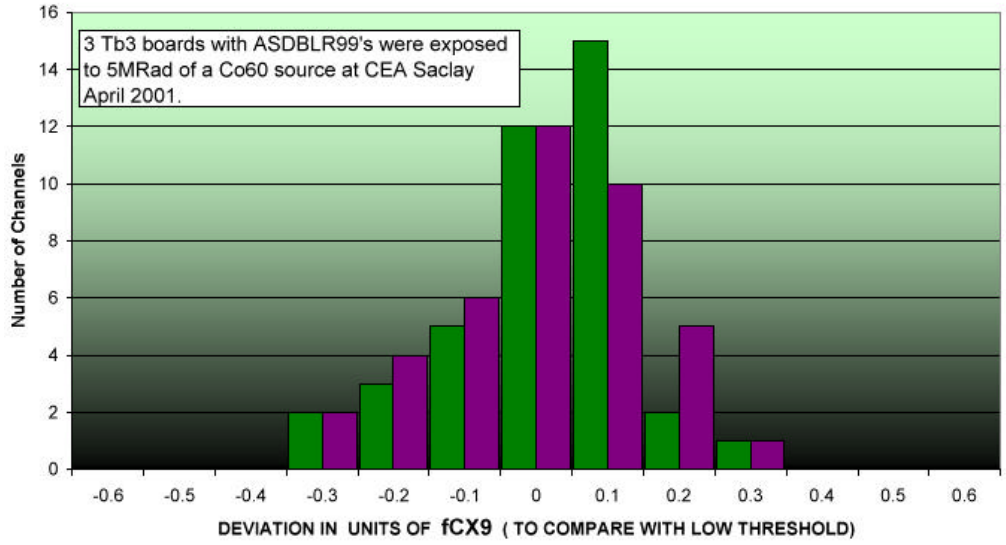
ASDBLR 99 Gamma Irradiation April, 2001

Five TB3 Boards (each with 2 ASDBLR ASICS) were exposed under power to a Co60 source at Saclay at a rate of 1.6Mrad per hour. All five were first exposed to 5Mrad. Two were exposed to a second dose of 5Mrad for a total of 10Mrad. An internal short to –3V developed in the current mirror reference for the output drivers of one chip exposed to 5Mrad. There was evidence of comparator activity internally on the chip. So this failure is related to the peripheral support function. All other chips remained fully functional. Channel deviations from chip average are shown in the plot below for the chips exposed to 5Mrad of Co60. The mean value of the thresholds for both high and low threshold did not change appreciably.

Pre (green) and post (purple) 5Mrad deviations from chip mean Low Threshold



Pre (green) and post (purple) 5Mrad deviations from chip mean High Threshold



The two plots on the previous page are scaled to the same comparator threshold sensitivity. The Track (Low) and TR (High) comparators are nearly identical copies. The sensitivity difference is determined by an attenuator network at the comparator inputs. The TR comparator is implemented by increasing the shaping time from 7.5ns to 10ns and by using a resistive attenuator network with a larger attenuation ratio. The result is that the inputs of the TR comparator are more directly coupled to each other desensitizing it to DC and other offsets from preceding stages. These results show that the comparator section is largely unaffected by the 5Mrad Gamma dose. The comparator circuit is nearly identical in ASDBLR99, 00 and 01.