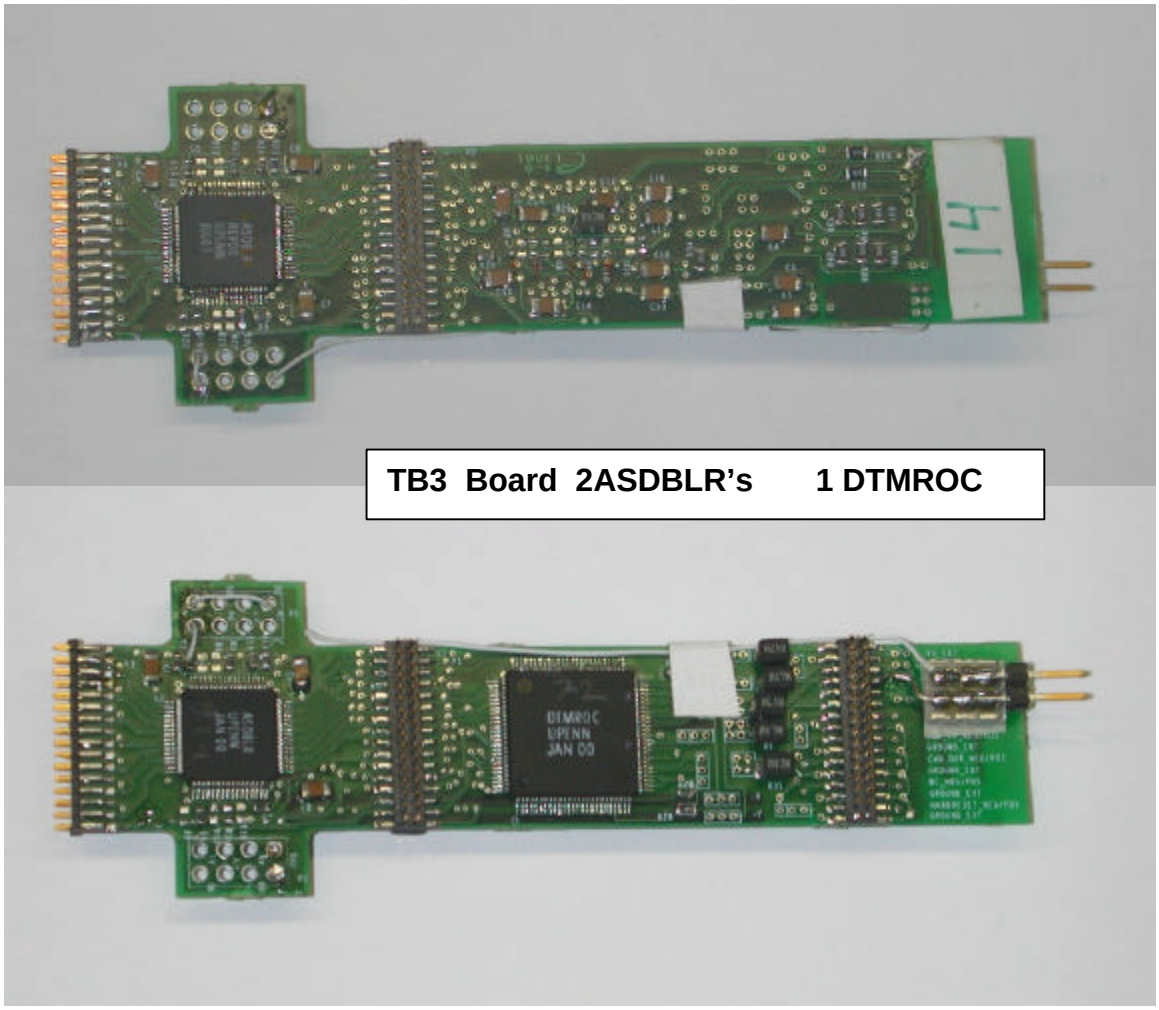
ASDBLR 99 Proton Exposure October 2000

Three TB3 boards (each with 2 ASDBLR ASICS) were exposed to the proton beam at CERN. The chips were powered and placed on a mobile platform that scanned across the beam to expose uniformly an area of approximately 8X8cm. A total dose of $1X10^{14}$P was administered to all three boards.



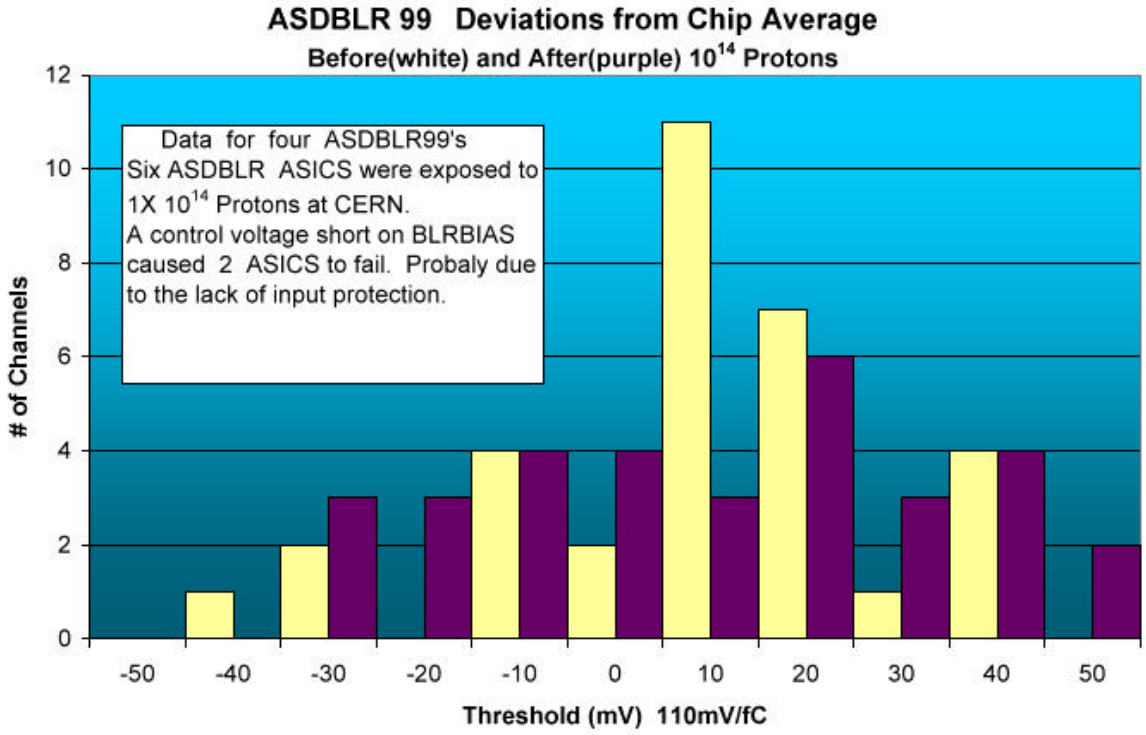
Chip Level Failures

After the proton exposure we found the BLR bias line which does not have input protection in ASDBLR99 shorted to the –3 power rail on two of the chips (Two different TB3 boards.) This control line was rigged with a hand wired lead and connector for external control. It is a diagnostic input and is not usually connected to anything. After examining the layout and schematic we added input protection on the ASDBLR00. This line was unwired in all subsequent radiation tests and has not been observed to fail since.

ASDBLR 99 Proton Exposure October 2000

Parametric Changes After Exposure

The change in the mean threshold indicates only a small loss in gain, ~10% after exposure so the deviations from chip average are shown without gain adjustment below. No significant increase in deviation is observed.



Power

Only a small change in current draw is observed.

Measured Supply currents for one TB3 board

Supply	Pre Rad (mA)	Post Rad (mA)
+3V	105.3	101.6
-3V	80	75.5

Power Off Input resistance

ASDBLR 99 Proton Exposure October 2000

The input of each preamp is connected to ground through the junction of the 20K feedback resistor with a 6K resistor to ground that supplies current to the output emitter follower. Mean value measured before and after exposure is:

Average Input Resistance Before and After Radiation

Pre Rad	Post Rad
27KΩ	29KΩ

Change in Gain

The absolute threshold for a constant input charge is a sensitive function of gain. The small change in gain for both the low and high thresholds at 5Mrad and 10Mrad implies that we should expect only a small change in gain as a result of exposure to relatively high amounts of ionizing radiation. The threshold gain for the low threshold is ~ 110mV/fC

Average Threshold for all exposed chips Pre and Post Rad

Comparator	Pre Rad (mV)	Post rad (mV)
Track (Low) 3fC	435	393
Tr (High) 30fC	352	326