Block Name: CMOS_CMP (AKA DC_COMP)
DSM Comparator Block for Voltage and Temp Sensing

Size: Area = 185X225 μm

Power Requirement: - 2.5V +/- 0.2V .7mW

Inputs:

- **IN+** Comparator + input (0 – 1.25V)
- **IN-** Comparator - input (0 – 1.25V)
- Bias PMOS MIRROR gate ref. for current mirror (17μA unit mirror) from CERN Library OTA BIAS)

Outputs:

- **Out** Digital high if IN+ > IN-

Functionality: The comparator has been adapted from a CMOS OTA amplifier in the CERN DSM Library designed by Paulo Moreira. We initially thought it could be used directly but found it desirable to have a wider output swing.
Refering to the schematic: Input transistors M7 and M8 are PMOS source followers operating at a current of about 16μA that provide a matched voltage translation of about 800mV to allow input voltages in the range of the DAC (0 - 1.25V) to be sensed. The differential pair M2 and M3 monitor the outputs of the source followers and each directs it's current to an independent diode connected PMOS mirror master, M5 and M4. M12 copies the of the current in M4 and directs it to a current summing output node. M11 copies the current in M5 which connects to an NMOS mirror pair M14 and M13. A current summing node is formed by connecting the drains of M12 (PMOS) and M13 (NMOS) . This high gain node, effectively the comparator output swings nearly rail to rail and is connected to a standard cell invertor that has been copied into the layout.

Given the relatively large size of the source followers, differential pair transistors and current mirror devces (L∗W ~120 - 200μm^2) we expect an offset of less than 2mV. For our purpose of remote sensing this is not necessary but it would be quite nice if the input matching was better than the least count of the voltage DAC used as the input reference for the comparator (5mV).

CMOS Comparator