# Block Name: LVDSdsmNcd
# Low Level Differential Driver with Tristate.

**Used in the DSM_DTMROC to provide "data out" always enabled.**

(Requires external termination for current output.)

**Used for 'DATA OUT' in the DTMROC**.

Size: Area = 223 X 243μm

Power Requirement: - 2.5V +/- 0.2V , ~12mW

Inputs:
Digital -
- oe - output enable High (2.5V) = Enable (Always HIGH in DSM_DTMROC)
- in - data Input for Low Level Driver

Analog –
- adjCur - Adjusts current (Short to Vdd unless lower current is desired) attaches through internal 2.3KΩ resistor to current mirror master.
- monSF- Allows monitoring of current source gate voltage. Diagnostic only. -->Not pinned out.<--

Outputs:
- outPlus – positive (voltage) going output. (3mA sink-source)
- outMinus – negative (voltage) going output. (3mA sink-source)

Output Reference – Current outputs must be referenced to an external voltage (provided by the receiver) of 1.2V +/-.3V A small net current, due to the mismatch in PMOS and NMOS output current mirrors is expected. (~50uA)

Functionality:
Originally designed to provide low level differentia current outputs for both 'DATA_OUT' and 'cmd_out' this block will be used only for 'DATA OUT'. The tristate function will not be used output 'oe' = will be tied hi. LVDSdsm3Ncd provides a fast trigger output will be used to drive 'cmd_out' data.

| In | outPlus | outminus |
|---|---|---|
| Lo (0V) | 3mA sink | 3mA source |
| Hi (2.5V) | 3mA source | 3mA sink |

This block is designed to have constant current draw in all modes of operation.

Termination - In order to allow careful termination the long twisted pair lines, a high impedance output is utilized. A fixed reference of ~1V at the receiver is

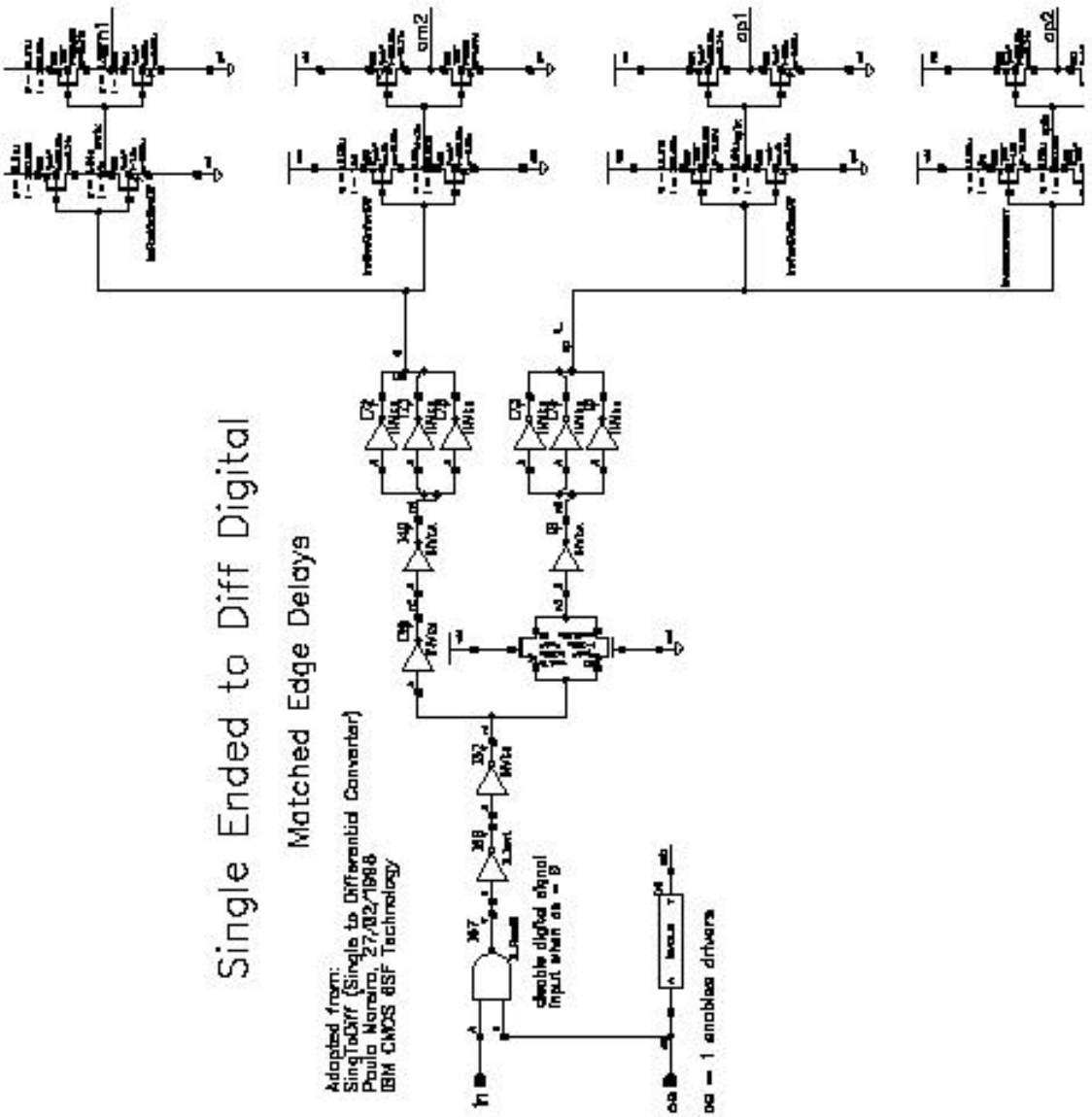
required and will be part of the termination network. The load used in our SPICE characterization includes 50Ω on each output to a common node connected to a termination voltage through a 75Ω resistor. Stray capacitance is modeled using 12.5pF between outputs and 12.5pF on each output to gnd. SPICE calculations and tests of prototypes indicate that the LOW Level Driver should be able to operate at data rates well in excess of 50MHz. A measured output can be found in the **Fastout** block description.

Schematics –
The **Single ended to Differential** drive (see schematic) has been designed to match the transition times of high to low and low to high transitions to minimize common mode on the output lines.

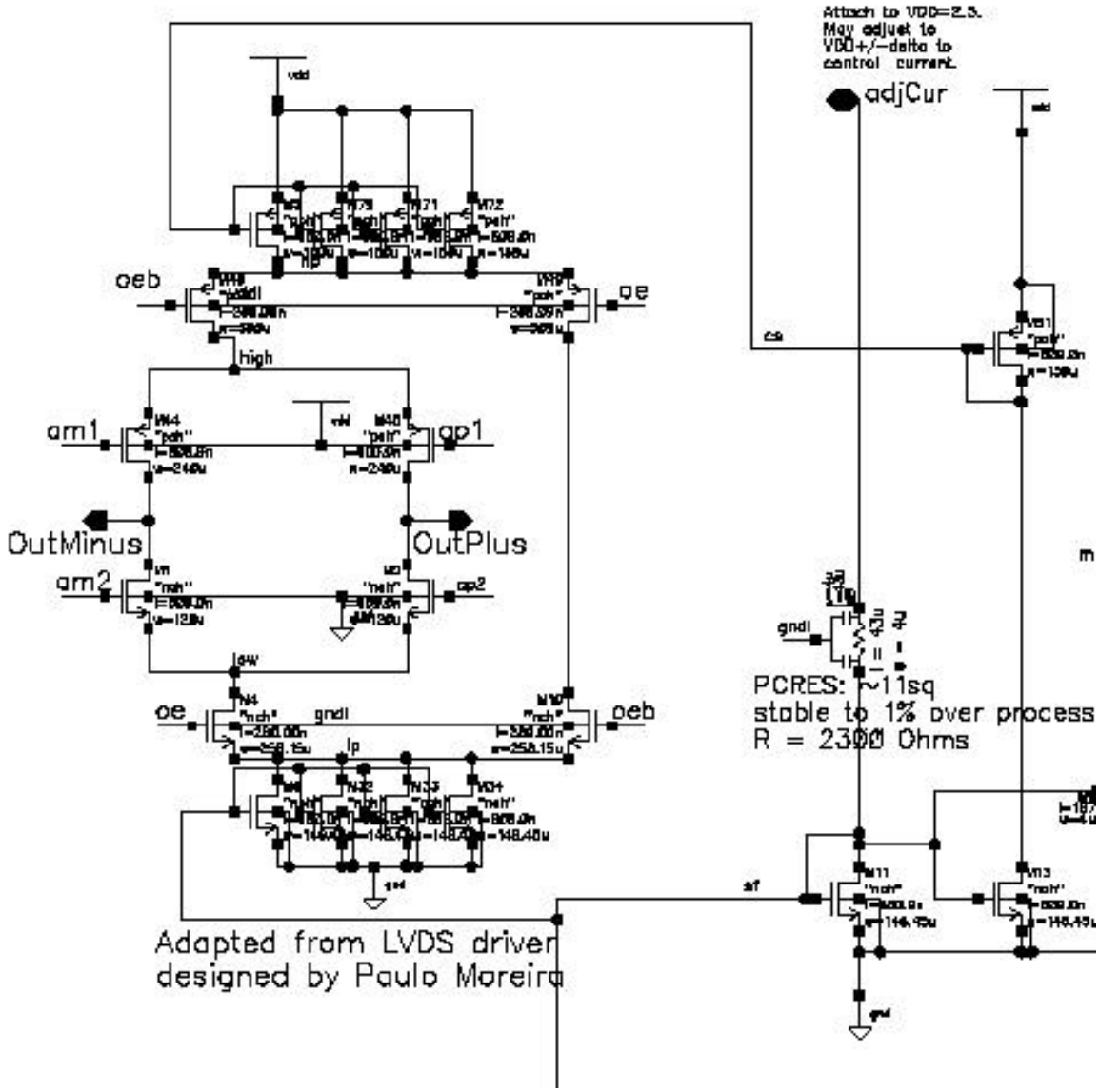
**Output Drive with current sources -** utilizes a constant current bridge drive network.
Each output (OutPlus, OutMinus) is connected to the drain of one NMOS and one PMOS switch. Current flows from the data selected PMOS switch through the output cable and termination and back through the cable to the NMOS switch. A matched 'sink' and 'source' current of ~3mA is provided by a simple current mirror scheme. Small differences in the output current can be expected due to differences in matching of the NMOS and PMOS current mirrors.

**Current Mirror masters for Low Level Driver -** A simple resistor based mirror master is used to provide the output current reference. of approximately 750μA. Output current depends most directly on the fabricated value of sheet resistance, PCres, (211Ω/sq). No difficulty is envisioned with the +/-20% spec, however we expect this is a very conservative value.

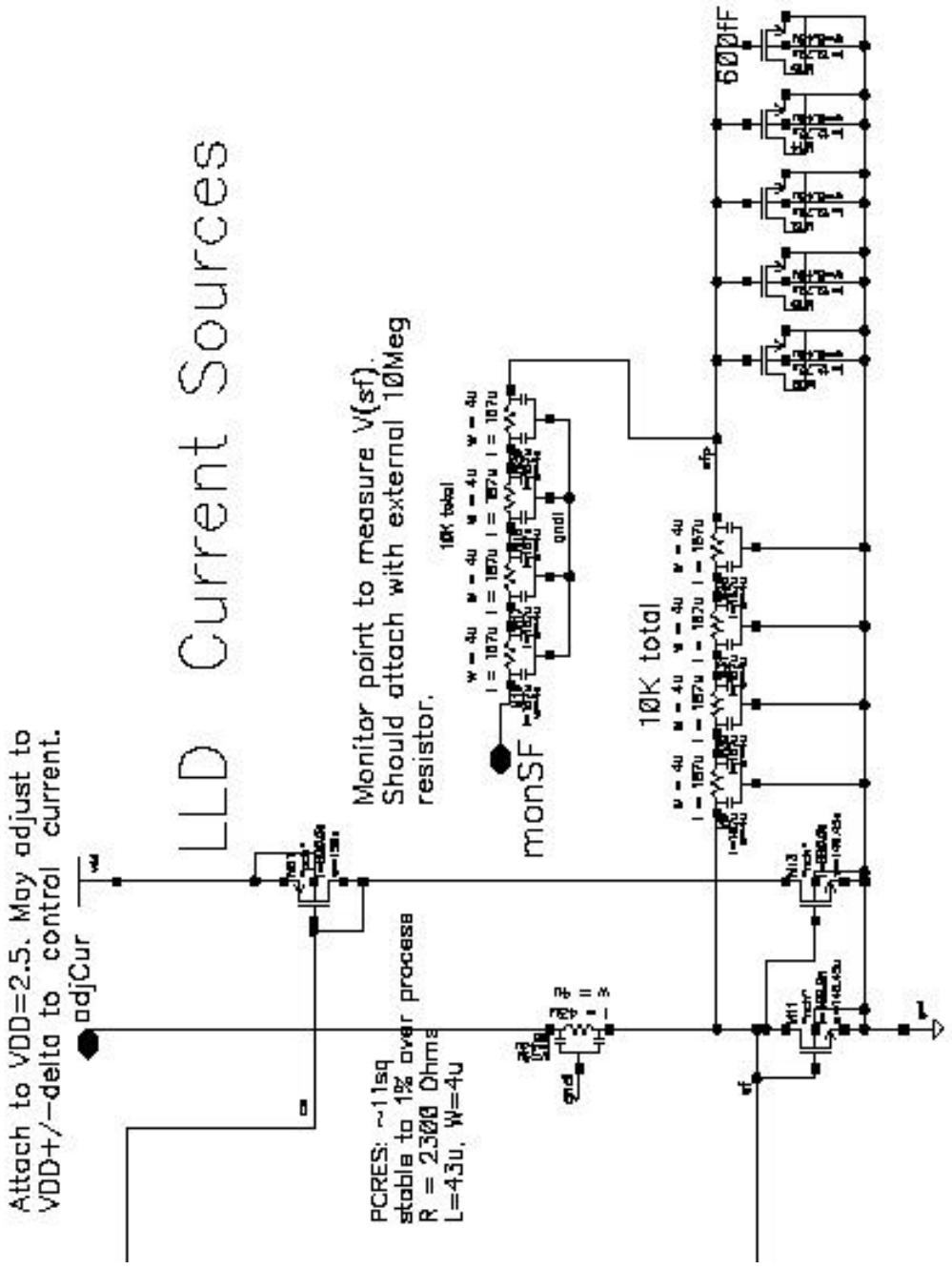
**Single ended to Differential Drive**
(Digital Logic)



**Output Drive with Current sources and Current Mirror Master**
(see next schematic page for complete Mirror Master)



## Current Mirror Masters for Low Level Driver



# **LVDSdsmNcd** Layout

220 X 243µm