Block Name: LVDSdsm3Ncd
Low Level Differential Driver with Tristate and Wire OR.
(Requires external termination for current output.)

Used to provide both 'cmd_out' data and a fast trigger mode.

Size: Area = 354 X 243μm

Power Requirement: - 2.5V +/- 0.2V , 14mW

Inputs:
Digital -
- wr - wire 'or' enable
- oe - output enable
- wr_datain - logic levels for 'or' output
- cmd_datain – standard data output for Low Level Driver

Analog –
- adjCur - Adjusts current will attach to Vdd in this version
- monSF- Allows monitoring of current source gate voltate. Diagnostic only. →Not pinned out.←

Outputs:
- outPlus – positive (voltage) going output. (3mA sink-source)
- outMinus – negative (voltage) going output. (3mA sink-source)

Output Reference – Current outputs must be referenced to an external voltage (provided by the receiver) of 1.25V +/-.3V A small net current, due to the mismatch in PMOS and NMOS output current mirrors is expected. (~50uA)

Functionality:
Low Level Driver is enabled by 'oe' = hi for either of two operational modes.
Outputs nominal 3mA +/-.5mA
1) wr = low (0V) Full current (3mA) output mode. Intended for use with only one device 'enabled' at at time when multiple devices are connected on the same databus.

cmd_datain	OutPlus	outminus
Lo (0V)	3mA sink	3mA source
Hi (2.5V)	3mA source	3mA sink

2) wr=high (2.5V) 1/2 current , zero offset mode. Outputs source or sink current only when input is high. This allows a wire 'or' mode of several chips together.

wr_datain	OutPlus	outminus
Lo (0V)	~0mA	~0mA
Hi (2.5V)	1.5mA source	1.5mA sink

Wire 'Or' mode was added as part of a *fastout* option to allow a self triggering mode, useful for initial checkout of detector mounted electronincs. In this mode, any of the 16 ternary inputs (attached and enabled) that has dete cted a signal over its selected threshold will apply a logic high at the wr_datain Note that wire 'or' refers only to the connection of multiple , enabled, low level drivers in wire or mode.
When multiple outputs are connected in parallel (up to ~13) the currents add. More than one Low Level Driver output triggering can be detected with a level sensitive receiver. Since the output is ~0 when wr_datain is low no cumumulative offset results when multiple low level drivers are connected in parallel.

Termination - In order to allow careful termination the long twisted pair lines, a high impedance output is utilized. A fixed reference of ~1.25V at the receiver is required and will be part of the termination network. The load used in our SPICE characterization includes 50Ω on each output to a common node connected to a termination voltage through a 75Ω resistor. Stray capacitance is modeled using 12.5pF between outputs and 12.5pF on each output to gnd. SPICE calculations and tests of prototypes indicate that the LOW Level Driver should be able to operate at data rates well in excess of 50MHz. An measured output can be found in the **Fastout** section.

Hookup - a special mode will need to be built into the ROD receiver to accommodate both output modes of this driver. One possibility could be to utilize a programmable offset and threshold in a differential comparator.

Schematics –
The **Single ended to Differential** drive (see schematic) has been designed to match the transition times of high to low and low to high transitions to minimize common mode on the output lines.

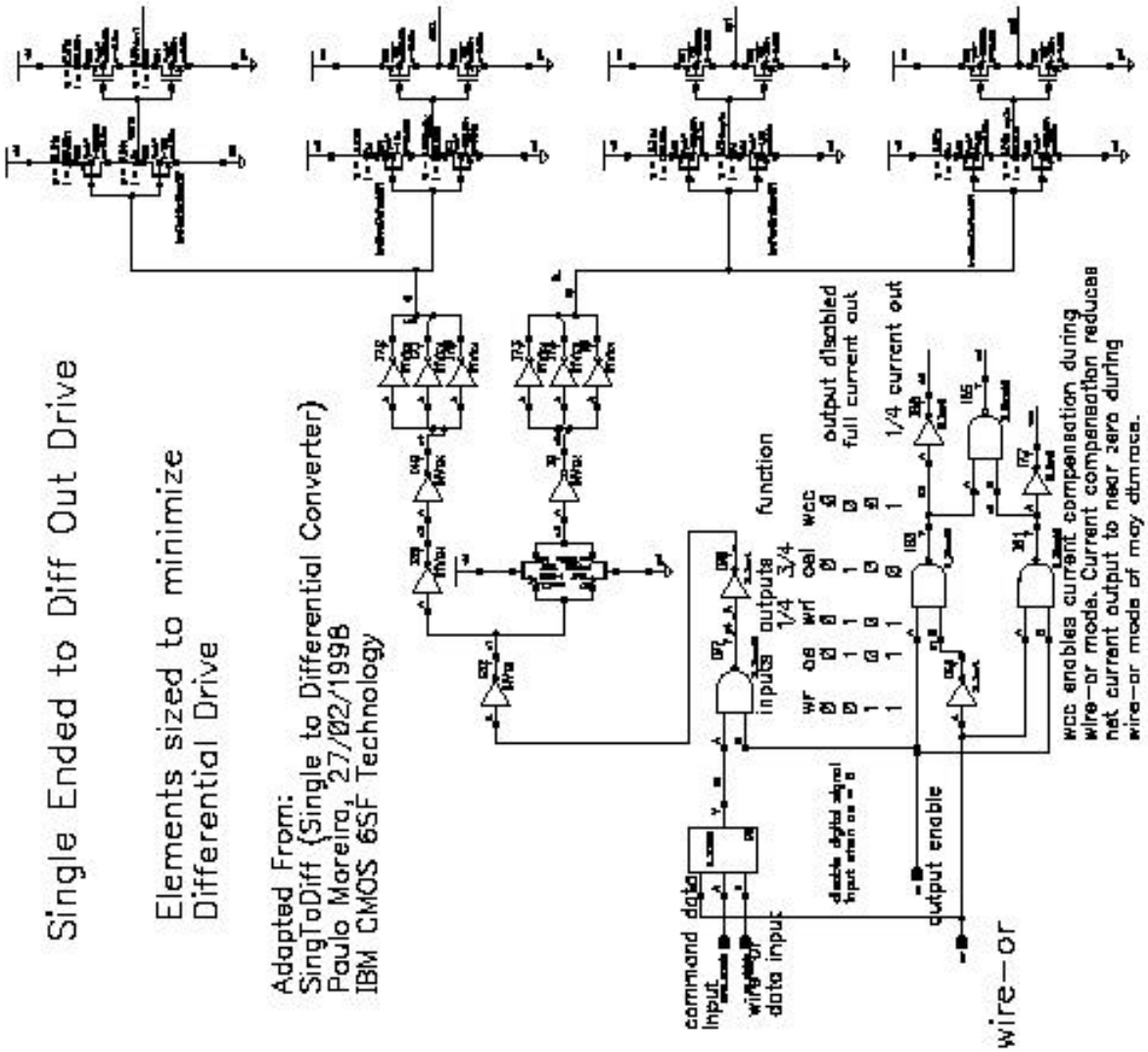
Output Drive with current sources - utilizes a constant current bridge drive network.
Each output (OutPlus, OutMinus) is connected to the drain of one NMOS and one PMOS switch. Current flows from the data selected PMOS switch through the output cable and termination and back through the cable to the NMOS switch.

A mode dependent matched current is provided to the NMOS and PMOS switches by a parallel current mirror pair in 1/4 and 3/4 proportion.
In 'Data Out' mode the parallel current mirror slaves are both switched on resulting in a matched 'sink' and 'source' current of ~3mA. Small differences in the output current can be expected due to differences in matching of the NMOS and PMOS current mirrors.
In wire 'or' mode the current source providing 3/4 of the data mode current is shunted around the switch allowing only 1/4 of the current to be switched by the bridge network. A parallel network is connected to the output providing 1/4 of

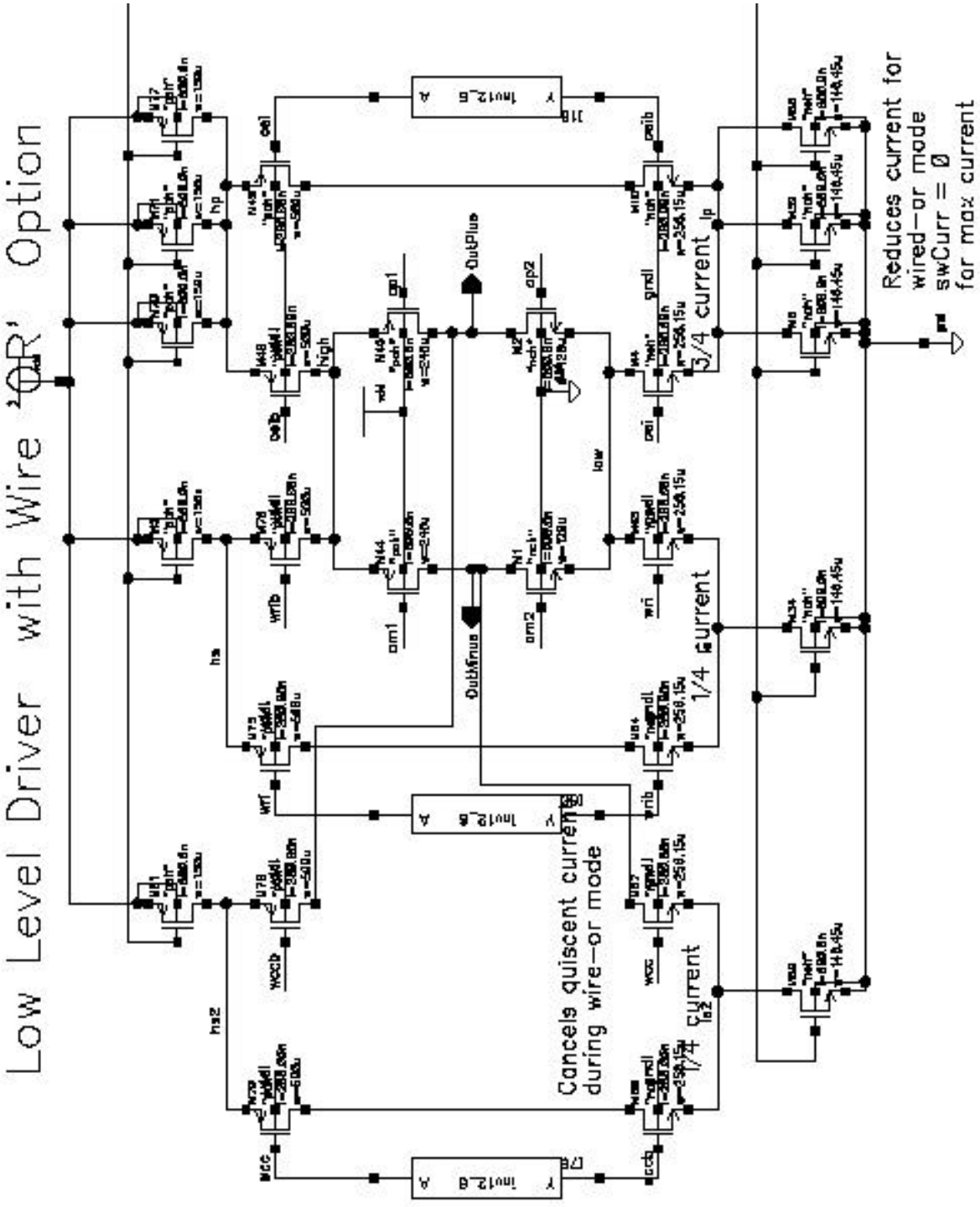
the data mode current to the outputs in a fixed state. It is wired so that when 'wr_datin' is low the currents cancel; no current flows through the cable and when 'wr_datin' is high the currents add resulting in a total current of 1/2 of the normal data mode value.
This block is designed to have constant current draw in all modes of operation.

Current Mirror masters for Low Level Driver - A simple resistor based mirror master is used to provide the output current reference. of approximately 750μA. Output current depends most directly on the fabricated value of sheet resistance, PCres, (211Ω/sq). No difficulty is envisioned with the +/-20% spec, however we expect this is a very conservative value.

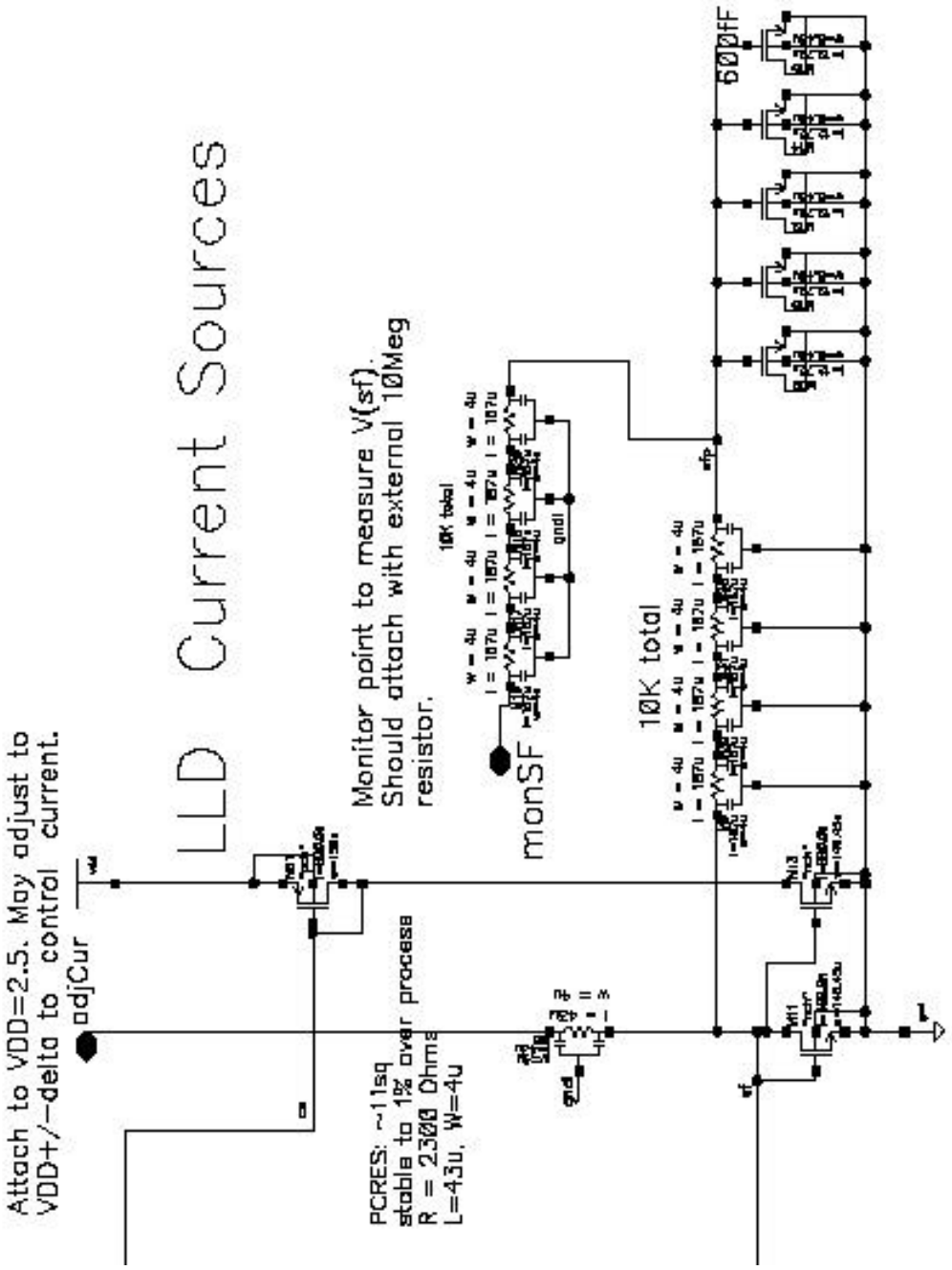
Single ended to Differential Drive
(Digital Logic)



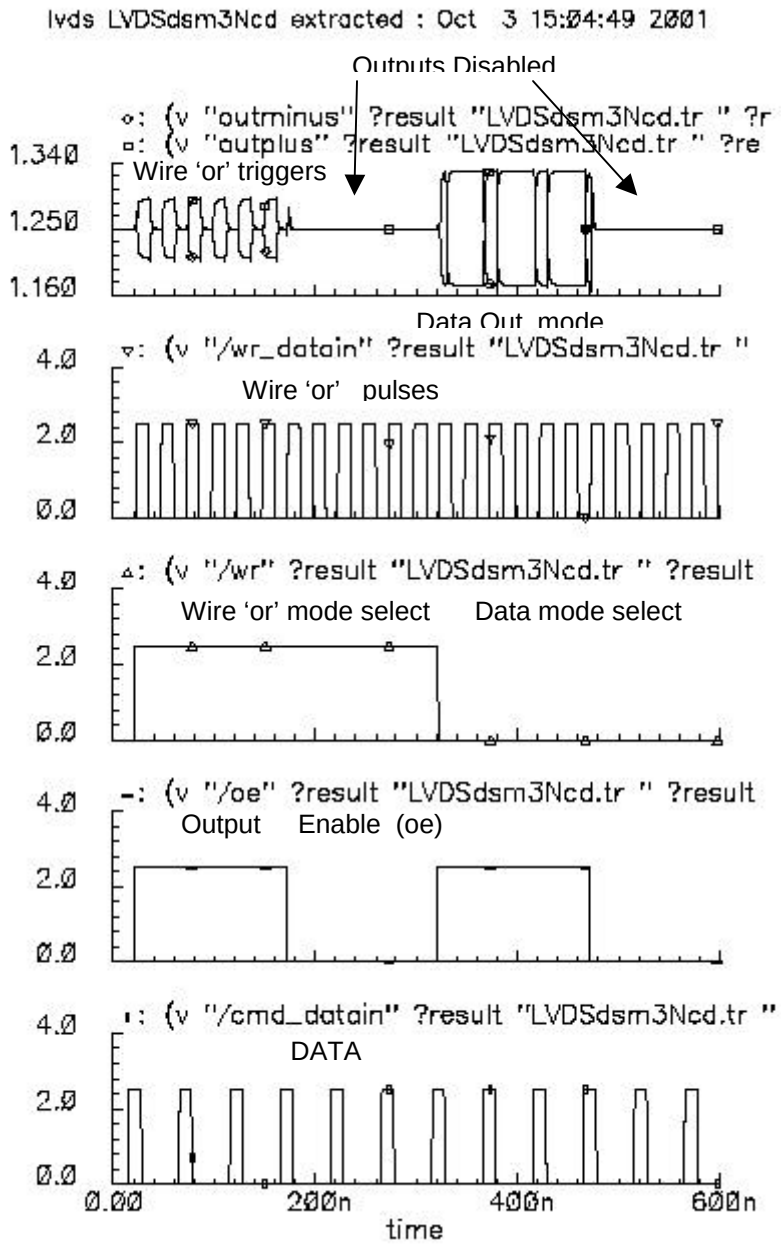
Output Drive with Current sources



Current Mirror Masters for Low Level Driver



SPICE Calculations



LVDSdsm3Ncd Layout

354 X 243µm