Block Name: powerup_V2

Power up circuit, senses Vdd-gnd and sends the trigger to an asynchronous 8-bit counter that provides the power on reset signal for the DTMROC.

Resource Blocks: E_Inv2 Enclosed Gate Standard Cell

Size: Area = 230X185μm

Power Requirement: 0.3mW Vdd >1.6 – 1.8V
Input:

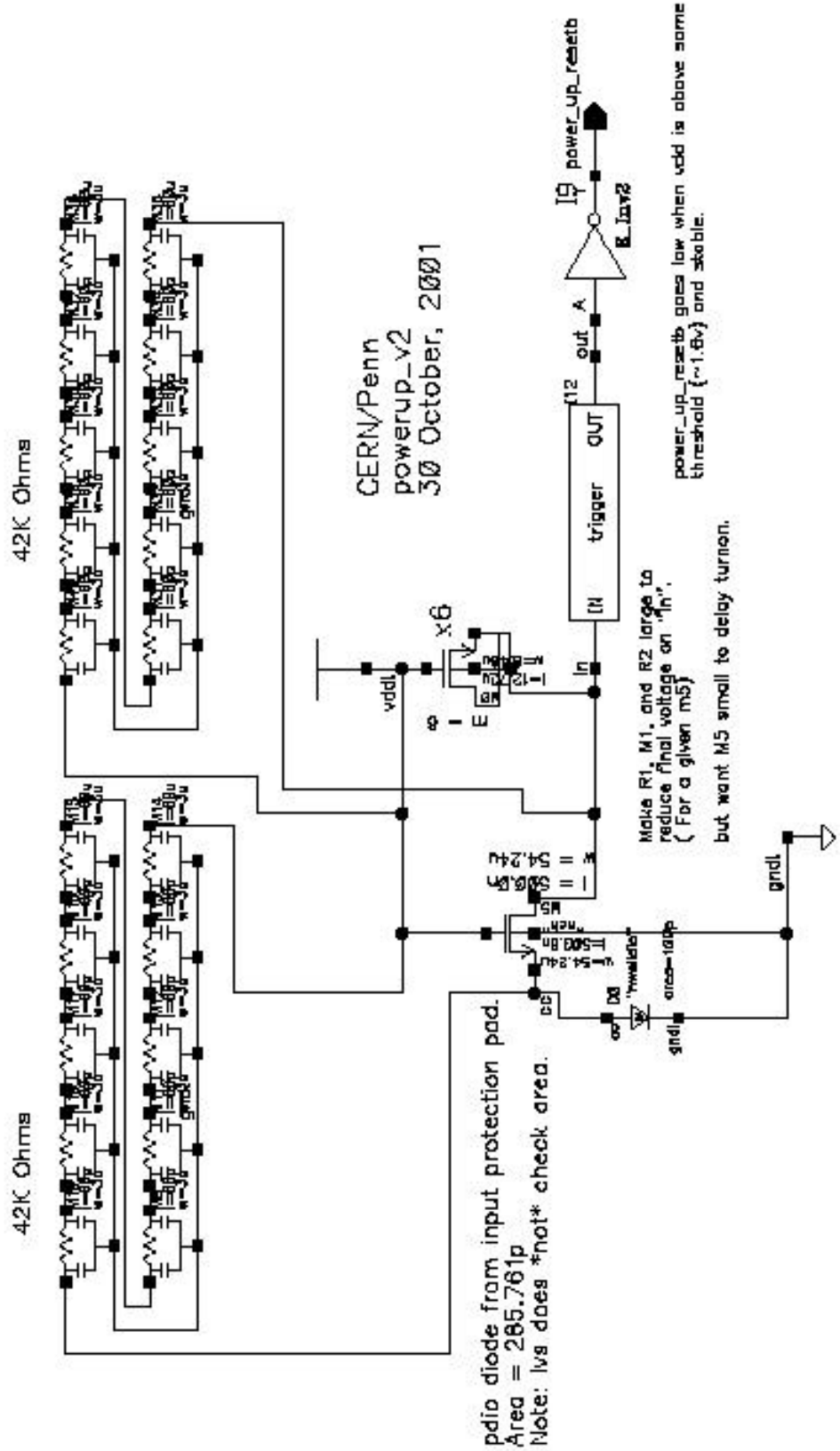
- Vdd (sense)

Output:

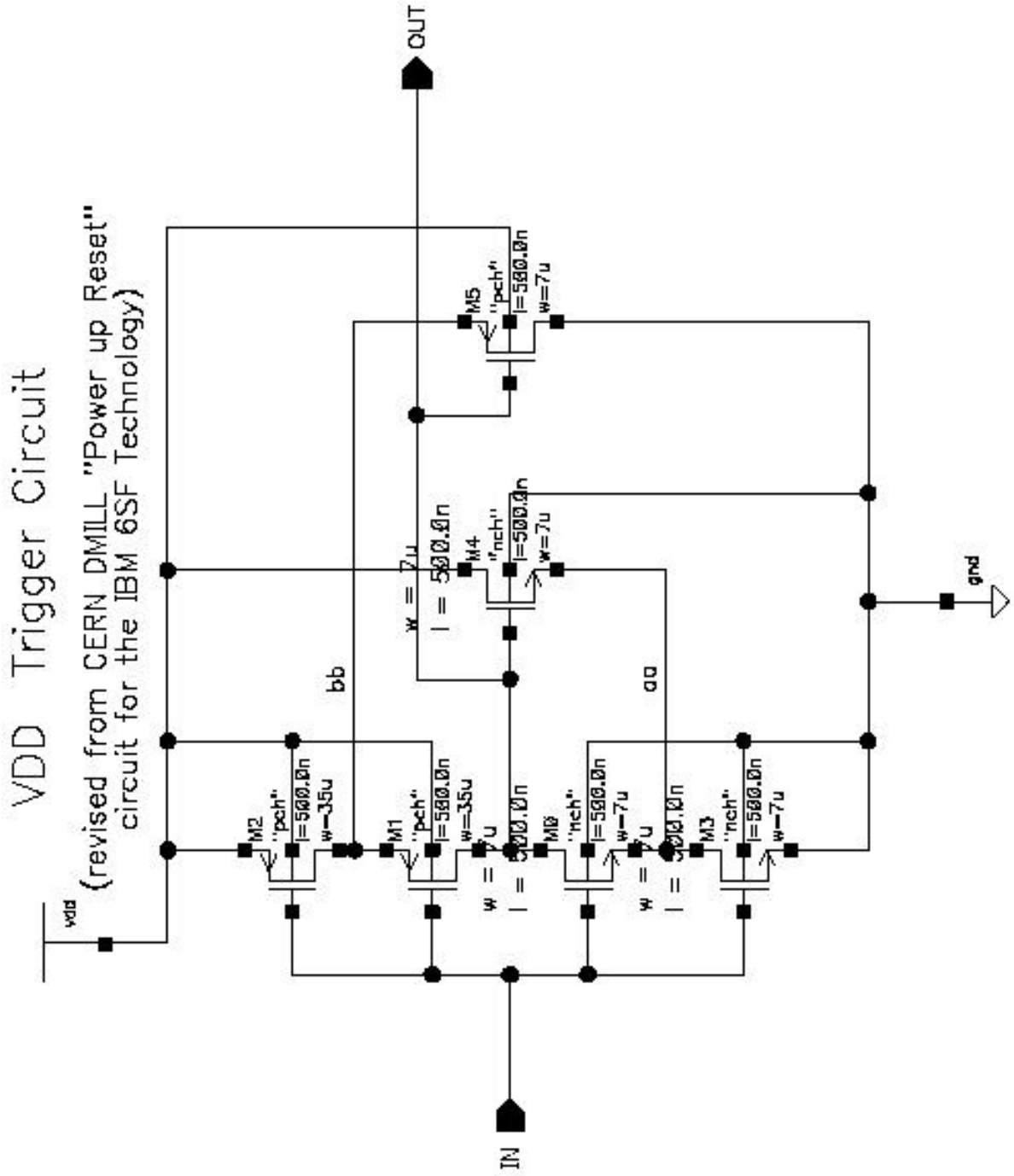
- power_up_resetb (low if Vdd-gnd > ~1.6V)

Functionality: A trigger circuit (see Trigger schematic) comprised of three PMOS and three NMOS transistors monitors the difference between Vdd and a diode controlled input, (IN). The output, **power_up_resetb** is set initially high and goes low when Vdd > 1.6V.

A capacitor (see schematic Powerup_V2) attached between the input (IN) of the trigger circuit and Vdd assures that the input will follow closely the potential of Vdd until current starts to flow in diode (D0). (Refer to Trigger schematic for the following.) This turns NMOS transistors M0 and M3 on to provide a low impedance path between the output (OUT) and gnd assuring a reliable initial, LO, state. As Vdd ramps up to ~1V current begins to flow in diode D0 (see schematic Powerup_V2) limiting the potential of the input (IN) to the Trigger circuit to approximately one diode drop above GND. In the trigger circuit current begins to flow in PMOS transistors M2 and M5 keeping the potential of the source of M1 somewhat below Vdd and keeping M1 whose gate is attached to IN off momentarily. When Vdd exceeds 1.6V the Vgs on M1 becomes large enough to turn it on and current flows into the OUT node pulling it high. M1 is 5X larger than M5 and creates a low impedance connection between OUT and Vdd. Since the gate of M5 (PMOS) is tied to OUT this transistor is turned off and the output is held high by the short to Vdd provided by M1 and M2 as long as the power is above 1.6V. A standard cell inverter, E_inv2, attached to OUT sets the proper polarity and insures a sharp transition of the **power_up_resetb** signal.

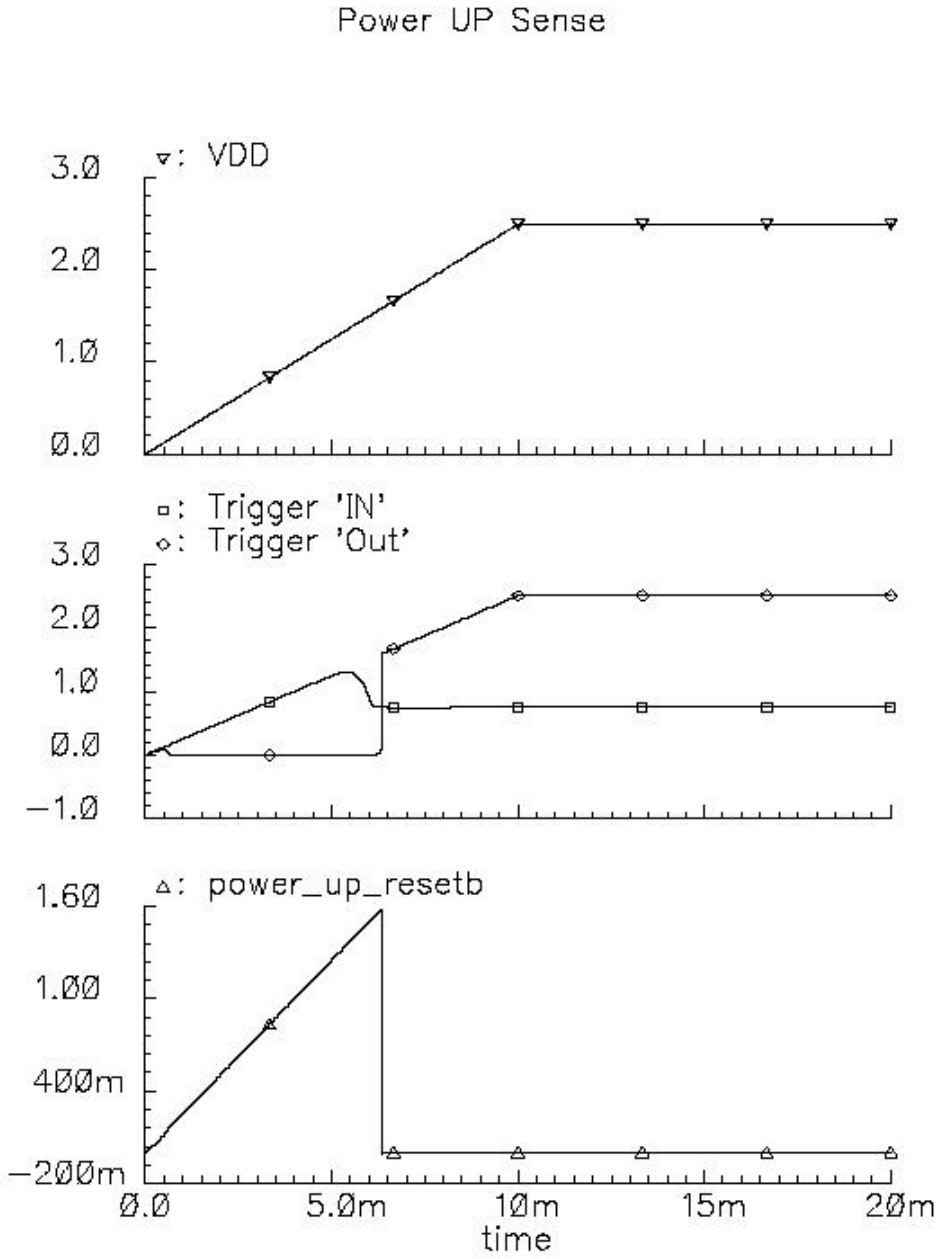

42K Ohms
42K Ohms
CERN/Penn
powerup_v2
30 October, 2001
power_up_resetb
power_up_resetb goes low when vdd is above some threshold (~1.8v) and stable.
Make R1, M1, and R2 large to reduce final voltage on "in". (For a given M5)
but want M5 small to delay turnon.
pdio diode from input protection pad.
Area = 285.761p
Note: lvs does *not* check area.
x6
trigger
OUT
IN
out
vdd!
gnd!

Trigger Block

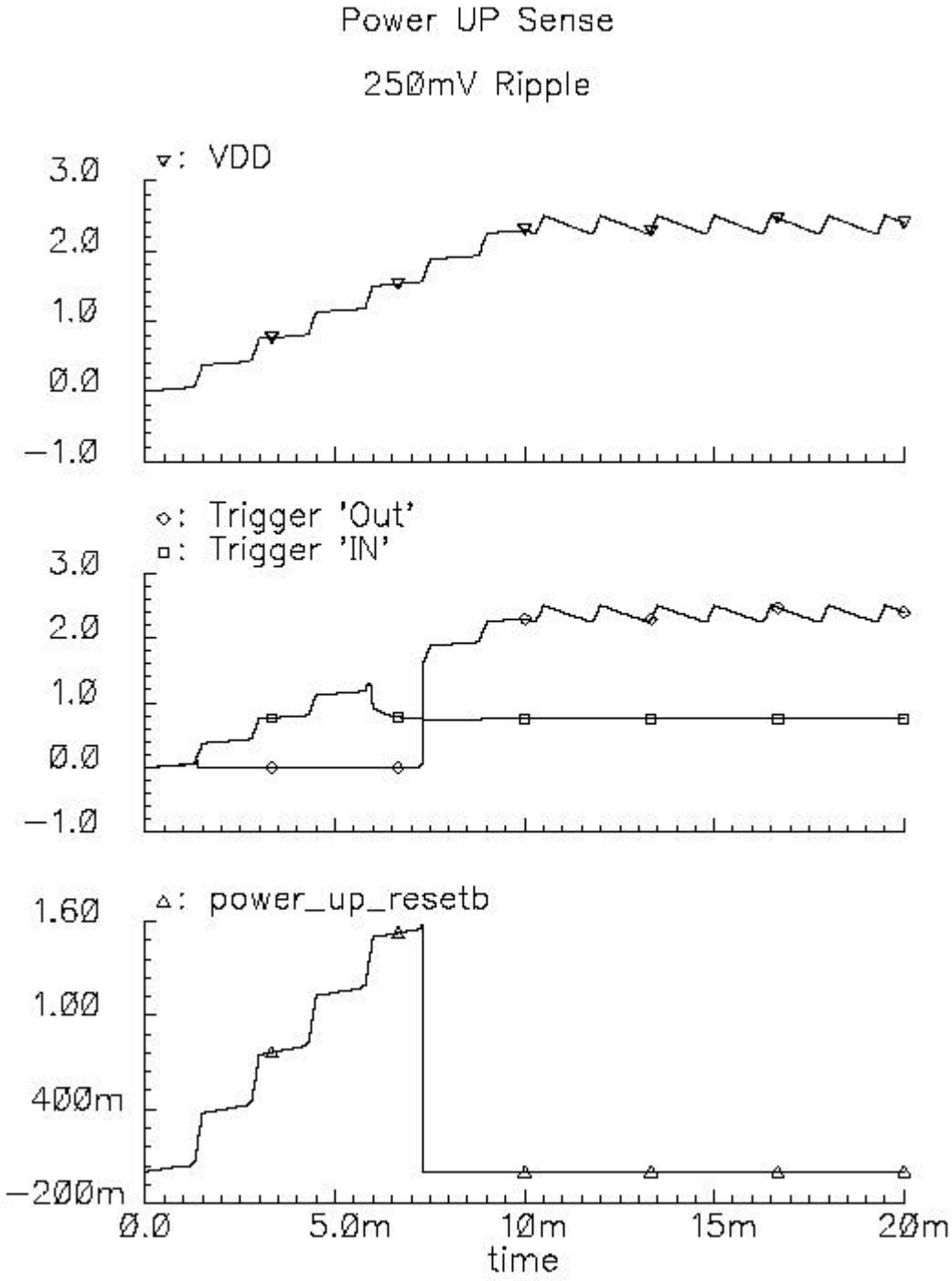


SPICE calculations

Initially we chose a diode connected NMOS transistor as the trigger sensor. (Presently D0). Variation of process from –3 sigma to plus 3 sigma caused a variation from .91V to 1.5V in one version in the trip point for **power_up_resetb**. A P-N junction diode provides a more robust voltage and significantly reduces this variation. SPICE calculations showed that changes in temperature change the trigger point by only 100mV and even when combined with changes in process the variation is less than 200mV. While the use of P-N junction diodes is not recommended we realize that they have been demonstrated to work in the Band Gap and are also used as input protection structures. The layout for the diode (D0) that we used has been taken from the Input protection pad.

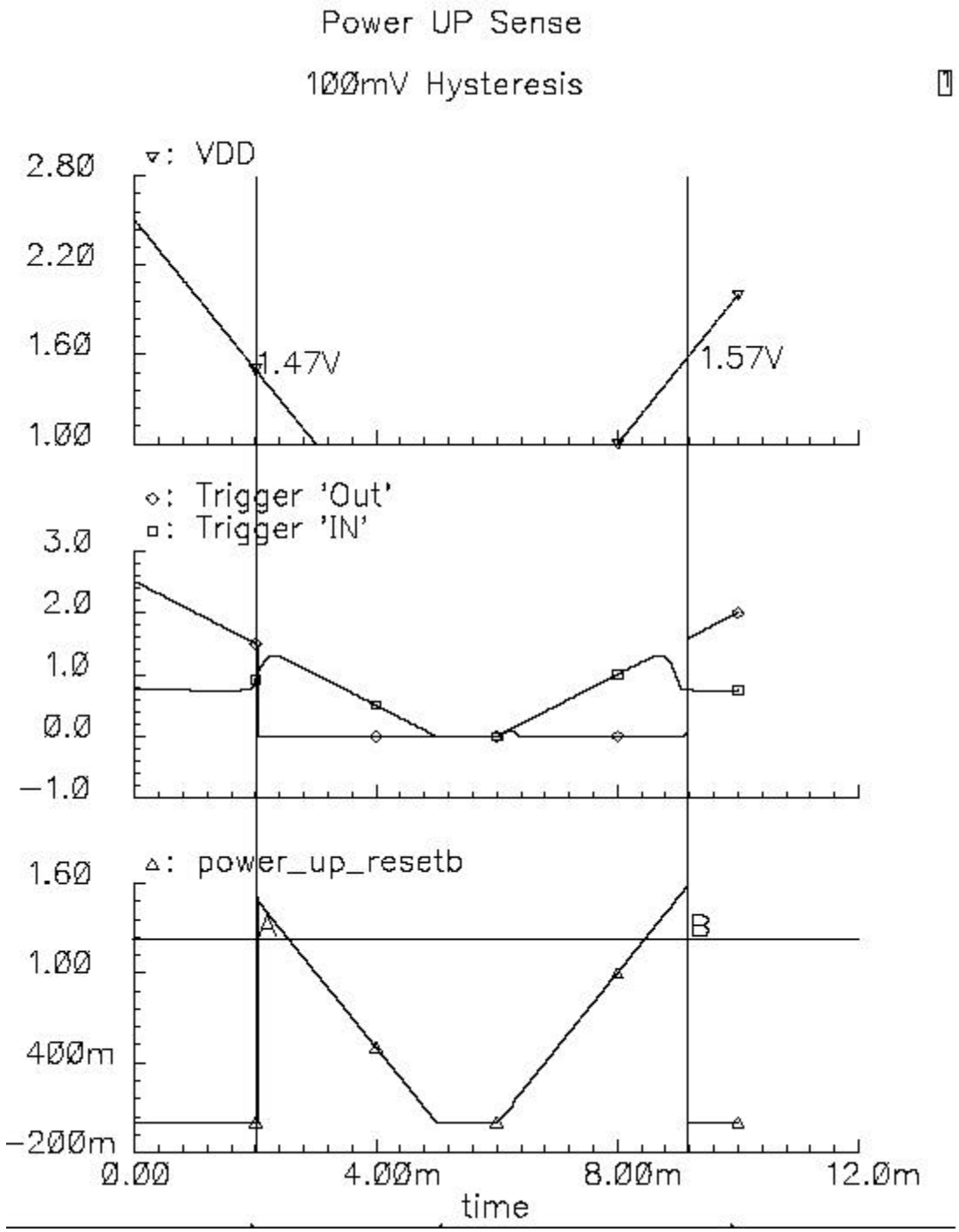


SPICE CALCULATIONS



SPICE Calculations

Vdd is ramped from 2.5V to zero and back up to 2.5V . The trigger points for which **power_up_resetb** switches are noted with vertical cursors and the values of Vdd at the trip point are noted.



LAYOUT