Block Name: Threshold_DAC_V2

Provides 2 8bit Programmable Voltage References.

Does **NOT** include data latching registers.

Size: Area = 785 X 425µm

Power Requirement: 2.5V +/-0.2V 2.3mW

Inputs:

Digital –

- <DH1:8> High threshold Register bits
- <DL1:8> High threshold Register bits

Analog –

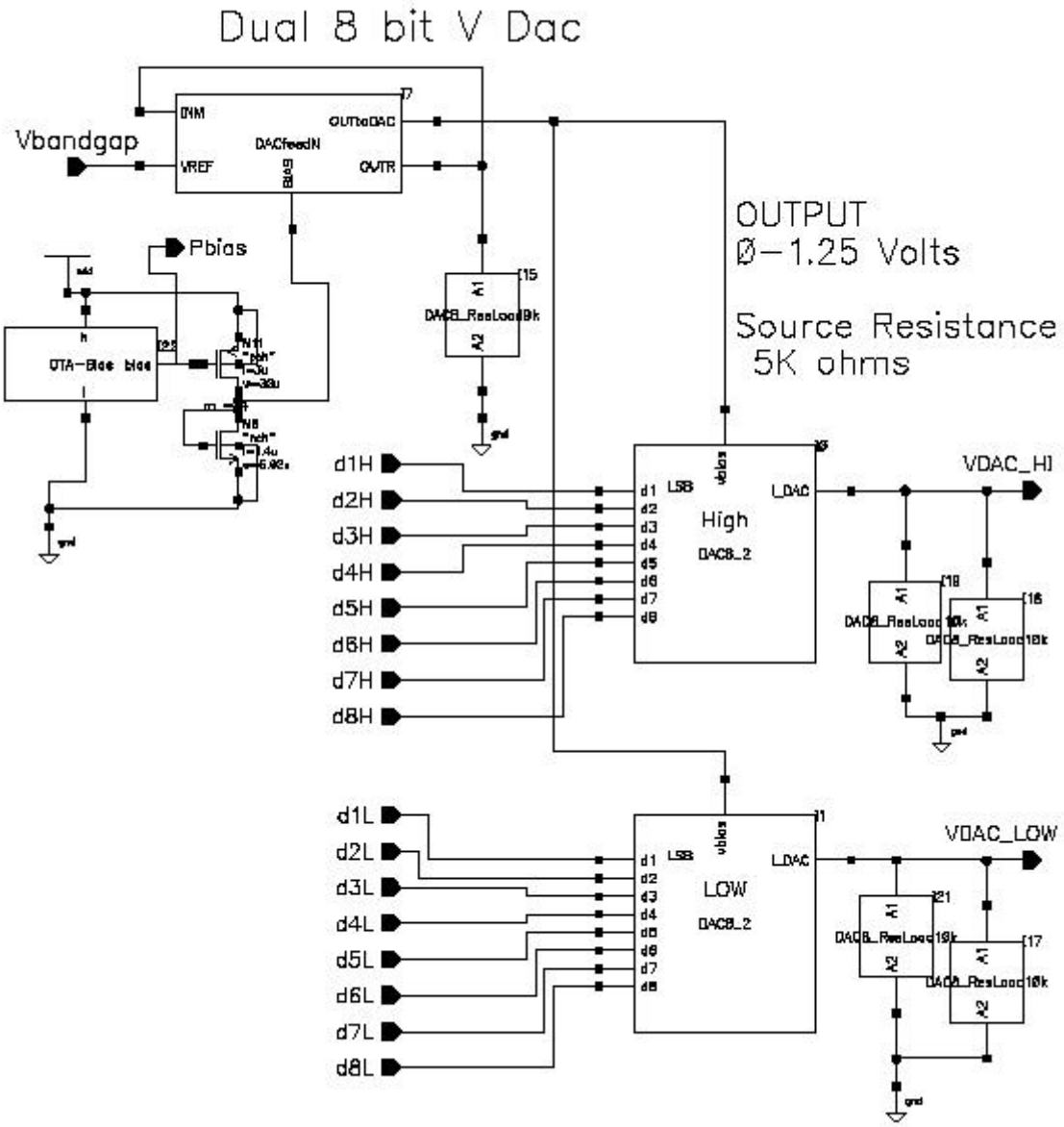
- Vbandgap - 1.25V (1.167V) Bandgap source

Outputs:

- VDAC_HI - 0-1.25V High threshold 8 bit DAC output.
- VDAC_LO - 0-1.25V Low threshold 8 bit DAC output.
- Pbias – bias generator output for PMOS devices locally.

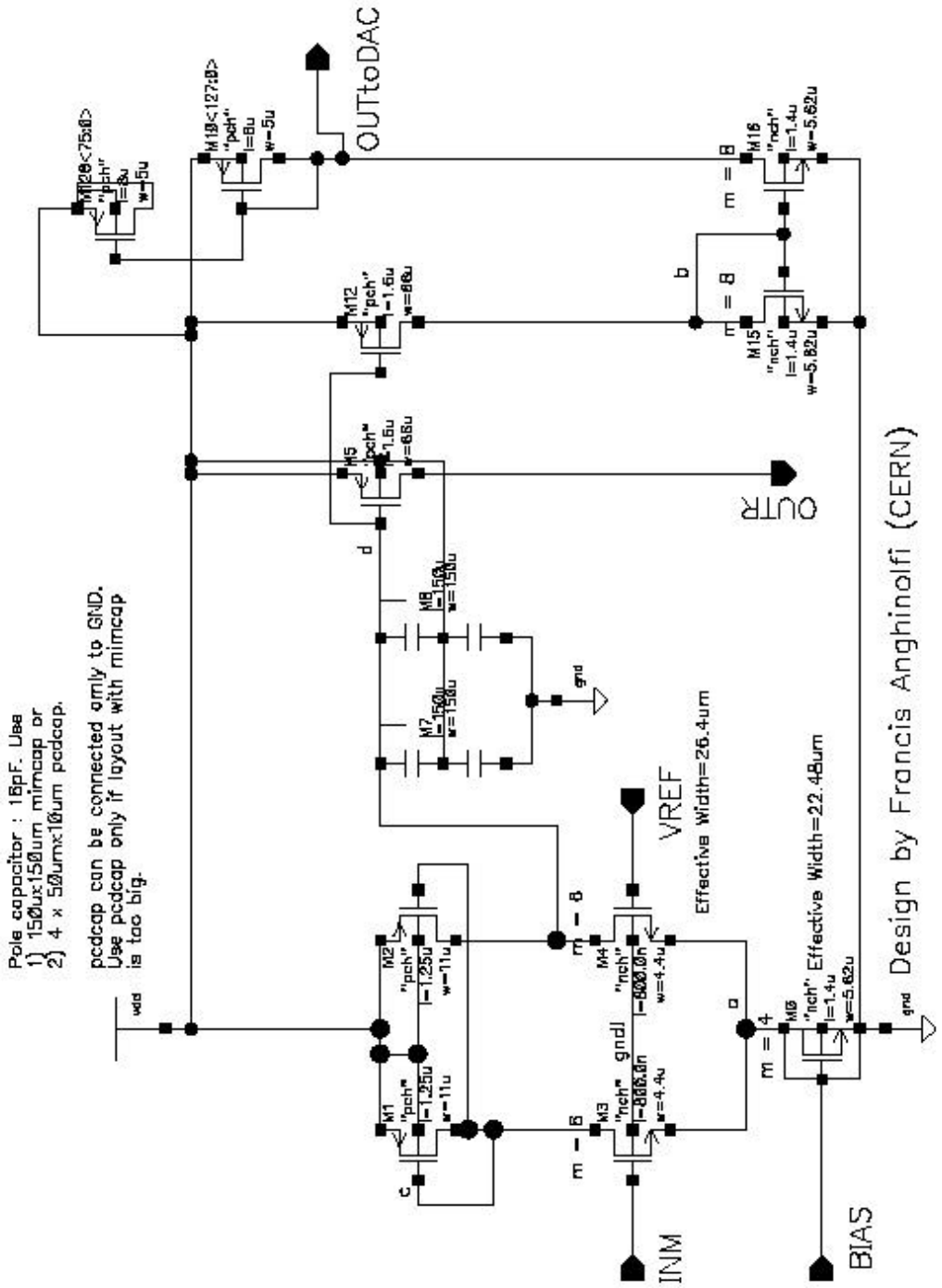
Functionality: Each threshold DAC creates an 8bit reference voltage with a source impedance of 5Kohms. Two 8bit switch arrays steer ratioed currents from current mirror slave devices to provide an 8 bit current output into a 5K resistor. Current in the mirror master array is adjusted by an Opamp driver to provide an output voltage across an internal resistor (~10K) that matches the band gap's 1.25V reference. This avoids sensitivity to process variation in both resistors the mirror reference transistors. The current mirrors and switches were fabricated in an MPW and appear to work properly, although there was an unresolved difficulty with programming of the LSB that is believed to be due to prototype's control logic.

Threshold_DAC_V2
Top level Schematic

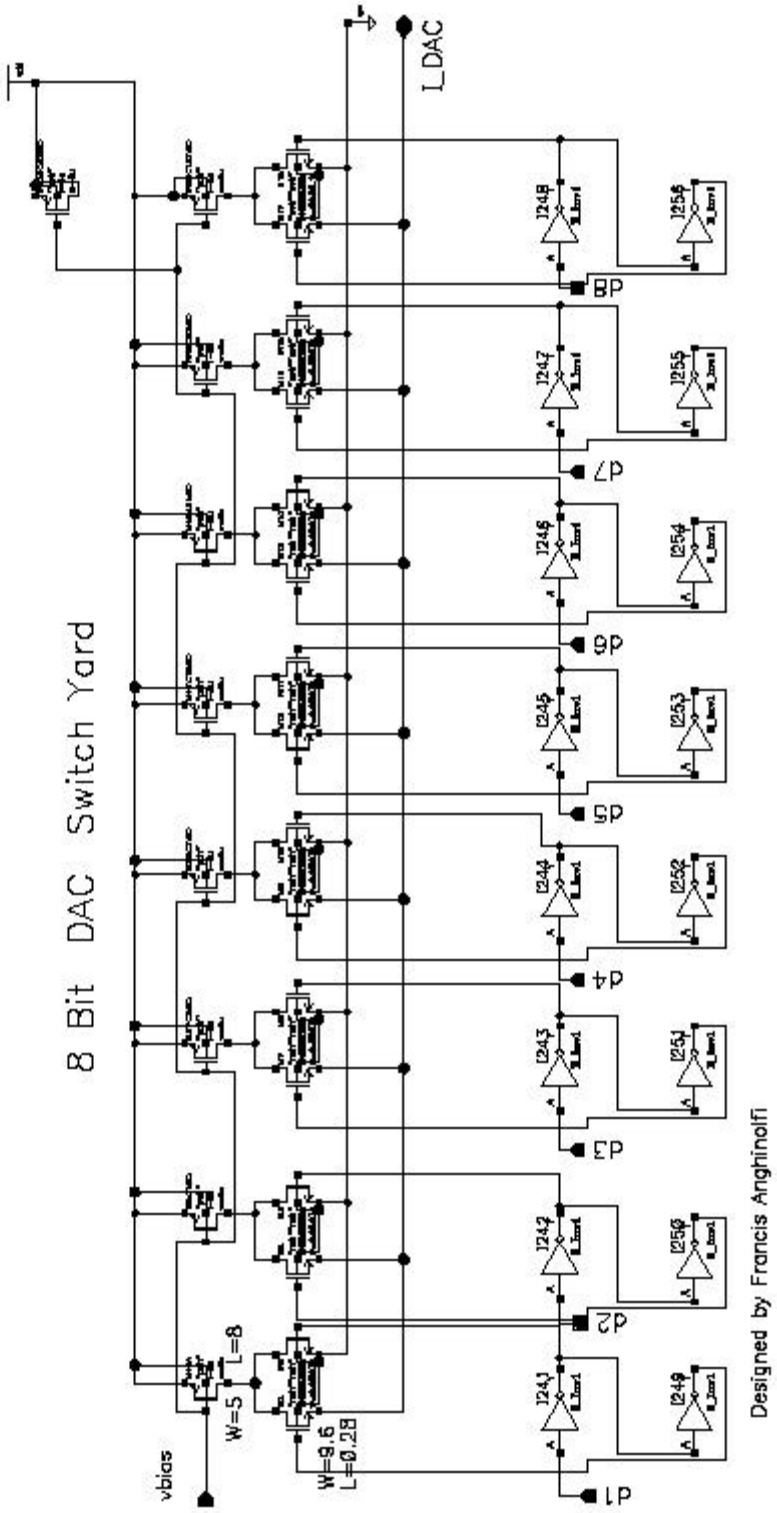


DACfeedN Schematic
(OpAmp Reference)

'OUTtoDAC' provides a current adjusted reference for the DAC PMOS current mirror slaves. The voltage at 'INM' is compared with VREF (the bandgap Vref). 'OUTR' provides a current output that attaches to an external (10K) resistor to GND. At the top level, 'OUTR' is connected to 'INM' to provide the feedback path.

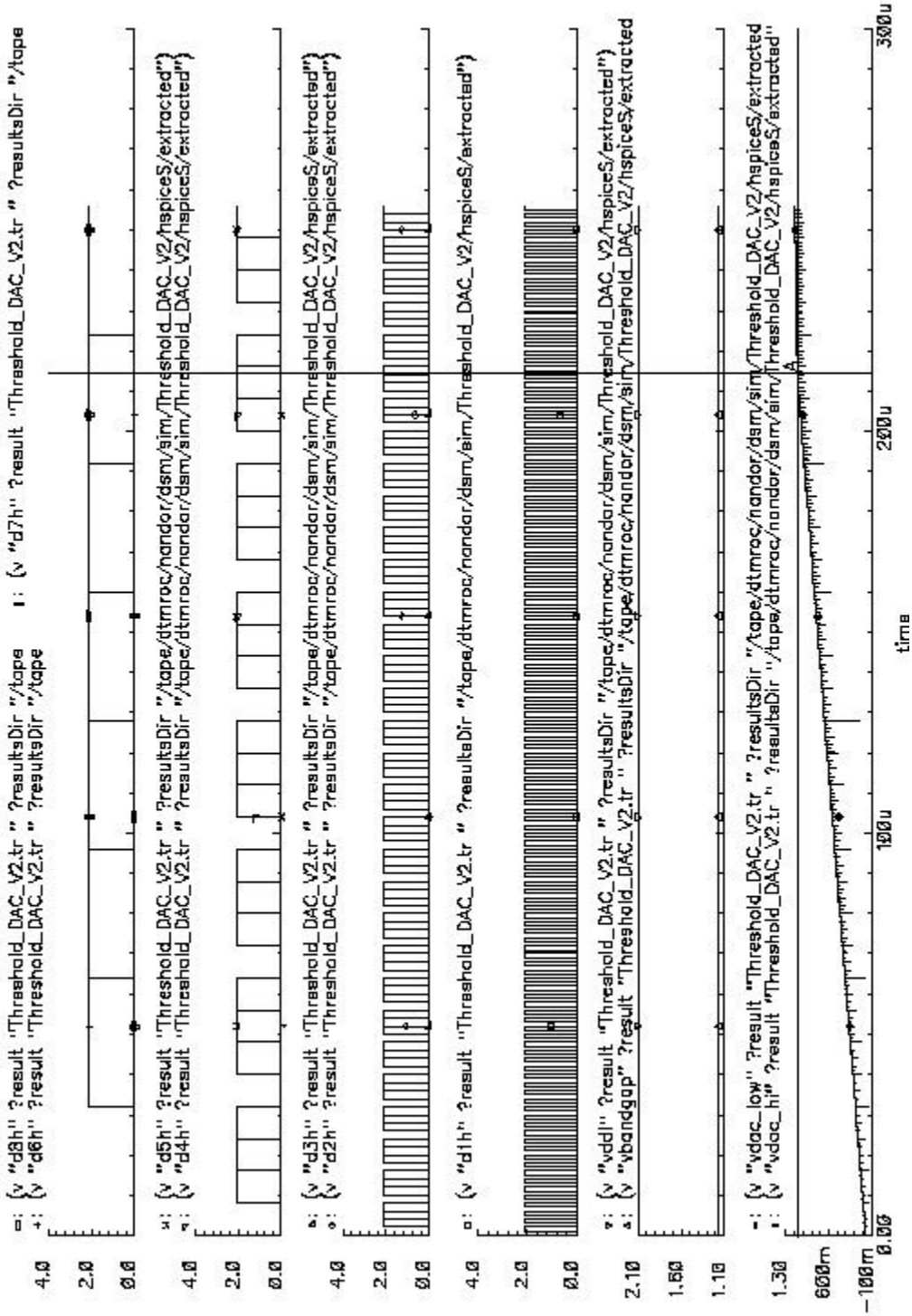


DAC8_2


LDAC
8 Bit DAC Switch Yard
d8
d7
d6
d5
d4
d3
d2
d1
vbias
W=5
L=8
W=9.6
L=0.28
Designed by Francis Anghinolfi

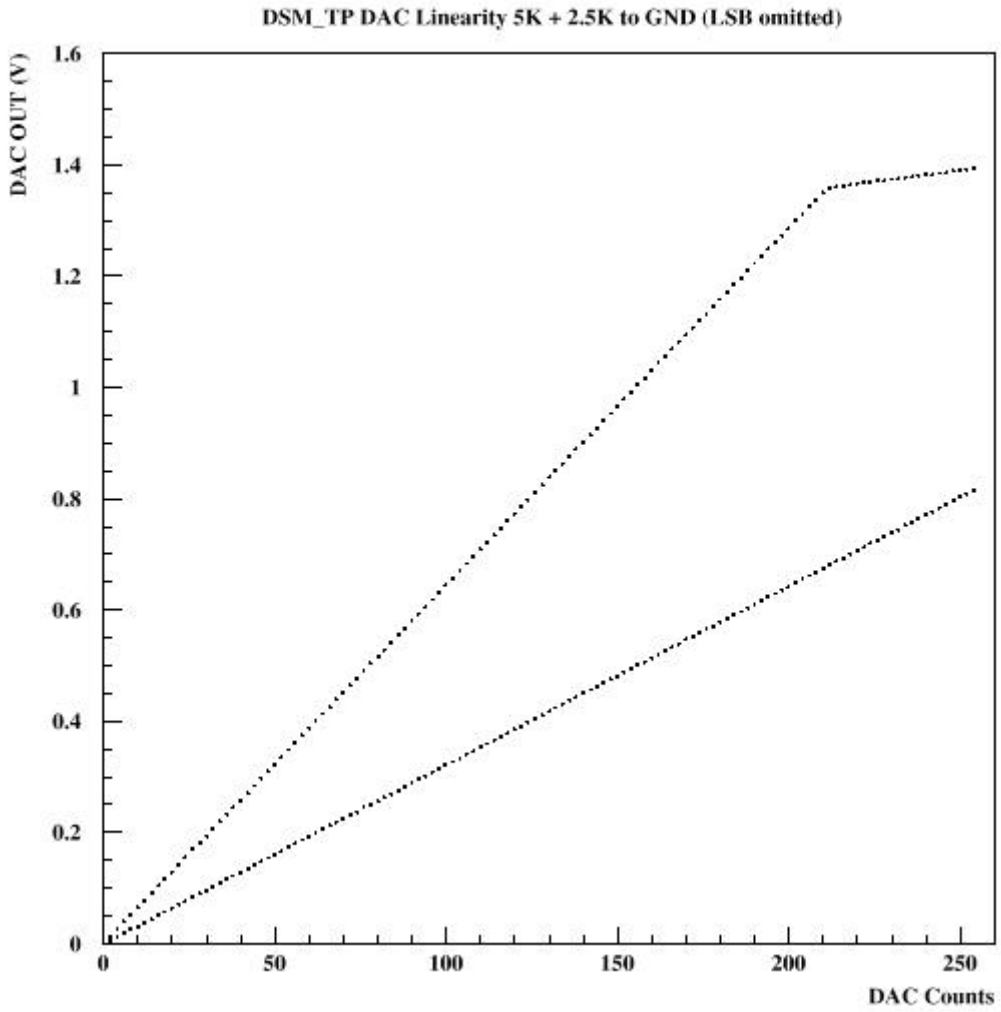
SPICE Sim of Extracte Netlist Vdd = 2.1V

Temp = 55C Nominal models. This simulation shows that the DAC saturates at 1.11V output, a setting of 210 decimal at the inputs. Lower Trace is DAC out. Second trace from bottom is Vbandgap = 1.16V



Measured DAC Performance

The DAC_8_2 with reference was fabricated in an MPW run. Although not an exact replica of the Threshold DAC it indicates appropriate compliance with a maxim output voltage in excess of 1.25V with a 5K ohm load. In this plot the LSB is not toggled.



Threshold_DAC_V2 Layout

Each of DAC consists of 256 identical PMOS unit current slaves. Reference for the slave mirrors is provided by a current mirror master consisting of 128 PMOS unit devices (L=8µm W=5µm). The master is sandwiched between the two DACS. Dummy devces are located around the periphery and an effort has been made to topologically break up the higher order current mirror devices. The Op-amp (upper right) ensures a drop of 1.25V across a ~10K reference resistor for the mirror master. Large capacitors (Top Center) are used to ensure stable feedback.