Block Name: V_T_Block
Internal Temp and Voltage Sensing with remote sense.

Analog Blocks Used: Threshold_DAC_V2, CMOS_cmp

Size: Area =   ~ 400 X 400μm (Layout in progress)

Power Requirement: - 2.5V +/- 0.2V   4.5mW

Inputs:
- **IN_Mon1** - analog input referenced to Dac8_A   → Output Mon1_Status
- **IN_Mon2** - analog input referenced to Dac8_B   → Output Mon2_Status
- **Dac8_A**   - 8 bit programmable Voltage reference input for
              Temp sensing diode and IN_Mon1
- **Dac8_B**   - 8 bit programmable Voltage reference input for
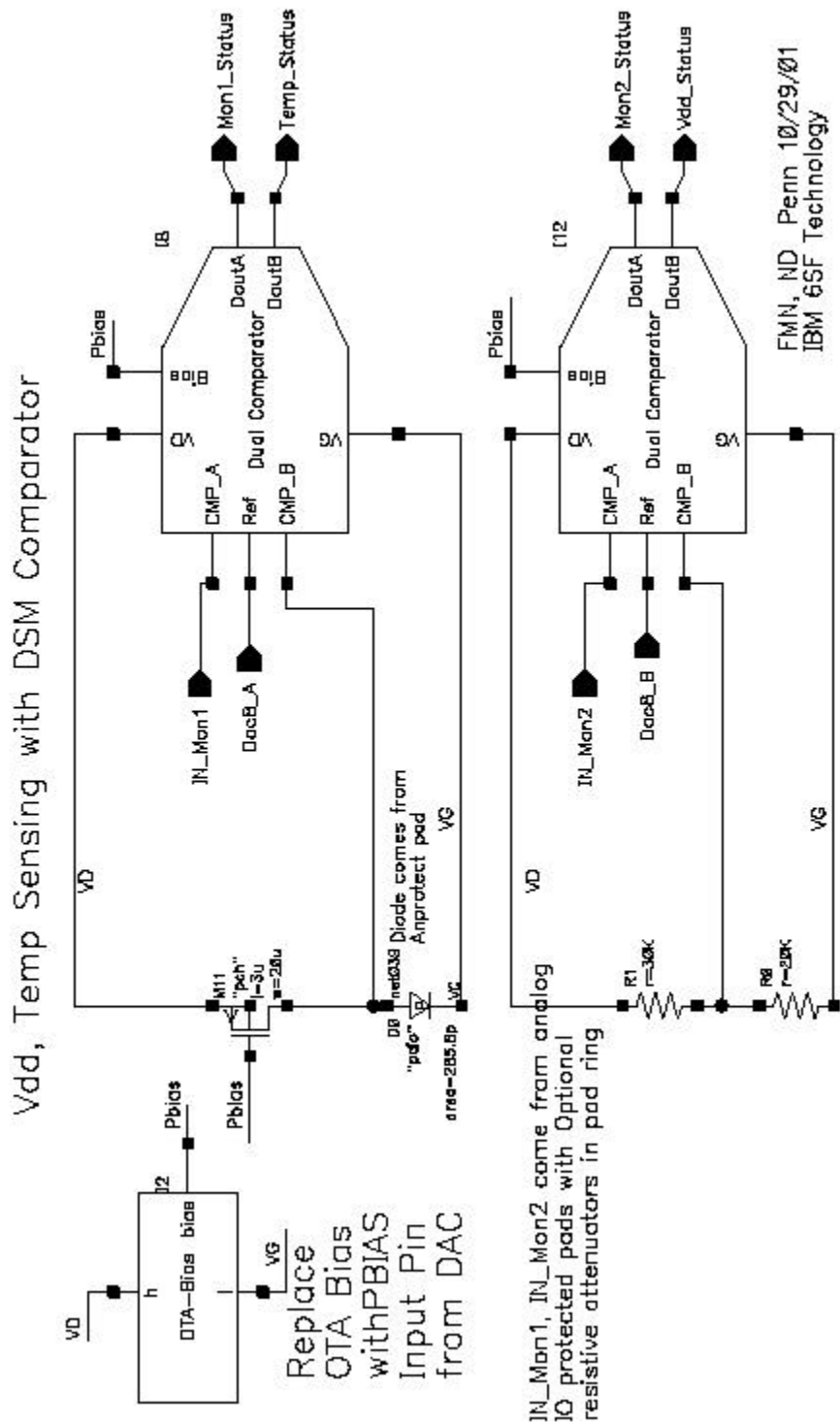   2/5∗Vdd sensing and IN_Mon2

Outputs:
- **Mon1_Status** **-** Digital Output = Hi if Mon1_Status > Dac8_A
- **Temp_Status** **-** Digital Output = Hi if Vdiode > Dac8_A
- **Mon2_Status** **-** Digital Output = Hi if Mon2_Status > Dac8_B
- **Vdd_Status**   **-** Digital Output = Hi if Vdd∗2/5 > Dac8_B

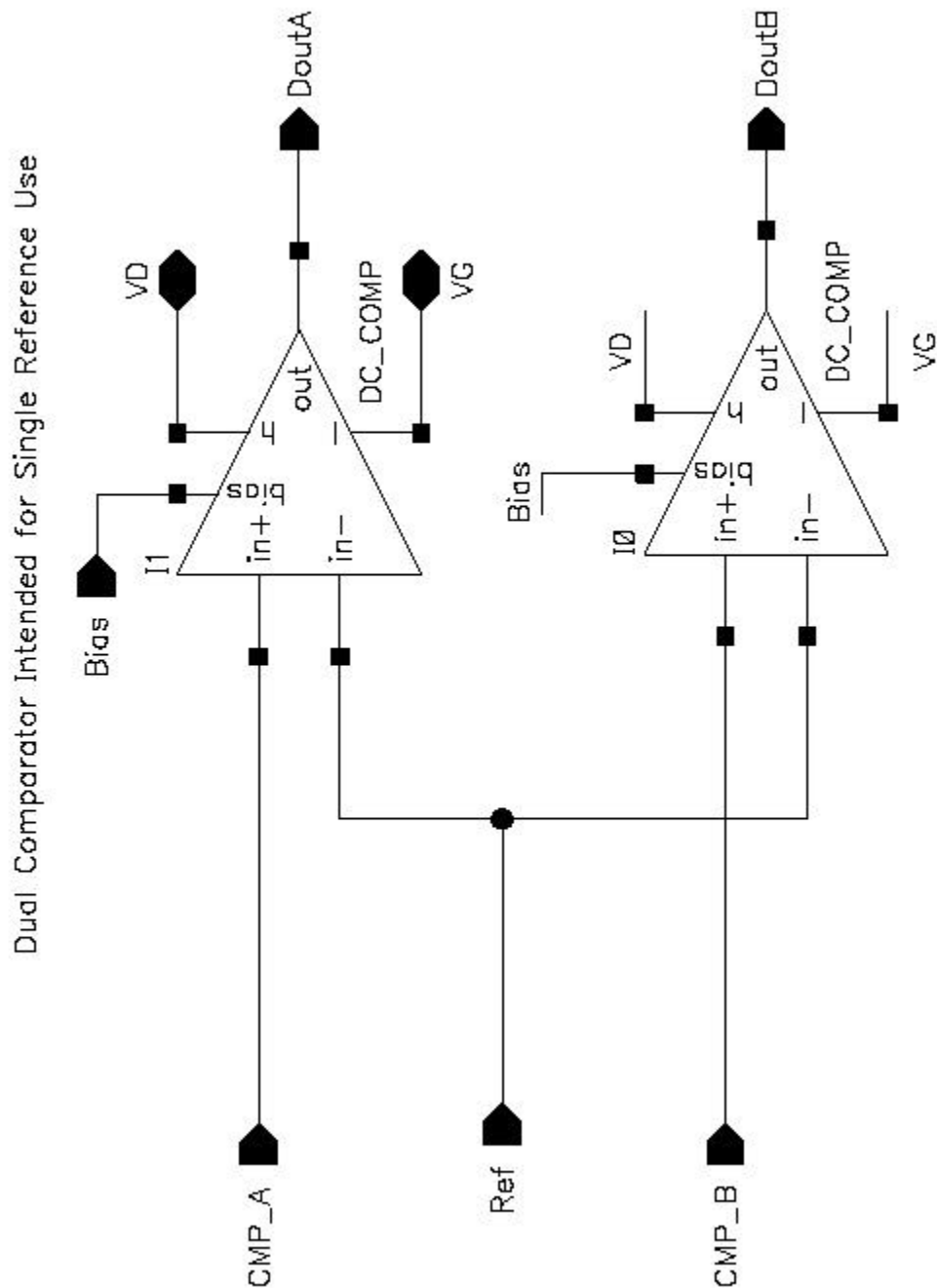Functionality: Four comparators sense voltage temperature and two indepenent monitors.   A diode copied from the Input Protection block is attached to ground and biased (M11 Top level schematic) with a constant current of ~17μA utilizing the CERN OTA_Bias block.   Temperature on the chip will be sensed by examining the comparator output **Vdd_Status** for several values of reference voltage **Dac8A**. Similarly the Value of Vdd will be sensed by comparing at the voltage at the junction of resistors R0 (30K) and R1(20K) with settings of **Dac8_B**.   In addition two pads that may be wired as resistor dividers or as direct inputs will be available for comparison with **Dac8_A** and **Dac8_B**.

An explanation of the comparator block is given in the **CMOS_cmp** writeup.

V_T_Block
Top Level Schematic

Vdd, Temp Sensing with DSM Comparator

Mon1_Status

Temp_Status

Mon2_Status

Vdd_Status

Pbias

I3

DoutA
DoutB

Bias   Dual Comparator

VD   VG

CMP_A   Ref   CMP_B

IN_Mon1   DacB_A

Pbias

I12

DoutA
DoutB

Bias   Dual Comparator

VD   VG

CMP_A   Ref   CMP_B

IN_Mon2   DacB_B

M11
"pch"
l=3u
w=28u

net039 Diode comes from
D8 Anprotect pad
"pd6"   VG
area=285.8p

VD

VG

R1
r=38K

R8
r=28K

VD

VG

I2
OTA-Bias bias

VD   h

Pbias

Pbias

VG

Replace
OTA Bias
withPBIAS
Input Pin
from DAC

IN_Mon1, IN_Mon2 come from analog
IO protected pads with Optional
resistive attenuators in pad ring

FMN, ND Penn 10/29/01
IBM 6SF Technology

Dual comparator block
(note that DC_COMP is the same as CMOS_cmp)

Voltage and Temperature Measurement

◁: (i "i1(xi8~xi0~m9)" ?result "V_T_Block.t
▷: (i "i1(xi8~xi0~m10)" ?result "V_T_Block.

Input Source Follower Current

−17.140u
−17.200u
−17.260u
−17.320u

◇: (v "aux_1" ?result   □: (v "/net010" ?resu
▽: (v "/net022" ?resu

Voltage Sweep / Ref = 1V and output

3.0
2.0
1.0
0.0
−1.0

△: (v "tmp_trig" ?res   □: (v "/net010" ?resu
□: (v "/net039" ?resu

Temp Sweep / Ref=800mV and output

3.0
2.0
1.0
0.0
−1.0

0.0   10u   20u   30u

time