Progress on the development of a detector mounted analog and digital readout system for the ATLAS TRT

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***Abstract*--The 430,000 element ATLAS Transition Radiation straw tube Tracker (TRT) is divided into a central barrel tracker consisting of 104,000 axially mounted straws and two radially arranged end caps on either side of the barrel with 160,000 straws each. To achieve a track position resolution of 140μm, the front end electronics must operate at a low (2fC) threshold with a time marking capability of ~1ns. Two ASICs, the ASDBLR and DTMROC provide the complete pipelined readout chain. Custom designed FBGA packages for the ASICs provide a small enough outline to be detector mounted and the extensive use of low level differential signals make mounting the analog packages on printed circuit boards directly opposite the 40 MHz digital chips feasible. The readout electronics for the barrel occupies a potentially important part of the active tracker volume and an aggressive effort has been made to make it as compact as possible. Utilizing a single board for both analog and digital ASICS a 0.1 cm^3 per channel volume has been achieved for the active electronics. This has meant the development of 14 layer boards with four levels of blind vias to separate analog and digital functionality. The design of the packages and boards along with performance measurements is discussed.**

I. Introduction

Analog signal processing requirements for the ATLAS TRT require detection avalanche signals from a few primary drift ions in the TRT straw sensors with nanosecond timing precision at triggering rates as high as 18MHz. The closely packed 4mm diameter the straws present a high density readout.

These requirements led to the design of a custom ASIC (ASDBLR) with a bandwidth of 33MHz, very close to the system clock frequency of 40MHz. The 30 - 80cm long straw tube wire that connects to the amplifier input can potentially act as an antenna that is only about a factor of two shorter than an ideal ¼ wavelength antenna for the beam clock at these frequencies. Thus the straw sensors and analog ASIC's require a high degree of electrical isolation from the digital readout. References such as [1] provide excellent guidelines for wiring and shielding high bandwidth readout systems with similar constraints, but usually these concern single channel systems rather than the close packed sea of sensors and readout that comprise the TRT. Our objective has been to try to employ sensible grounding and shielding rules treating the TRT end tension plates and sensor interconnect networks as the basic analog reference and utilizing board planes and detector support structures as part of a faraday shield.

The two main configurations of the TRT detector are the end cap wheel where straws are placed radially outwards from the beam and the barrel where straws are placed axially in 1.6m modules that form cylinders around the beam line. More detailed information about the TRT design may be found in Reference 2.

II. Brief Description of the Front End Electronics Architecture

The front end ASICS have been discussed in detail in reference 3 and 4. Two ASDBLRs and one 16 channel DTMROC form the basic front end readout block. The signal processing flow is shown in Figure 1. The ASDBLR provides the complete analog signal processing chain. It receives and shapes the straw signals eliminating the long ion tail and provides baseline restoration prior to presenting the signal to a dual comparator section. The output of the ASDBLR is a three level differential (ternary) current switching a constant current of 400μA between outputs in 200μA steps. A custom ternary receiver on the DTMROC provides a low impedance source for the ASDBLR ternary outputs. Comparator threshold control is provided by 8 bit DAC's on the DTMROC ASIC. The low level comparator on the ASDBLR is used to signal the presence of the first primary electrons ionized by charged particle tracks in the straw. This is encoded in the first ternary step output. The second comparator is set to a higher level and optimized for discrimination of total energy deposition. Thresholds will be adjusted to detect the presence of Transition Radiation photons created by highly relativistic particles traversing polypropelene films between the straws. Xenon in the straw tube gas is a highly efficient convertor for these photons.

The DTMROC digitizes the decoded ASDBLR low level comparator output in 3.1ns time bins storing eight time bins and the High threshold output level at every beam crossing clock in a 2.5μs pipeline. Data in the pipeline from three consecutive beam crossings are latched and stored in a readout FIFO if a level one trigger is decoded by the DTMROC. Off chip communication with the back end system (ROD and TTC) utilize low level differential signals compatible with LVDS standard. The ASDBLR ASIC has been described in Reference 3 and the DTMROC ASIC in Reference 4.

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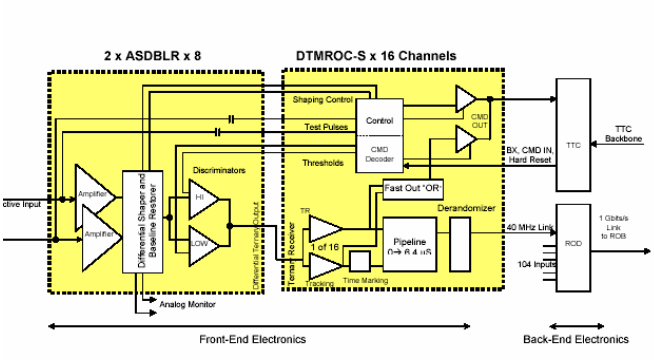

Figure 1 The on detector signal processing chain for the ATLAS TRT is shown in the figure above. Two ASDBLR's and one DTMROC provide the full Front end readout. Low level differential signals are used for all off chip communication.

III. TRT End Cap Wheel Readout

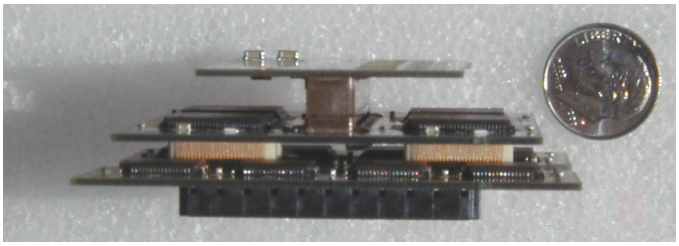

Figure 2 The photograph above shows a 64 channel detector mounted endcap wheel readout board. The upper board is an unstuffed connector board for power and data. The next lower board (center) houses four DTMROC ASICS and primarily handles digital I/O. The bottom board (4100mm^2) has eight ASDBLR ASICS and connects directly to the end cap wheel straw anode connectors.

In the end cap wheel the straws are aligned radially away from the beam pipe. The readout electronics is placed at the largest radius where the wire anodes connect to the electronics through an intermediate connector board just outside the straw ends. An area of 64mm^2/wire is available at the outer surface of the end cap wheels and vertical height of more than 3cm allows the use of separate analog and digital boards. A prototype of the end cap wheel electronics is shown in Figure 2. Eight ASDBLR ASICS are mounted on the board closest to the straw ends (lowest in the figure). Connection to the straws and reference to the straw cathodes is provided by two miniature connectors on the underside of the board. Ternary outputs from the ASDBLR's go to four floating connectors between boards and are directed to four DTMROC chips on the board just above where digital signal processing, ASDBLR control and communications with off detector electronics is handled. The top board in the figure is the data and power connector (shown unstuffed). This readout format has been highly successful. In test beam measurements operational threshold levels were achieved that are nearly at the limit due to intrinsic noise in the front end amplifiers. A small amount of clock feed through is observed through the test pulse lines from the DTMROC, but it is far below the desired operational 2fC threshold level. A publication is in preparation on these studies.

IV. TRT Barrel Readout

The barrel electronics is located in a very narrow region at each end of the barrel. Cables, electronics, cooling pipes cooling plate, support frame, cooling and module gas lines are allocated approximately 25mm along the direction of the beam. The density of readout is about 30mm^2/wire about twice that of the end cap wheel. Electronics assemblies are limited to varying triangular foot prints with no more than 16mm of height. After several prototypes we have converged on a single board design that houses both analog and digital ASICS. A liquid cooling plate is attached to the digital side of the board and the total height of the assembly including cooling plate and connectors is less than 1.5 cm. Although variations in geometry by end and by module layer will require a total of 16 different board and cooling plate footprints, the design approach will be the same for each. The basic rule is to separate the board into analog and digital domains splitting a total of 14 layers equally between them. Four levels of blind and vias allow isolation of analog and digital signals within their separate domains. All fast signals are low level differential.

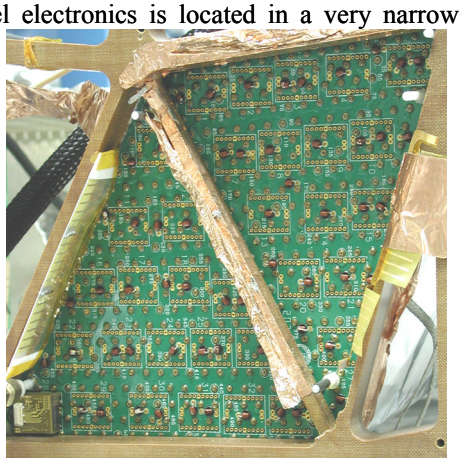

Figure 3 The picture shows the end of a barrel module Type I. The trapezoidal cross section is split into two triangles by the support structure. Connection to the straws is arranged in rectangular sets of 16 sockets with 6 cathode reference sockets at each location.

Barrel boards are arranged in 16 channel ASIC triplets consisting of two eight channel ASDBLR's and one DTMROC. Analog connectors and ASDBLR's face inwards towards the barrel module. Two signal layers separated by an analog ground plane utilize short vias to isolate the inputs from the rest of the board. An empty layer below the input signal layers and a power layer with cutouts corresponding to the location of input signals minimize the capacitance to the other board layers. The analog side is enclosed by a second

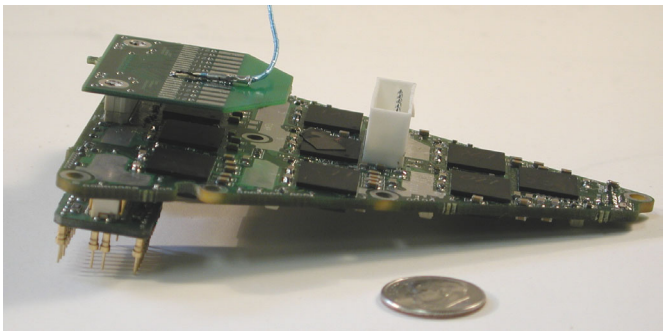

Figure 4 The photograph above shows a module 1 barrel board with a protection input board attached in one location at the bottom of the board and the data cable connector board (unstuffed) attached to the top of the board. The DTMROC FBGA chips can be seen at the top of the board which faces away from the module end. This 4600mm^2 board reads out 160 channels.

analog ground plane with a power layer finally facing outwards towards the digital side.

The DTMROC ASICS are placed on the outermost layer away from the barrel. Analog and digital grounds are completely separate but provision is made on the digital side to connect them using surface mount resistors placed around the perimeter of the triangular footprint. At these locations direct access to analog and digital ground is provided with large pads to allow low inductance connection in any combination of analog and digital ground to the conductive support structure of the barrel module. Although not proven in a multi-module environment it is our intention to attach the analog ground directly to the support frame of the barrel module enclosing the frame and analog layers of the board in a faraday shield.

A sketch depicting important aspects of the current 14 layer barrel board is shown in Figure 5. Digital signals are routed on the upper two layers of the board to isolate them as much as possible from the analog side and digital power and ground are routed on the next lower layers. The remaining inner layers are largely left open except that a ring of analog ground is routed around the perimeter of the board. This approach is intended to minimize capacitance between analog and digital power planes and to keep digital signal lines from broadcasting directly to the analog side. Preliminary tests including test beam studies have shown that it is a largely successful technique. Remaining channels with excess clock noise appear to be due to a combined effect of board and module.

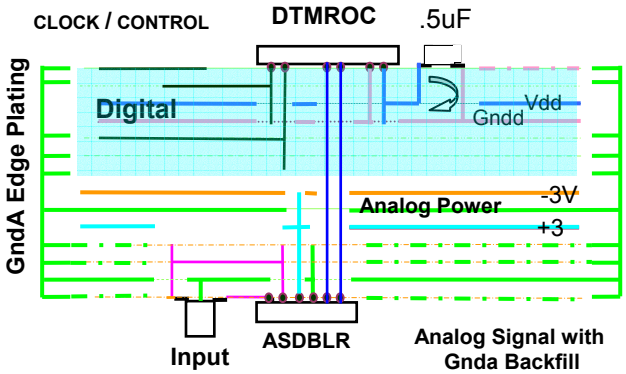

Figure 5 The drawing above illustrates major points of our 14 layer analog and digital barrel board layout. The shaded *digital* region is isolated from the analog region. On the digital side, capacitors near the DTMROC help keep currents due to clock related chip activity local. Analog power layers above the inputs shield the low level analog inputs from digital transients.

V. Calibration and Noise Tests

Using the combined ASDBLR and DTMROC readout we can construct several noise tests. As noted in Section II the DTMROC stores the status of the low level discriminator for each beam crossing in eight 3.1ns time bins in a 2.5μs time pipeline. For each level 1 (L1) sent by the TTC the DTMROC saves the digitized data from three beam crossings for all channels in a readout buffer. This snapshot of the the low level discriminator output can be used in several ways:

1) Calibration with test pulse - Generating L1 with an appropriate delay after injection of a test input charge allows the threshold versus input charge to be calibrated..

2) Noise - Generating L1 at random times with a fixed threshold we can infer an absolute noise for that threshold. Ramping over threshold values provides data for triggering rate versus threshold.

In the Figure 6 the diagnostic power of the threshold ramp is shown. Two plots show results for 16 channels at one location on the barrel board shown in Figure 4. At each threshold setting (DAC count) one hundred L1 triggers are generated. For each channel the number of L1 triggers with a low level comparator above threshold is recorded. In the upper plot even numbered channels are shown to require a higher threshold maintain the same occupancy as odd numbered channels. This is a strong indicator that one of the test pulse lines that go to odd and even numbered channels separately is picking up signals from an external source. Removing a series resistor in the path of the test pulse between the DTMROC and ASDBLR eliminates the odd and even differences. The pickup is shown to be synchronous with the beam crossing clock in Figure 7 where the occupancy for each of the time 24 3.1ns time bins is plotted for two even and one odd channel with the test pulse components in place.

VI. Conclusions

We have designed two types of boards utilizing the DTMROC and ASDBLR custom ASICS. Due to the amount of space available in the end cap wheel we were able to use a layered approach with dedicated analog and digital boards. This was by far the simplest approach and has resulted in relatively few design cycles. The barrel boards after several iterations are converging on a single design approach that combines analog

and digital functionality on the same board. Our approach with this board has been to separate analog and digital domains keeping inputs referred to an analog ground plane and reducing the capacitance from inner layer input traces to other layers. It is important to shield the inputs from the digital side using well filtered analog supply planes that are closed over the inputs, but several layers away. Digital and analog grounds are connected only at the perimeter of the board where resistors help control current passing between domains. Our work now focuses on interactions between the barrel module and the barrel boards. Significant clock pickup is exhibited in several locations of our current prototype when connected to the module only. We are awaiting a new prototype with edge plating and significantly increased analog ground fill on analog layers.

Software tools have been developed to exploit the DTMROC readout and are being successfully employed to quantify noise and pickup issues.

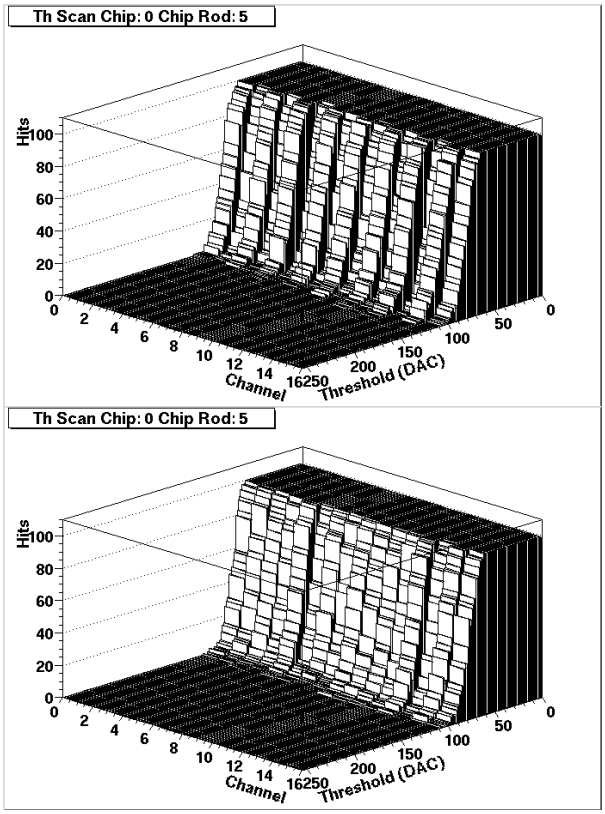

Figure 6 The figures above show a threshold scan for one DTMROC on the board pictured in Figure 4. Evidence of pickup in one of the test pulse lines between the DTMROC and ASDBLR is displayed in the upper figure where even numbered channels are shown to require a higher threshold to match triggering rates of odd numbered channels. This ~8 count difference disappears when a series resistor in the test pulse path is removed. For reference a 2fC signal will trigger the low level threshold with 50% efficiency at ~120 DAC counts.

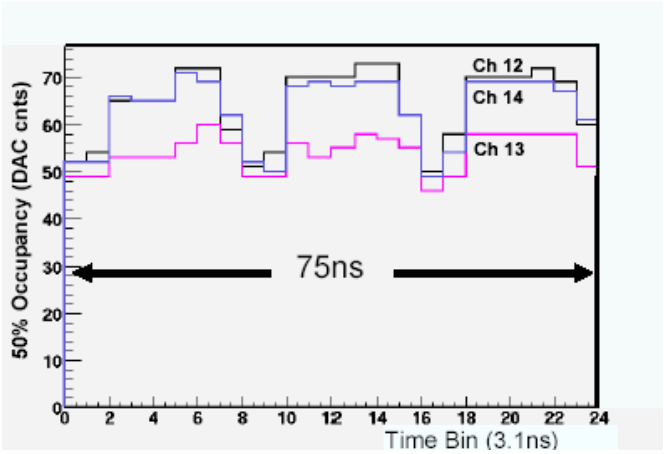

Figure 7 The plot above shows the measured 50% occupancy thresholds by time bin with no injected signal for three DTMROC channels found to have additional pickup on the even test pulse line (See Figure 4). The plot shows that the occupancy is modulated by the 40MHz beam clock. The clock synchronous pickup was reduced to expected levels when test pulse components were removed.

VII. References

[1] Ralph Morrison, Grounding and Shielding Techniques in Instrumentation New York : Wiley, c1977

[2] Atlas Inner Detector Technical Report Volume 1, CERN/LHCC 97-16, April 30, 1997.

[3] N. Dressnandt, N. Lam, F.M. Newcomer, R. Van Berg and H.H. William Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL Technology, , IEEE (2000) Trans. On Nucl. Sci. V48 n4 p1239

[4] F. Anghinolfi, N. Dressnandt, P. Eerola et. al., DTMROC-S deep sub-micron version of the readout chip for the TRT detector in ATLAS, 8th workshop for electronics for LHC experiments, Colmar, France Sept 2002, pp 95-99.